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Novel Non-Linear Control of DFIG and SSSC for Stability Increment of Power System

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ABSTRACT

This study examines stability improvement of the power system which includes Double Feed Induction Generators (DFIGs) and Static Series Synchronous Compensator (SSSC). The proposed nonlinear controller is designed based on the terminal sliding mode control theory. A sliding mode observer is also developed to remove the need to access the information of all the state variables. The final closed-loop of the power system modeling is robust against parameter variations and uncertainties. The limitations of the control signals in the process of controller design are also considered. The application of such a method increases the stability margins and results in higher robustness degrees. A comparison with other nonlinear approaches such as back-stepping and feedback linearization approaches is carried out. The results show the faster and more reliable convergence rate of the power system-controlled trajectories to reach back to the equilibrium point after occurring a sudden fault. The results are obtained by performing a simulation on the standard 39-Bus, 10 machines NEW ENGLAND power system.

Nomenclature

δ_i	Rotor angle of the ith generator
ω_i	Rotor speed of the ith generator
$\acute{E}_{qi}$	Internal voltage of ith generator in q-axes
$\acute{E}_i$	Internal voltage of the ith generator
I_{di}	Stator current of the ith generator in d-axis
I_{qi}	Stator current of the ith generator in q-axis
v_{fi}	Excitation voltage of the ith generator
M_i	Moment of inertia of the ith generator
P_{mi}	Mechanical input power of the ith generator
u_d	Signal control of DFIG
δ_{0i}	Rotor angle of the ith generator in steady state
ω_{0i}	Rotor speed of the ith generator in the steady state
V_i	Amplitude of the ith generator terminal voltage
X_i	Equivalent reactance of DFIG in steady state
θ_i	Phase of the ith generator terminal voltage
$\acute{T}_{d0i}$	Time-constant of the ith generator excitation coil
x_{di}	d-axis steady state reactance of the ith generator
$\acute{x}_{di}$	d-axis transient state reactance of the ith generator
x_{qi}	q-axis steady state reactance of the ith generator

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I. Introduction

The consumption of electrical energy is increasingly growing in today's industrial world. The need for more electrical energy brings attention and widespread investment in building new electrical transmission lines and power plants. The problems of environmental-friendly and safety of the newly built power plants have also been a major factor in generating electrical energy. Paying attention to decreasing the amount of consumption of fossil fuels and pollutant and greenhouse gases in traditional electrical power plants have paved the way to replace them with solar or wind power generation. Due to the emerging technological growth and suitable infrastructure, building wind-turbine power plants has gained a tremendous amount of attention now. In Germany and France, the nuclear power plants are rapidly replacing with wind-turbine ones. For instance, in Germany, five-gigawatt nuclear power plants are replaced with a thousand wind-turbine plants by implementing DFIGs [1].

The second factor in the electrical energy industry is the high cost of constructing new transmission lines to transmit and distribute electrical power. The increase in power energy consumption with the natural limitation of the current transmission networks brings about the problems of insulation, stability, and thermal capacity, [2-3]. Hence, there is a need to distribute the maximum possible power through the available electrical networks. Flexible AC Transmission systems (FACTS) are now spread and installed in electrical networks as a solution to increase transmission capacity. One of the important FACTS components is SSSC, [4-6]. In the SSSC structure, passive elements are not employed. High level of switching mode in SSSC results in the injection and absorption of active electrical power at low cost and high speed.

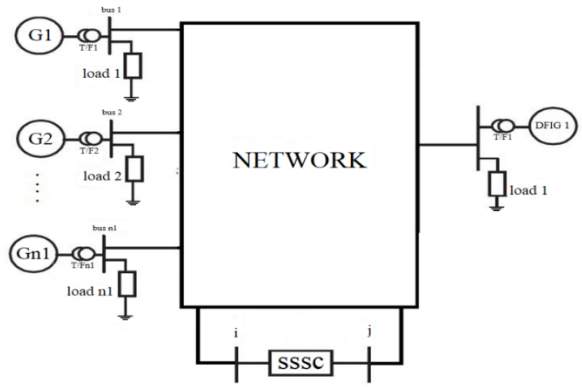
Maintaining the stability of power networks after occurring a sudden fault is one of the important issues in Transient Stability Assessment (TSA). Moreover, the power system should also be robust against unwanted disturbances. Utilizing DFIGs in addition to SSSC to increase the stability and endurance of power networks is now a major research trend. Applying a suitable control on DFIGs, SSSCs and excitation circuits of synchronous generators will lead to stability improvement [7-10].

In most of the existing research in improving the stability of power networks, power system stabilizers are developed based on a local linear model around the operating point, [11, 12]. In this research area, Linear Matrix Inequalities (LMIs) or Root-Locus methods are implemented to design a linear control law that stabilizes the system all around the operating point. However, power systems are complex nonlinear systems with a high amount of coupling between their components. They are always under enormous power demand to be supplied. Therefore, the operating point varies with different conditions [13]. Hence, assuming local linear models about the operating point and designing local linear control laws result in a closed-loop control system with very low stability margins. Naturally, some researchers have paid attention to implementing nonlinear control laws to design power system stabilizers. For instance, the feedback linearization method by output feedback is implemented in [14] to improve stability with respect to linear control laws. However, in this approach, the exact system model is required to be known. However, usually, there is a need to access high-order derivatives of the signals. Hence, applying this linearization method is very limited in many cases. In [15], linearization by output-feedback is offered, in which, the designer should access the information of all the state variables of the system. Moreover, this method is not robust against parameter variations and structured uncertainties. In the literature survey [16-18], adaptive control techniques for parameter estimation were implemented. These methods have a higher robustness degree with respect to the above-mentioned approaches. However, information on all state variables of the system is needed to be available in the design methodology. In [19, 20], adaptive backstepping approaches are developed to cope with the above difficulties in the design of the nonlinear control laws. However, in this design trend, the coupling effect of SSSC and DFIG are not equally employed to improve stability. Moreover, these methods are again not completely robust performance compared to the existing structured uncertainty in the power system.

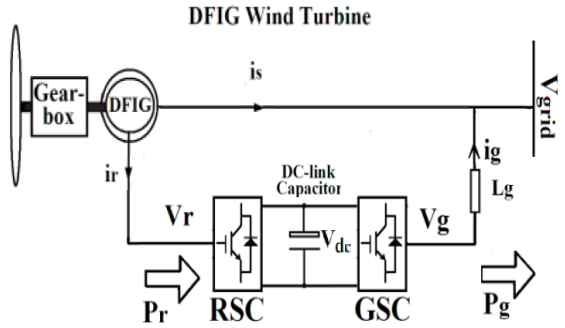
In [21-22], adaptive backtracking and multi-input DSC are used to improve stability in which the design of the controller is limited by the number of inputs and outputs. In [23], the transient energy function (TEF) is used. The main problem of using TEFs is the complexity of the controller design for large networks.

In this paper, a terminal sliding mode approach is proposed to enhance the performance of the power system in presence of both DFIG and SSSC. In this regard, by control of the DC link voltage profile, DFIG modeling is considered as a synchronous generator. Besides, another sliding mode observer is also implemented in the design procedure to remove the need to access the information of all the state variables of the system. The close-loop observer-based controller is proved to be stable. In the proposed method, certain existing limitations on the signals in the system are also considered in the design stage. The application of such a method increases stability margins and results in higher robustness degrees.

This paper is organized as follows: In Section 2, a brief review of the power system modeling which includes both DFIG and SSSC is presented. Section 3 until 7is devoted to the design procedure of the proposed control law by applying a terminal sliding mode in addition to a sliding mode observer. In this section, particular attention is paid to the implementation of the designed controller and observer. In Section 8 a simulation is performed to investigate the application of the proposed controller on the specific power network. Also, a comparison is made with the existing results in the literature.



a)



b)

Fig. 1. a) The schematic diagram of the considered case study, b) the diagram of DFIG.

II. Power System Modeling

Fig. 1 depicts the general form of the evaluated power system and the case study. The considered power system consists of n1 synchronous generators, one DFIG component plus one SSSC. It is assumed that the transmission lines resistances are negligible. Hence, the transmission lines are modeled only by $\overline{Y}_{ij} = jB_{ij}$. In the formulation of the power system model, the mechanical power input to the generators is assumed to be constant. Moreover, the resistance of stators is negligible. The total consumed power in each bus is modeled by $Y_i = G_i - jB_i$ [24]. The following mathematical model describes the multi-machine power system including DFIG and SSSC where, V_i و θ_i are the amplitude and phase angle of the connected bus voltage, respectively.

$$\begin{cases} \dot{\delta}_i = \omega_i - \omega_{0i} \\ \dot{\omega}_i = \dfrac{1}{M_i}\left[P_{mi} - \dfrac{\acute{E}_{qi}V_i \sin(\delta_i - \theta_i)}{\acute{x}_{di}} - \dfrac{{V_i}^2 sin2(\delta_i - \theta_i)}{2x_{qi}\acute{x}_{di}}\right] \\ \dot{\acute{E}}_{qi} = \dfrac{1}{\acute{T}_{d0i}}\left(v_{fi} - \dfrac{\acute{E}_{qi}x_{di}}{\acute{x}_{di}} - \dfrac{V_i(x_{di} - \acute{x}_{di})\cos(\delta_i - \theta_i)}{\acute{x}_{di}}\right) \end{cases} \quad (1-a)$$

$$\begin{cases} \dot{\delta}_i = \dfrac{1}{\acute{E}_i T_{0i}}[-T_{0i}(\omega_i - \omega_0)\acute{E}_i - \dfrac{X_i - \acute{X}_\iota}{\acute{E}_{qi}T_{0i}} V_i \sin(\delta_i - \theta_i) + T_{0i}\omega_0 u_{di}\cos(\delta_i)] \\ \dot{\omega}_i = \dfrac{\omega_0}{2H_i}\left[P_{mi}\dfrac{\omega_s}{\omega_i} - B_i\acute{E}_i V_i \sin(\delta_i - \theta_i)\right] \\ \dot{\acute{E}}_i = \dfrac{1}{T_{0i}}\left[-\dfrac{X_i}{\acute{X}_\iota}\acute{E}_i + \dfrac{X_i - \acute{X}_\iota}{\acute{X}_\iota}V_i\cos(\delta_i - \theta_i) + T_{0i}\omega_0 u_{di}\sin(\delta_i)\right] \\ \dot{V}_{dc} = \dfrac{1}{C_{dc}V_{dc}}\left[P_r - \dfrac{1}{x_g}(u_{g2}cos(\theta_i) - u_{g1}sin(\theta_i)\right] \end{cases} \quad (1-b)$$

$$\begin{cases} \dot{V}_i = \sum_{j=1}^{n+p} c_{ij}H_j + \sum_{j=1}^{n+p} d_{ij}v_{fj} + \sum_{j=1}^{n+p} k_{ij}\,r \\ \dot{\theta}_i = \sum_{j=1}^{n+p} c_{i+n+2,j}H_j + \sum_{j=1}^{n+p} d_{i+n+2,j}v_{fj} + \sum_{j=1}^{n+p} k_{i+n+2,j}\,r \end{cases} \quad (1-c)$$

where Eq. (1-a) is related to the synchronous generators. In this study, governor modeling is not considered as it creates a time delay in the stability study. Eq. (1-b) models the DFIG, and Eq. (1-c) describes the bus voltages of the connected buses to the DFIG, SSSC, and synchronous generators. In the above model, v_{fi} (excitation voltage of synchronous generators) represents the control input in the generator excitation circuit, u_{di} is the control input of the RSC part of DFIG, and r is the control signal in the SSSC component [25-26]. Eq. (1-b) models the DFIG. In this equation, $\acute{E}_i$ is the internal voltage of the i[th] generator, B_i is the reactance of the admittance matrix of the system between the DFIG and its connected bus. Also, $u_{di} = V_{ri}cos(\Phi_{ri})$ is the applied voltages to the DFIG rotor, where V_{ri} and Φ_{ri} are amplitude and phase in polar coordinates, respectively. Due to the structure of back-to-back DFIG converters and the presence of a relatively large capacitor in the DC link, if a suitable controller is not used, it can lead to an adverse effect on the stability of the system. Here, the dynamics of capacitor voltage changes are also considered in the equations. Full details and how to obtain Eq. (1) are given in Appendix A. Eq. (1-c) formulates the relations between the amplitudes and phases of the synchronous generators, the DFIG, and the SSSC with its connected buses. The mathematical Eq. (1) is derived based on the algebraic power balance equations at buses which synchronous generators, DFIG and SSSC are connected to. It is assumed that the SSSC component only generates and consumes reactive power, and its series reactance is zero [27].

Here, considering that the SSSC only produces and absorbs reactive power, the voltage of the capacitor voltage component related to the SSSC has insignificant changes practically, and for this reason, its dynamics have been neglected.

III. Design of terminal sliding mode nonlinear control law

According to Eq. (1), the goal is to convert the equations into the form of state Eq. (2) and to design the terminal sliding controller. Let's consider the n[th]-order nonlinear strict feedback with uncertainty d in the following form:

$$\begin{aligned}&\dot{x}_1 = x_2\\&\dot{x}_2 = x_3\\&\dot{x}_3 = x_4\\&\dots\\&\dot{x}_{n-1} = x_n\\&\dot{x}_n = F(x_1, x_2, .., x_n) + G(x_1, x_2, .., x_n)u\\&\qquad\qquad + d(x_1, x_2, .., x_n)\end{aligned} \tag{2}$$

where $x_i \in$ R is the i[th] element of the state-vector for i=1, 2, …, n, and d represents the uncertainty in the system model with the upper bound D>0, F , G are differentiable n-th order with $G \neq 0$, and u∈ R is the control input. Let's define a sliding surface in the following form:

$$S = x_3 + c_2 x_2 |x_2|^{\alpha_2} \mathrm{sgn}(x_2) + c_1 x_1 |x_1|^{\alpha_1} \mathrm{sgn}(x_1) \tag{3}$$

In the above, c_1 و c_2 are constant design factors and α_1 و α_2 satisfy the condition:

$$\begin{cases} 0 < \alpha_2 < 1 \\ \alpha_1 = \dfrac{\alpha_2}{2 - \alpha_2} \end{cases} \tag{4}$$

The sliding surface of (3) can be also written as:

$$S = x_3 + c_2 {x_2}^{\alpha_2} + c_1 {x_1}^{\alpha_1} \tag{5}$$

In the sliding condition, $S = 0$, we have:

$$\begin{aligned}&S = x_3 + c_2 {x_2}^{\alpha_2} + c_1 {x_1}^{\alpha_1} = 0 \qquad (6)\\&\rightarrow x_3 = -c_2 {x_2}^{\alpha_2} - c_1 {x_1}^{\alpha_1}\end{aligned}$$

Therefore, (2) and (6) lead to

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = -c_2 {x_2}^{\alpha_2} - c_1 {x_1}^{\alpha_1} \end{cases} \tag{7}$$

Note that c_1 and c_2 are positive scalars that should be designed in such a way that the polynomial $p^2 + c_2 p + c_1$ becomes a Hurwitz polynomial. This fact guarantees that the equilibrium point is stable, and it converges in a limited time. See [28] for complete proof. Differentiating Eq. (6) and Eq. (2) results in the following control law:

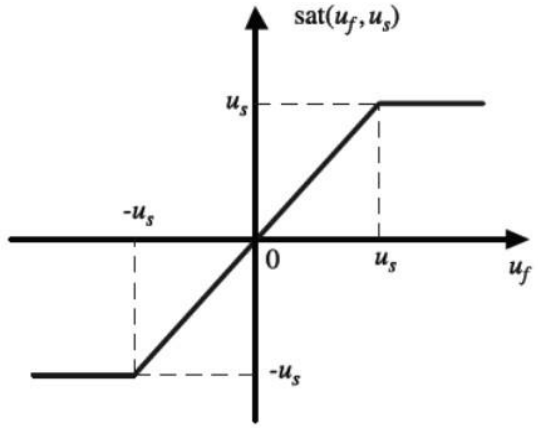


Fig. 2. Saturation function.

$$u = b^{-1}(x)\left[-f(x) + sat(u_f, u_s) - ksgn(s)\right] \tag{8}$$

$$u_f = -c_2 \alpha_2 {x_2}^{\alpha_2 - 1} x_3 - c_1 \alpha_1 {x_1}^{\alpha_1 - 1} x_2 \tag{9}$$

In the above, $sat(u_f, u_s)$ is the saturation function depicted in the below figure:

The assumed condition leads to choosing $k = D + \eta$ and constant $\eta > 0$ with $u_s > 0$ as the threshold value.

IV. Implementing the terminal sliding control design to power system

To apply the theory of the terminal sliding mode technique to the power system described by Eq. (1), first, it is essential to define a new set of variables [29]:

$$\begin{cases} \mathrm{x_{1i}} = \delta_\mathrm{i} - \delta_\mathrm{i0} \\ \mathrm{x_{2i}} = \omega_\mathrm{i} - \omega_\mathrm{0i} \\ \mathrm{x_{3i}} = \dfrac{1}{\mathrm{M_i}}\left[\mathrm{P_{mi}} - \dfrac{\acute{\mathrm{E}}_\mathrm{qi}\mathrm{V_i}\sin(\delta_\mathrm{i} - \theta_\mathrm{i})}{\acute{\mathrm{x}}_\mathrm{di}} - \dfrac{{\mathrm{V_i}}^2 \sin 2(\delta_\mathrm{i} - \theta_\mathrm{i})}{2\mathrm{x_{qi}}\acute{\mathrm{x}}_\mathrm{di}}\right] \\ 1 < \mathrm{i} < \mathrm{n_1} \\ \mathrm{x_{3i}} = \dfrac{1}{\mathrm{M_i}}\left[\mathrm{P_{mi}}\dfrac{\omega_\mathrm{s}}{\omega_\mathrm{i}} - \mathrm{B_i}\acute{\mathrm{E}}_\mathrm{i}\mathrm{V_i}\sin(\delta_\mathrm{i} - \theta_\mathrm{i})\right] \\ \mathrm{n_1} + 1 < \mathrm{i} < n \end{cases} \tag{10}$$

Due to the existing difference between the speed of synchronous generators and DFIG, $\mathrm{x_{3i}}$ is introduced in a different form.

The variables of Eq. (10) are strictly defined to achieve a suitable feedback model. Here, $\mathrm{x_{1i}}$ is the error related to the internal angle of the generator and the optimal value of the internal angle before the fault occurs for the i-th machine, $\mathrm{x_{2i}}$ is the error of the rotor speed compared to the synchronous speed, and $\mathrm{x_{3i}}$ is the difference value between the output power and the output of the i-th machine. Because the studied synchronous generators are of the salient pole type and the DFIG generator is of the flat-pole type, the definition of synchronous generators and The DFIG generator is different. Applying the new set of variables in Eq. (1):

$$\begin{cases} \dot{\mathrm{x}}_\mathrm{1i} = \mathrm{x_{2i}} \\ \dot{\mathrm{x}}_\mathrm{2i} = \mathrm{x_{3i}} \\ \dot{\mathrm{x}}_\mathrm{3i} = \mathrm{f_{Ti}} + \sum_{\mathrm{j=1}}^{\mathrm{n+2}} \mathrm{g_{Tij}v_{fj}} + \sum_{\mathrm{j=1}}^{\mathrm{n+2}} \mathrm{L_{ij}\,r} \end{cases} \tag{11}$$

The above equations will transform to the following matrix form

version:

$$\begin{cases} \dot{X}_1 = X_2 \\ \dot{X}_2 = X_3 \\ \dot{X}_3 = F_T + G_T V_f + Lr \end{cases} \quad (12)$$

where:

$$V_f = [v_{f1}\ v_{f2}\ ..\ v_{fn-1}\ u_d\ ]^T$$
$$X_1 = [x_{11}\ x_{12}\ ..\ x_{1n}]^{T,}$$
$$X_2 = [x_{21}\ x_{22}\ ..\ x_{2n}]^T$$
$$,X_3 = [x_{31}\ x_{32}\ ..\ x_{3n}]^T \quad (13)$$

Now, according to Eq. (12), a new control input of the form $U = G_T V_f + Lr$ is defined. This new control input consists of n+1 components.

$U = [u_1\ u_2\ ..\ u_{n+1}]^T$.

In the final stage, with the definition of the sliding surface of the form:

$$s_i = x_{3i} + c_{2i}x_{2i}^{\alpha_{2i}} + c_{1i}x_{1i}^{\alpha_{1i}} \quad (14)$$

The control inputs will be obtained as:

$$u_i = [-f_i(X) + sat(u_{fi}, u_{si}) - k_i sgn(s_i)] \qquad u_{fi} = \quad (15)$$

$$-c_{2i}\alpha_{2i}x_{2i}^{\alpha_{2i}-1}x_3 - c_{1i}\alpha_{1i}x_{1i}^{\alpha_{1i}-1}x_{2i} \quad (16)$$

According to Figure 2, the use of the saturation function causes a significant reduction in the output chattering phenomenon .

V. Design of the sliding mode observer

In the power system described by Eq. (1), the angle of each generator rotor and the amplitudes and phases of the terminal voltages of all the generators are accessible for controller design. However, the designer does not access the information on the remaining state variables. Therefore, an observer is needed to estimate these variables. In this paper, a sliding mode observer is proposed. The nonlinear system in Eq. (3) which has only one output is considered in the following way [30-31]:

$$\begin{cases} \begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \vdots \\ \dot{x}_{n-1} \\ \dot{x}_n \end{pmatrix} = \begin{pmatrix} x_2 + g_1(x_1, u) \\ x_3 + g_2(x_1, x_2, u) \\ \vdots \\ x_n + g_{n-1}(x_1, x_2, \dots, x_{n-1}, u) \\ f_n(x, u) + g_n(x, u) \end{pmatrix} \\ y = x_1 \end{cases} \quad (17)$$

where x_i represents the state variables, $u \in R^m$ is the control input and $y \in R$ is the only output. f_i and g_i are nonlinear analytical functions. It is possible to introduce the following sliding mode observer:

$$\begin{cases} \begin{pmatrix} \dot{\hat{x}}_1 \\ \dot{\hat{x}}_2 \\ \vdots \\ \dot{\hat{x}}_{n-1} \\ \dot{\hat{x}}_n \end{pmatrix} = \\ \begin{pmatrix} \hat{x}_2 + g_1(x_1, u) + \lambda_1 sgn_1(\bar{x}_1 - \hat{x}_1) \\ \hat{x}_3 + g_2(x_1, \bar{x}_2, u) + \lambda_2 sgn_2(\bar{x}_2 - \hat{x}_2) \\ \vdots \\ \hat{x}_n + g_{n-1}(x_1, \bar{x}_2, \dots, \bar{x}_{n-1}, u) \\ +\lambda_{n-1} sgn_{n-1}(\bar{x}_{n-1} - \hat{x}_{n-1}) \\ f_n(x_1, \bar{x}_2, \dots, \bar{x}_n, u) + g_n(x_1, \bar{x}_2, \dots, \bar{x}_n, u) \\ +\lambda_n sgn_n(\bar{x}_n - \hat{x}_n) \end{pmatrix} \\ \hat{y} = \hat{x}_1 \end{cases} \quad (18)$$

In the above, $\bar{x}_i$ is defined as:

$$\bar{x}_i = \hat{x}_i + \lambda_{i-1} sgn_{moy,i-1}(\bar{x}_i - \hat{x}_i) \quad (19)$$

where $sgn_{moy,i-1}$ is, in fact, the sgn_{i-1} which is in series with a low-pass filter to transform the saturate function from the initial discontinuous switching function. The function sgn_i is defined below:

$$sgn_i(\bar{x}_i - \hat{x}_i) = \begin{cases} 0 \ , \text{if exists } j \in \{1, .., i-1\} \\ \quad \text{Such as } \bar{x}_j - \hat{x}_j \neq 0 \\ sgn(\bar{x}_i - \hat{x}_i) \ , \text{other} \end{cases} \quad (20)$$

Due to the presence of the sgn term in the state observer modeling, there is chattering in the observed states, and considering that the saturation function is used in the main non-linear controller, the presence of chattering in the observer states does not have much effect on the performance of the controller. In fact, the above function implies that the correcting term becomes active, if and only if for all $j \in \{1, .., i-1\}$, we have $\bar{x}_j - \hat{x}_j = 0$. The λ_i coefficients determine the required convergence time for the observer.

In order to prove the convergence of the proposed observer, it is first assumed that $e_i = x_i - \hat{x}_i$. This assumption implies that $e_1 = x_1 - \hat{x}_1$and

$$\dot{e}_1 = e_2 - \lambda_1 sgn(e_1) \quad (21)$$

Considering $e_2 = \bar{x}_2 - \hat{x}_2$, if $|e_2|_{max} < \lambda_1$, then the sliding surface $e_1 = 0$ will be an attracting surface that can be reached in t_1 time, which leads to $\dot{e}_1 = 0$. Now, a continuous function with the name of $sgn_{eq}$is defined in such a way that $e_2 - \lambda_1 sgn_{eq}(e_1) = 0$. This fact results in $\bar{x}_2 = x_2$. We also have $sgn_{eq} = sgn_{moy}$, therefore,

$$\dot{e}_1 = x_2 - \left(\hat{x}_2 + \lambda_1 sgn_{eq}(x_1 - \hat{x}_1)\right) = \bar{x}_2 - x_2 = 0 \quad (22)$$

Hence, it is obtained that $g_2(x_1, x_2, u) - g_2(x_1, \bar{x}_2, u) = 0$. In this stage, for e_2, we have $\dot{e}_2 = e_3 - \lambda_2 sing(e_2)$. Similar to the above procedure, if one has $|e_3|_{max} < \lambda_2$, then after passing a limited t_2 time, $e_1 = e_2 = 0$ and $\dot{e}_2 = 0$, which both leads to $\bar{x}_3 = x_3$, and

$$\dot{e}_2 = x_3 - \left(\hat{x}_3 + \lambda_2 sgn_{eq}(x_2 - \hat{x}_2)\right) = \bar{x}_3 - x_3 = 0 \quad (23)$$

Continuing the similar path for the $n-1$ stage, $e_1 = e_2 = .. = e_{n-1} = 0$, which concludes $\bar{x} = x$ in passing t_{n-1} time, the error vector between the actual states and the observed ones converges to zero.

VI. Implementing the sliding observer for the power system including both the DFIG and SSSC

Considering the above procedure in the observer design and Eq. (1), it will be obtained that:

$$\begin{cases} \begin{pmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \end{pmatrix} = \begin{pmatrix} X_2 \\ X_3 \\ F_T + U \end{pmatrix} \\ Y = X_1 \end{cases} \quad (24)$$

where Y is the system output, i.e. the angle of the synchronous generator rotors and the DFIG. According to the above equations, the sliding mode observer will be defined as below:

$$\begin{cases} \begin{pmatrix} \dot{\hat{X}}_1 \\ \dot{\hat{X}}_2 \\ \dot{\hat{X}}_3 \end{pmatrix} = \begin{pmatrix} \hat{X}_2 + \lambda_1 \mathrm{sing}_1(X_1 - \hat{X}_1) \\ \hat{X}_3 + \lambda_2 \mathrm{sing}_2(\bar{X}_2 - \hat{X}_2) \\ F_T(\bar{X}) + U(\bar{X}, u) + \lambda_3 \mathrm{sing}_3(\bar{X}_3 - \hat{X}_3) \end{pmatrix} \\ Y = X_1 \end{cases} \quad (25)$$

and

$$\begin{pmatrix} \bar{X}_1 \\ \bar{X}_2 \\ \bar{X}_3 \end{pmatrix} = \begin{pmatrix} \hat{X}_1 + \lambda_0 \mathrm{sing}_{\mathrm{moy},0}(X_1 - \hat{X}_1) \\ \hat{X}_2 + \lambda_1 \mathrm{sing}_{\mathrm{moy},1}(\bar{X}_2 - \hat{X}_2) \\ \hat{X}_3 + \lambda_2 \mathrm{sing}_{\mathrm{moy},2}(\bar{X}_3 - \hat{X}_3) \end{pmatrix} \quad (26)$$

The control input U is an input vector that includes the of synchronous generators excitation voltage and the controllable voltage of the rotor side converter and the control input related to SSSC. Details on how to apply inputs are given in Appendix A.

Fig. 3. The Diagram of the proposed terminal sliding mode controller alongside with the observer for the considered power system which includes both DFIG and SSSC.

VII. The proposed algorithm for stability improvement of the power system including the DFIG and SSSC

In the following flowchart, the general configuration for the power system under consideration, applying the terminal sliding mode control law plus a sliding mode observer, is presented.

VIII. Simulation results

To evaluate and validate the effectiveness and performance of the proposed observer-based controller laws on a power system, a simulation is carried out. The considered power system is the standard 39-Bus NEW ENGLAND network. This power system includes 10 synchronous machines, a DFIG component in Bus 19, and a SSSC one between 16, and 19 Buses. The system specifications are presented in Appendix B and a more complete description is offered in [32]:

All simulations are done in the MATLAB software environment. It is assumed that in the vicinity of G4 of the mentioned power system, a short-circuit fault occurred and lasted for 100 milliseconds. In the first stage, it is assumed that there is no control in the power system. The plot of speed deviation of the G4 generator and DFIG is depicted in Fig. 6-a. As it is observed from this plot, the power system is all unstable.

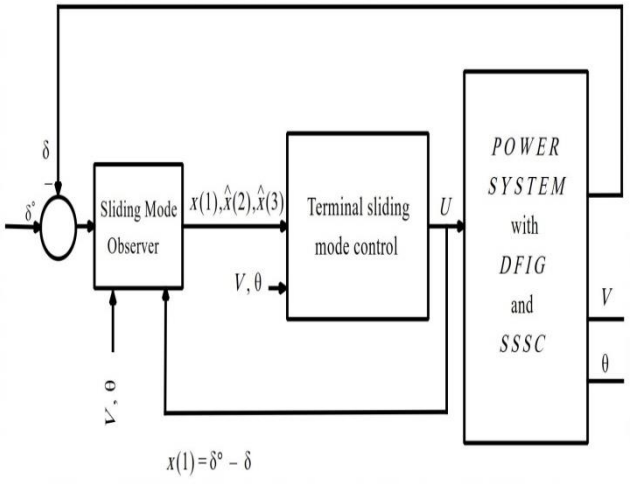


Fig. 3 depicts the schematic diagram of the systems' performance together with the applied proposed control law:

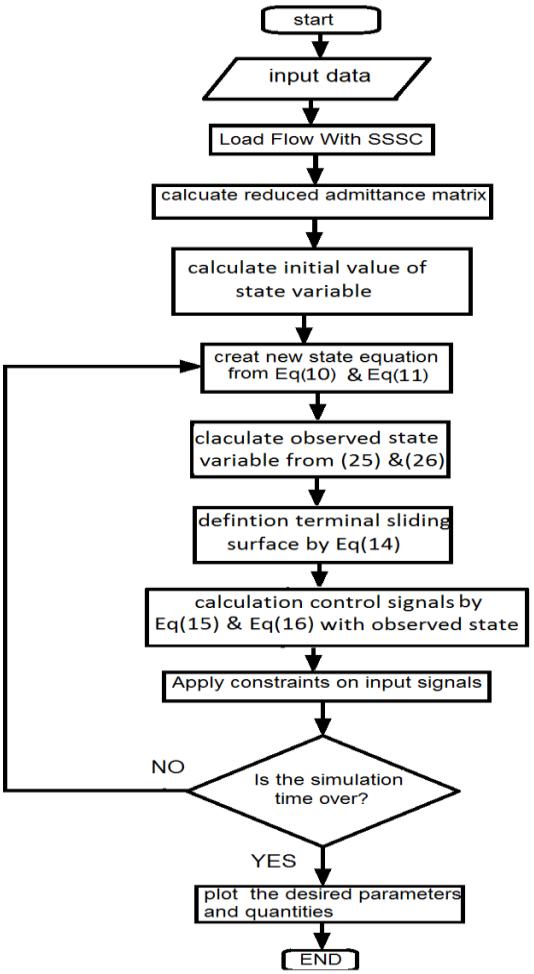


Fig. 4 The simulation flowchart of the power system including both DFIG and SSSC, applying terminal sliding mode control law and the sliding observer.

In Figure 6-a, the speed deviations are shown. In terms of speed change, this generator has the highest speed change compared to other system generators which is about [-5, 5] rad/sec at an angular speed of 377 rad/sec, and it can change the frequency to 0.9 Hz. Linear controllers certainly cannot be used to improve stability due to extreme changes in the operating point. In the second stage, DFIG control input, and synchronous generators are considered for stability improvements by the terminal sliding mode scheme.

All simulation is cariad out based on $a_2 = 0.5$ .In Figures 6-b and 6-c, the deviations in internal angle and speed of machines after the short-circuit fault are depicted. It is clear that all the machines plus DFIG are returned to their equilibrium conditions.

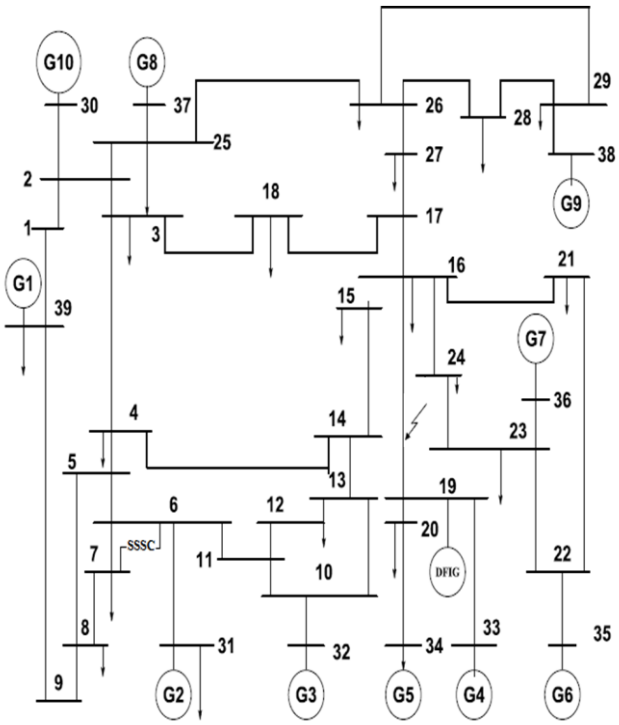


Fig. 5 The NEW ENGLAND standard 39-Bus power system which includes DFIG and SSSC.

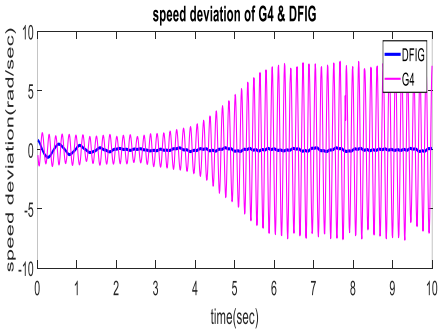


Fig. 6-a Speed deviation of G4 and DFIG without control.

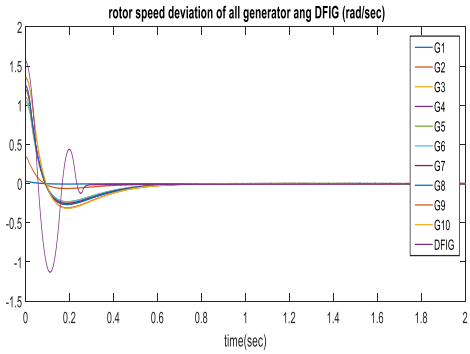


Fig. 6-b Rotor speed deviation of all generators and DFIG applying the proposed controller.

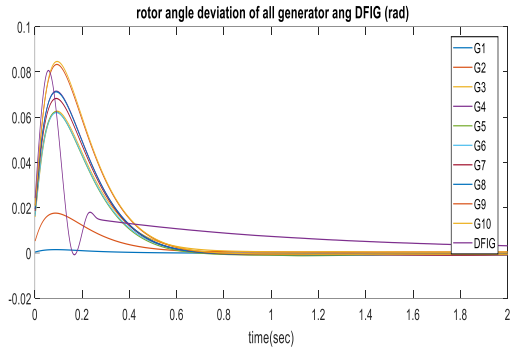


Fig. 6-c Rotor angle deviation of all generators and DFIG applying the proposed controller.

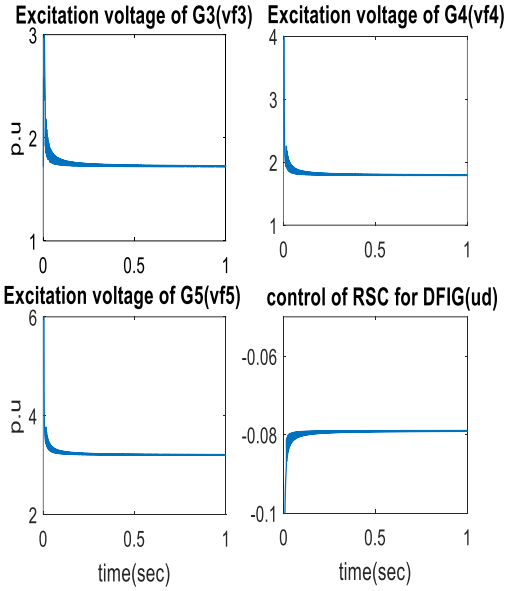


Fig. 7. Excitation voltage of G3, G4, G5, and RSC control of DFIG.

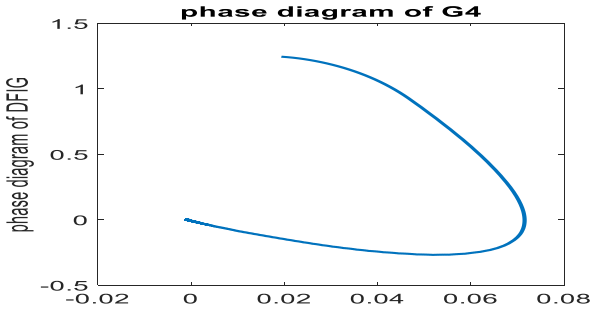


Fig. 8. The phase diagram of the G4 generator after removing the fault

In Figure (7), the excitation voltages of generators No. 3, No.4, No.5, and the control signal of DFIG are drawn due to their proximity to the fault location and greater effectiveness .For a better understanding of the phase diagrams G4 and DFIG after removing the fault are plotted in Figs. 8 and 9.

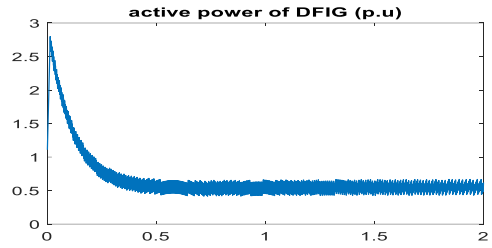


Fig. 10. Changes in the active power of DFIG after clearing the fault.

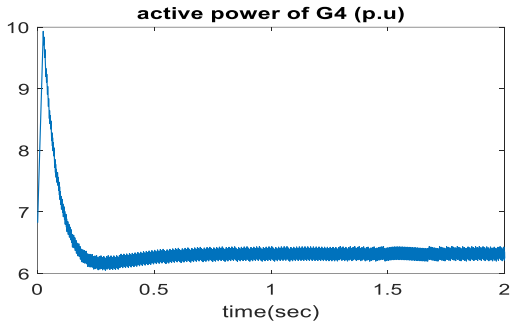


Fig. 11. Changes in the active power of the G4 generator after clearing the fault.

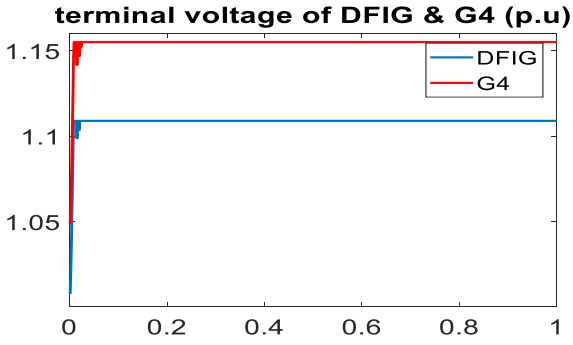


Fig. 12. Terminal voltages of G4 generator and DFIG after clearing the fault.

It is evident from the figures that the mentioned variables tend toward zero with an acceptable speed from their initial conditions after clearing the fault occurrence.

Fig. 10 and Fig. 11 depict the deviation of one of the important parameters of stability, that is, the changes in the active power for the G4 generator and DFIG. Due to the increase of the power angle during the fault, the power changes are instantaneous, and their duration is very short. After fault clearing, the controller should properly dampen these changes.

It is observed from the figures that the active powers converge to their reference values in 0.3 seconds after the fault. In Fig. 12, the plot of terminal voltages related to the G4 generator and DFIG are shown. This figure shows that the terminal voltages reach their initial values in a short duration of time after the fault occurrence.

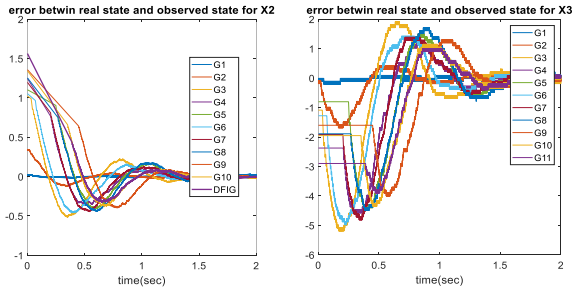


Fig. 13. The Error between the actual values and the observed values for X2 and X3 in all the generators and DFIG.

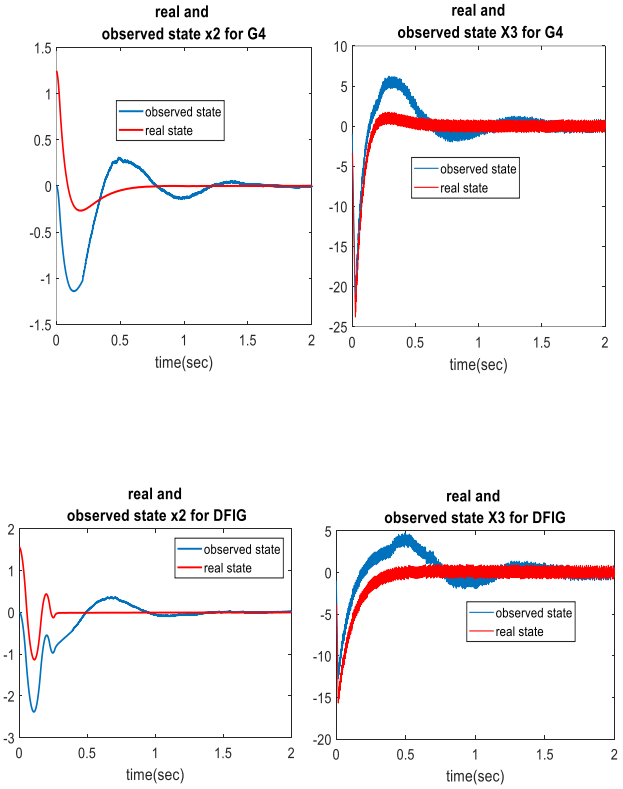


Fig. 14. A Comparison between the real state values with the observed ones for the G4 generator and DFIG.

To examine the performance of the sliding mode observer, the errors between the actual and the observed state variables x2 and x3 are plotted in Fig. 13.

The corresponding observer error reaches zero in about 2 seconds. In Fig. 14, a comparison is made between the actual states with their observed values for the G4 generator and DFIG. The figure shows that the DFIG state-variable tends to its actual value in a short duration of time.

In the following scenarios, the robustness of the designed control method against the sudden change of the mechanical power input of one of the generation units and the change of the fault location and the change of the wind speed, as the input of the DFIG have been investigated separately.

In Fig. 15, the performance of the G4 generator in the case of

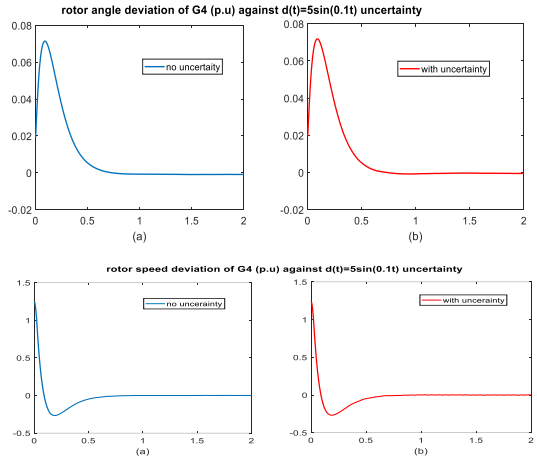


Fig. 15. A Comparison between the real state values with the observed Ones for the G4 generator and DFIG under the effect of noise.

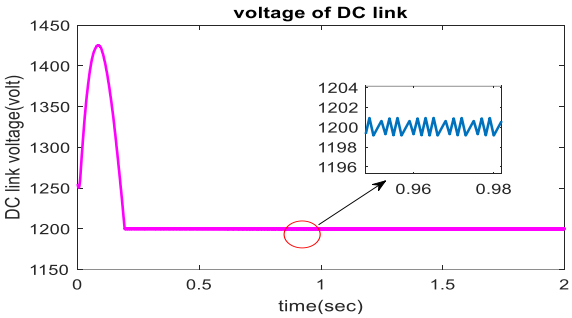


Fig. 16. Voltage of DC link in DFIG.

imposing uncertainty with the value of $d(t) = 10sin(.1t)$ to the power system is depicted. The plot shows that adding this uncertainty does not have a particularly important effect on the controller performance and the resulting output states. This fact demonstrates the robustness of the proposed control scheme, compared to the terminal sliding mode control law to structure uncertainty in the form of additional noises.

Figure (16) shows the voltage changes in the dc link of the grid-side converter. According to the figure, it can be seen that the controller designed for the grid-side converter has been able to adjust the voltage to the desired value of pre-fault.

To demonstrate the efficiency of the designed controller and its robustness to the location of the fault occurring, a short-circuit fault occurred for 100 milliseconds on bus No. 22 near generator No. 6. In Figure 17, the angular speed changes for generators No. 6 and No. 7, which are closer to the fault, are shown. According to these figures, both generators become stable after a short period of time and the controller has performed well against the fault.

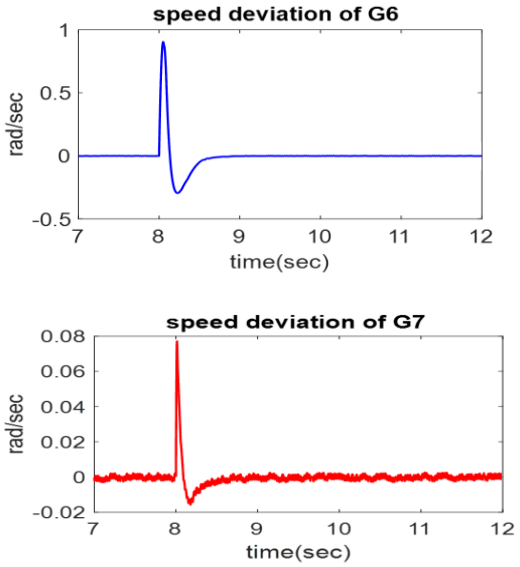


Fig. 17. Speed deviation of G6 and G7 against occurring fault at Bus No. 22.

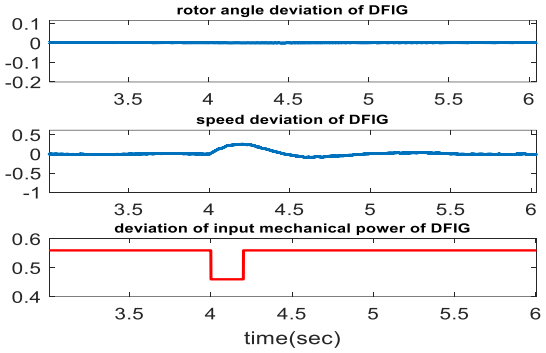


Fig. 18. Speed deviation and rotor angle deviation of DFIG against input mechanical power.

Also, considering that changes in wind speed cause changes in the input mechanical power to the DFIG generator, therefore, Figure 18 shows the changes in the angular speed and the internal voltage angle of the DFIG against a decrease in the input mechanical power by 17% in a period of 200 milliseconds. According to this figure, it can be seen that the controller performs well, the angular velocity changes are damped within 1.5 seconds and the DFIG becomes stable.

In order to further investigate, the performance of the proposed control law, with respect to the other important methods presented in the literature, a comparison is made with those in [11] and [16]. Table 2 shows the comparison in terms of overshoot, rise-time, and settling time resulting from the applied control law in the presented approach with the multi-input back-stepping method [16]. This table clearly shows the superiority of the proposed control law with respect to [16].

TABLE 2: A COMPARISON OF CONTROL CHARACTERISTICS BETWEEN THE PROPOSED APPROACH WITH [16].

	Proposed control law in this article			Nonlinear control design reported in [16]		
$G3$	Rise time (Sec.)	Settling time (Sec.)	Overshoot (p.u.)	Rise time (Sec.)	Settling time (Sec.)	Overshoot (p.u.)
Speed deviation	0.35	2.5	0.0015	0.5	5.0	0.005
Rotor angle	0.35	2.7	3˚	0.1	5.0	15˚
Control signal	0.50	2.2	0.5	0.4	7.5	3.2

TABLE 3: A COMPARISON OF CONTROL CHARACTERISTICS BETWEEN THE PROPOSED APPROACH WITH [11].

	Proposed control law in this article			Optimized linear control design reported in [11]		
$G4$	Rise time (Sec.)	Settling time (Sec.)	Overshoot (p.u.)	Rise time (Sec.)	Settling time (Sec.)	Overshoot (p.u.)
Speed deviation	0.28	2.3	0.0025	0.20	4.5	0.015
Rotor angle	0.30	2.5	5˚	0.15	4.0	25˚
Control signal	0.04	2.1	1.25	–	–	–

Table 3 demonstrates the results obtained by applying the proposed control law in this paper in comparison with the offered linear method in Ref. [11]. This table also shows the improvement in the stability characteristics with respect to the results of Ref. [11].

IX. Conclusion

In this study, a nonlinear control law based on the theory of terminal sliding modes is developed for power systems that include DFIG and SSSC. The main contribution of the paper is to enhance power system stability and to design a controller to achieve a robust closed-loop performance. A sliding mode observer is also designed to provide information on inaccessible state variables.

In the simulation results section, the 39-bus power system including DFIG and SSSC was considered, which becomes unstable by taking into account the mentioned disturbance and no controller. In the next step the system is stabilized by applying the sliding non-linear controller. The changes in the excitation field voltage of the generators and the changes in the DC link of the DFIG were shown considering the limitations on the inputs. In the next step, the effectiveness of the observer in estimating states and their convergence in the minimum possible time was shown. Next, the robustness of the designed control method against the sudden change in mechanical change of one of the generators and the changing fault location and the change of the wind speed as the input of the DFIG was investigated separately and the effectiveness of the proposed control approach was shown. In the end, this method was compared with the linear controller and the non-linear back-stepping controller, based on some control criteria that are given in Tables 2 and 3, which indicate the superiority of the proposed controller over other methods.

For instance, according to the simulation results, in Table 3, the overshot level is decreased by 40% and the settling time is decreased by 15% compared to the existing nonlinear control laws.

Appendix A:

The injected model of SSSC:

In order to model SSSC in the power system, it is assumed that SSSC is located between bus *i* and bus *j* as shown in Fig. A1. The proposed model of the SSSC is a series converter. This converter can stabilize the voltage of the power system buses and improve dynamic stability by injecting reactive power into the series branch [33].

The main goal of SSSC control approach aims to improve dynamic stability by injecting the appropriate series voltage, i.e. V_{se}. Hence, this controllable voltage of the converter can be represented by Fig. A.2.

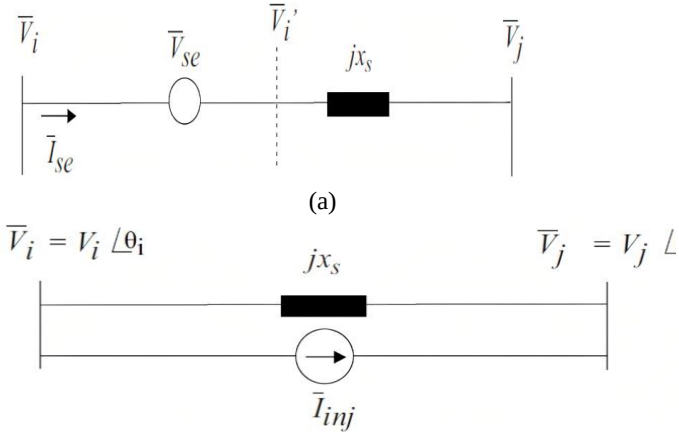


Fig. A.1. a) simplified model of SSSC, between bus *i* and bus *j*, b) equivalent circuit of SSSC.

$$\begin{cases} \dot{\delta}_i = \dfrac{1}{E_i' T_{oi}'}[\acute{T}_{oi}(\omega_i - \omega_s)E_i' - \\ \dfrac{X_i - X_i'}{X_i'} V_i \sin(\delta_i - \theta_i) + T_{oi}'\omega_s V_{ri} \cos(\delta_i - \varphi_{ri})] \\ \dot{\omega}_i = \dfrac{1}{M_i}[P_{mi}\dfrac{\omega_s}{\omega_i} - \dfrac{E_i' V_i^2 \sin(\delta_i - \theta_i)}{X_i'}] \\ \dot{E}_i' = \dfrac{1}{T_{oi}'}[\dfrac{X_i}{X_i'}E_i' - \dfrac{X_i - X_i'}{X_i'} V_i \cos(\delta_i - \theta_i)) \\ \quad + T_{oi}'\omega_s V_{ri} \sin(\delta_i - \varphi_{ri})] \end{cases} \quad \text{(A-1)}$$

where, V and θ are the amplitude and phase angle of the bus voltages, respectively. X_i' is the seires reactance of the system between the i-th DFIG and the bus connected to it. E_i' is the internal voltage of the i-th generator, and V_{ri} and Φ_{ri} are the amplitude and angle of the voltage applied to the DFIG rotor in polar coordinates, respectively.

From Fig.A.1 obtained:

$$\begin{cases} \bar{I}_{inj} = -jB_{ij}V_{se} \\ v_{se} = V_{se}e^{j\Phi_{se}} \\ B_{ij} = \dfrac{1}{x_{sij}} \end{cases} \quad \text{(A-2)}$$

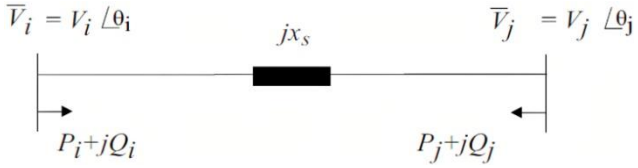


Fig. A.2. Alternative equivalent injected model of SSSC in power system.

In Fig. A.2, P_{si}, P_{sj}, Q_{si}, and Q_{sj} are defined between bus *i-th* and bus *j-th* as follows:

$$\begin{cases} S_{si} = P_{si} + jQ_{si} = -B_{ij}V_{sek}V_i \sin(\theta_i - \Phi_{sek}) \\ \quad +\mathrm{j}B_{ij}V_{sek}V_i \cos(\theta_i - \Phi_{sek}) \\ S_{sj} = P_{sj} + jQ_{sj} = B_{ij}V_{sek}V_j \sin(\theta_j - \Phi_{sek}) \\ \quad -jB_{ij}V_{sek}V_j \cos(\theta_j - \Phi_{sek}) \end{cases} \quad \text{(A-3)}$$

Here it is assumed that the SSSC component only generates and consumes reactive powerand also the series resistance of the transmission line on which the SSSC is located equals zero. Hence, the SSSC voltage angle is determined as follows:

$$\Phi_{sek} = tan^{-1}\left(\frac{V_j \sin(\theta_j) - V_i \sin(\theta_i)}{-V_j \cos(\theta_j) + V_i \cos(\theta_i)}\right) \quad \text{(A-4)}$$

Modeling of DFIG used in wind energy production

Fig. 1-b demonstrates the schematic diagram of a wind generator equipped with DFIG. the equivalent with the definition of $u_{df2i} = V_{ri}sin(\Phi_{ri})$ and $u_{df1i} = V_{ri}cos(\Phi_{ri})$ after the state-space equations can be rewritten as in Eq. (A.5).

$$\begin{cases} \dot{\delta}_i = (\omega_i - \omega_s) - \dfrac{X_i - X_i'}{E_i' T_{0i} X_i'} V sin(\delta_i - \theta_i) \\ \quad + \dfrac{\omega_s}{E_i'}(u_{df1i}cos(\delta_i) + u_{df2i}sin(\delta_i))] \\ \dot{\omega}_i = \dfrac{\omega_s}{2H_i}\left[P_{mi}\dfrac{\omega_s}{\omega_i} - \dfrac{E_i' V_i \sin(\delta_i - \theta_i)}{X_i'}\right] \\ \dot{\acute{E}}_i = \dfrac{1}{T_{oi}'}[-\dfrac{X_i}{\acute{X}_i}E_i' + \dfrac{X_i - X_i'}{X_i'} V_i \cos(\delta_i - \theta_i)) \\ \quad + T_{oi}'\omega_s(u_{d2i}sin(\delta_i) - u_{d1i}cos(\delta_i))] \end{cases} \quad \text{(A-5)}$$

Here, design principle is baed on using one of the inputs related to the rotor control in order to attain a strict feedback form.

$$(\omega_i - \omega_s) - \frac{X_i - X_i'}{X_i' E_i' T_{0i}} V sin(\delta_i - \theta_i) + \frac{\omega_s}{E_i'}(u_{df1i}cos(\delta_i) + u_{df2i}sin(\delta_i)) = (\omega_i - \omega_{0i})$$

$$u_{d2i} = \frac{E_i'(\omega_s - \omega_{0i})}{\omega_s \sin(\delta_i)} + \frac{X_i - X_i'}{T_{oi}'\acute{\omega}_s X_i' \sin(\delta_i)} V_i \sin(\delta_i - \theta_i) - \frac{E_i' cos(\delta_i)}{sin(\delta_i)}\ u_{d1i} \quad \text{(A.6)}$$

where ω_{0i} is the speed rotation of the DFIG generator in the steady state. Substituting u_{df2i} in Eq. (A. 5):

By replacing u_{d2i} and defining $u_{d1i} = u_{di}$, it is finally obtained:

$$\begin{cases} \dot{\delta}_i = \frac{1}{\acute{E}_i T_{0i}}[-T_{0i}(\omega_i - \omega_0)\acute{E}_i - \frac{X_i - \acute{X}_\iota}{\acute{E}_{qi} T_{0i}} V_i sin(\delta_i - \theta_i) + T_{0i}\omega_0 u_{di} cos(\delta_i)] \\ \dot{\omega}_i = \frac{\omega_0}{2H_i}\left[P_{mi}\frac{\omega_s}{\omega_i} - B_i \acute{E}_i V_i \sin(\delta_i - \theta_i)\right] \\ \dot{\acute{E}}_i = \frac{1}{T_{0i}}\left[-\frac{X_i}{\acute{X}_\iota}\acute{E}_i + \frac{X_i - \acute{X}_\iota}{\acute{X}_\iota} V_i \cos(\delta_i - \theta_i) + T_{0i}\omega_0 u_{di}\sin(\delta_i)\right] \end{cases} \quad \text{(A.7)}$$

The dynamics of DC link capacitor:

By suitably controlling the grid-side converter, it is possible to control the amount of DC link voltage ripple and the amount of output reactive power. The following relationship can be used to obtain the dynamics of the capacitor voltage [31]:

$$C_{dc} V_{dc} \frac{dV_{dc}}{dt} = [P_r - P_g] \quad \text{(A.8)}$$

Considering the output voltage of the grid-side converter in polar coordinates as $V_g \angle \Phi_g$, the output power from the grid-side converter to the generator terminal is obtained as follows:

$$P_g = \frac{V_g V_i}{x_g}\sin(\Phi_g - \theta_i) \quad \text{(A.9)}$$

$$Q_g = \frac{V_g{}^2}{x_g} - \frac{V_g V_i}{x_g}\cos(\Phi_g - \theta_i) \quad \text{(A.10)}$$

$$u_{g1} = V_g \cos(\Phi_g), u_{g2} = V_g \sin(\Phi_g) \quad \text{(A.11)}$$

$$V_g = \sqrt{u_{g1}{}^2 + u_{g2}{}^2}, \Phi_g = \text{atan}\left(\frac{u_{g2}}{u_{g1}}\right) \quad \text{(A.12)}$$

a result, the voltage dynamics of the DC link capacitor is obtained as follows:

$$\dot{V}_{dc} = \frac{1}{C_{dc} V_{dc}}\left[P_r - \frac{1}{x_g}(u_{g2} cos(\theta_i) - u_{g1} sin(\theta_i)\right] \quad (A.13)$$

Appendix B:

The specification of considered NEW ENGLAND 39-bus power system is presented here.

TABLE 4: EQUIVALENT SPECIFICATIONS OF WIND-TURBINE-BASED DFIG.

X_d	X_d'	X_q	H
2.605	0.107	0.0107	4

TABLE 5: EQUIVALENT SPECIFICATIONS OF SYNCHRONOUS GENERATORS.

No	H	Ra	$x'd$	xd	xq	$T'do$	xl
1	5.0	0	0.006	0.020	0.019	7.00	0.030
2	30.(	0	0.0697	0.295	0.282	6.56	0.035
3	35.8	0	0.0531	0.2495	0.237	5.70	0.0304
4	28.(	0	0.0526	0.166	0.670	0.62	0.440
5	26.(	0	0.132	0.670	0.620	5.40	0.054
6	34.8	0	0.050	0.254	0.241	7.30	0.0224
7	26.4	0	0.049	0.295	0.292	5.66	0.0322
8	24.3	0	0.057	0.290	0.280	6.70	0.028
9	34.5	0	0.057	0.2106	0.205	4.79	0.0298
10	42.(	0	0.031	0.100	0.069	10.2	0.0125

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Optimized Algorithm for Open-Circuit Fault Detection in Switches and Capacitor Voltage Balancing Control in Modular Multilevel Converters

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ABSTRACT

The modular multilevel converter (MMC) is a favored topology in the industry, but its reliability is at risk with an increase in the number of sub-modules (SMs) due to a rise in switching components. The essential need for maintaining capacitor voltage balance in each arm leads to increased complexity and cost, as numerous voltage sensors are required. This study introduces an innovative approach to minimize the number of voltage sensors by employing an enhanced algorithm for open-circuit fault detection in switches. The proposed scheme organizes each arm into groups, each containing two SMs and one voltage sensor, aiming to reduce the overall sensor count. A novel fault detection mechanism is presented, identifying open-circuit faults by comparing group output voltages in healthy and defective conditions. The capacitor voltage estimation algorithm in the sensor reduction scheme is noted for its simplicity compared to other methods. The effectiveness of these methods is validated through simulations and experimental implementations across diverse scenarios, affirming their reliability.

I. Introduction

Recently, the modular multilevel converter (MMC) has been used frequently for its various advantages [1], [2], [3]. These include fully modular design, easy construction, excellent output waveform quality, and fault tolerance in high and medium power applications [4], [5]. In the range of medium and high power applications, MMC with over 200 sub-modules (SMs) has been used in each arm [6], [7]. As the number of SMs increases, the converter's reliability reduces due to the use of numerous semiconductor switches [8], [9]. One of the most vulnerable components of power electronic converters is semiconductor switches [10], [11]. Typically, open-circuit and short-circuit failures on semiconductor switches are the two most common types of faults. [12], [13].

Short-circuit faults are extremely damaging and immediately cause numerous obstructions to the system [14]. Therefore, short-circuit faults must be identified quickly, and the identification process typically uses hardware methods [12]. On the other hand, open-circuit faults are not dangerous for the system immediately after the occurrence [15]. If such a fault occurs, it will not be detected in the system for an extended period. In such a case, the output voltage and current of the converter will be disturbed [16]. Also, if the open-circuit fault detection time is long, it will be destructive for other parts of the converter or even for the whole system [17], [18]. Therefore, fast and accurate detection of an open-circuit fault in MMC is necessary. For this reason, several studies have been done on detecting the open-circuit fault in MMC.

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TABLE I. COMPARISON OF FAULT DETECTION METHODS

Item	***Reference***													
	[19]	***[20]***	***[21]***	***[22]***	***[23]***	***[24]***	***[25]***	***[26]***	***[27]***	***[28]***	***[29]***	**[30]**	**[31]**	***[Proposed]***
Detection	Yes		Yes			No					Yes			No
Localization			NO	Yes										
Detection time	25 µs	----	100ms	10ms	< 20 ms	----					200 µs	---		
Localization time	85 ms	5 ms	----	120 ms		300µs	150 ms	300 µs		----	200 µs	---	0.33ms	<20 ms
No. arm voltage sensors	N	N+3	N								N+1	N		N/2
No. arm current sensors	1									0	1			
cost	Medium	High	Medium											Low
Computation burden	Low	High			Medium	Low	Medium	Low		Medium	High		Very high	Low

TABLE II. COMPARISON OF SENSOR REDUCTION METHODS

Item	***Reference***									
	[35]	***[36]***	***[37]***	***[38]***	***[39]***	***[40]***	***[41]***	***[42]***	***[43]***	***[Proposed]***
No. arm voltage sensors	N			1				N/2	Number of groups	N/2
No. arm current sensors	0			1						
Fault detection	NO								Yes	
correction factor	NO				Yes					NO
Computation burden	Medium	Low		Medium	Very high			Very low	High	Low

In [20], [21], hardware-based methods are used to detect open-circuit faults. These methods are simple, but increasing the number of SMs requires additional types of equipment, which causes hardware complexity and cost increment. Recently, software-based methods have been developed to detect defective switches in MMC [21]-[31]. A sliding mode observer is used in [19] to estimate the arm current in order to identify the open-circuit fault. The defective SM is then located by the assumption-verification method. In this method, the detection time is long, and many sensors are used. In addition, the defective switch is not detectable. In [22], the Kalman filter (KF) observer estimates the circulating current and detects the open-circuit fault in the SMs. When a fault occurs in the SM switches, there will be a discrepancy between the measured and estimated values of the circulating current. In this way, The SM fault is detected by exceeding the discrepancy value from the specified threshold. The disadvantages of this method include the intricacy of the estimation algorithm, the large number of sensors, the long detection time, and inefficiency in the case of several faults. Using the MMC state-space equations and the Luenberger observer, a method for identifying a defective switch of MMC is proposed in [23]. The time required to detect fault is relatively long, and in the several faults, the proposed method cannot detect defective switches. A fast fault detection method is presented in [24] to increase the reliability of the MMC. In this method, the voltage sensors are installed parallel with the SMs upper switch, and an indicator based on Boolean logic operations is designed to identify defective switches quickly. However, the method's use of several voltage sensors, which raises system costs, is a negative characteristic. Based on capacitor voltage increases, [25] presents a method for locating faults in lower switches of SM. However, there is no solution for fault detection in upper switches. In contrast to the two-step fault detection methods [19], [22], [23], a quick method for locating defective switches is presented in [26], [27] by relocating the location of the voltage sensors of the SMs. Although fast fault detection is possible, this system is expensive and complex due to the use of a large number of voltage sensors. The idea of fault detection is used in [26], [27] in reference [28] without using arm current sensors. However, many voltage sensors are still used in the MMC. Furthermore, the removal of current sensors will

complicate the converter's control of circulating current. A new multiple open-circuit fault detection method is presented in [29], which uses the error between the measured and expected arm voltages for fault detection. The location algorithm is based on assumption-verification, which increases the computation burden to locate the defective switch in MMCs with a large number of SMs. A fault detection method based on double clamp SM (DCSM) is proposed in [30] using the higher order Bayes model (HONBM). However, in industrial applications, half-bridge SMs are mostly used, and the response of the fault detection method in half-bridge SMs is unknown. Using the Entropy of Wavelet Packets (EWP), [31] presents a fault detection method for three-level MMC, the proposed method can detect open circuit faults at high speed. However, as the number of levels increases, the calculation load increases and the detection speed decreases. Table I provides a comprehensive comparison of fault detection methods. As is well known, fault detection methods have several limitations, which are as follows: (a) The speed of detecting and locating the faulty switch is long in most methods. (b) Some methods are complicated and associated with the increased computational burden. (c) Most methods employ a large number of voltage sensors and additional components, which raises the MMC's cost.

In addition to the open-circuit fault in the switches, controlling the voltage balance of the capacitors in the MMC is regarded as a major challenge [32], [33]. The presence of a large number of capacitors in the MMC structure necessitates the use of capacitor voltage balance control methods in this converter, which has resulted in the use of a large number of voltage and current sensors in conventional control methods [34]. Recently, the idea of lowering the number of sensors in MMC has been the subject of extensive research. The comparison of sensor reduction methods is shown in Table II. The removal of arm current sensors was proposed in [35], [36], [37]. However, the removal of these sensors challenges the control of circulating current and fault detection methods. In [38], the voltage of the capacitors is estimated using one voltage sensor in each arm. This method uses the discrepancy among the measured and estimated arm voltages to estimate the capacitor voltages, but capacitor voltage estimation of MMC in high voltage applications is a challenging issue that is not considered.

In [39], [40], [41], several algorithms with correction factor capabilities, such as the adaptive linear neuron, the exponentially weighted recursive least square (ERLS), and the KF, are used to estimate capacitor voltages. These approaches require two voltage sensors in each phase branch to complete the estimate procedure. In these methods, the computational burden increases significantly as the number of SMs increases. Also, high-voltage sensors are required. In addition, on the occasion of an open-circuit fault of the switches, the voltage estimation of the capacitors will be affected, and identifying a defective switch will be challenging.

In [42], a solution to reduce the computational burden is presented using a new topology based on the half-bridge (HB) SM in which high voltage sensors are removed. Each SM consists of two HBs, but solely one voltage sensor is employed among the positive poles of the two capacitors. However, despite decreasing the number of voltage sensors and computational burden, the presented topology does not offer a solution for detecting open-circuit faults. In [43], a new method for group measurement of capacitors voltage is proposed to reduce the number of voltage sensors and detect the switches' open-circuit faults. In the proposed method, the KF algorithm is used to estimate the voltage of the capacitors, which complicates the estimation process. Also, the fault detection method uses assumption-verification, which executes it difficult to apply this method in practical applications.

This paper provides approaches for estimating capacitor voltages with fewer voltage sensors and detecting open-circuit faults in SMs. The capacitor voltages estimation method divides SMs into groups of two SMs and a voltage sensor. Consequently, the number of voltage sensors is reduced by half compared to conventional MMC measurement methods. Furthermore, the proposed estimation method is more straightforward than earlier studies and speeds up the computing process. Also, an open-circuit fault detection method based on monitoring the output voltage of the SM groups is presented to detect defective switches. The proposed method can detect an open-circuit fault in switches in less than one cycle, significantly faster than existing fault detection methods. Based on the simulation and experimental results of using the proposed fault detection method, all SM states can be monitored simultaneously, and all defective switches in different SMs can be detected.

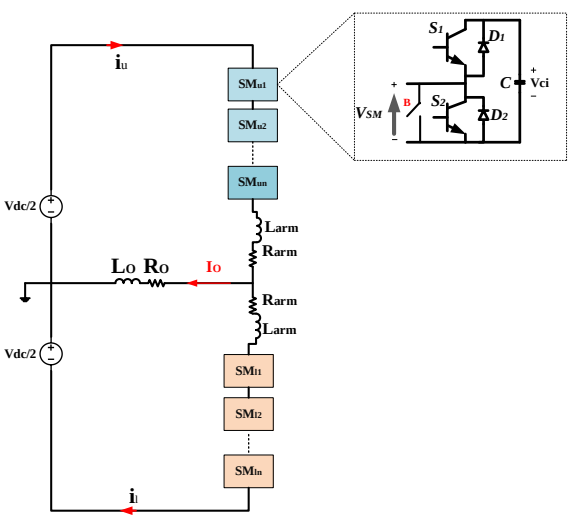

Fig. 1. MMC configuration

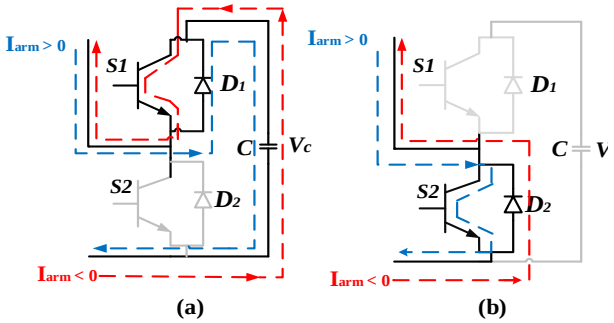

Fig. 2. Arm current paths in different switching of SM, (a) switching $S_1 = 1$, (b) switching $S_1 = 0$

TABLE III. THE SM BEHAVIOR UNDER DIFFERENT PERFORMANCE

state	I_{arm}	Capacitor behavior of the submodule		
		normal	S_1 fault	S_2 fault
S_1=1	< 0	Discharge	Bypass	Discharge
	>0	Charge	Charge	Charge
S_1=0	< 0	Bypass	Bypass	Bypass
	> 0	Bypass	Bypass	Charge

II. Topology and Normal Operation of MMC

In Fig. 1, the schematic representation of the Modular Multilevel Converter (MMC) configuration is depicted. This configuration comprises N series-connected Sub-Modules (SMs) and an inductor (L_{arm}) forming both the upper and lower arms of each phase. To model losses within the arms, a resistor (R_{arm}) is employed. Conventionally, the MMC adopts a half-bridge SM topology, characterized by two complementary Insulated Gate Bipolar Transistor (IGBT) switches, one capacitor, and two anti-parallel diodes. Additionally, a bypass switch (B) is typically integrated into the SM's output to facilitate the short-circuiting of malfunctioning SMs. In the standard SM operation mode, the arm's current paths are shown in Fig. 2. There are four different paths for arm current depending on the SM switching situation. Fig. 2 (a) shows the current paths at $S_1 = 1$ (1 stands for the on-state of a switch). In this case, if $I_{arm}>0$, the capacitor is charged, and if $I_{arm}<0$, the capacitor is discharged. The output voltage of SM is the same as the capacitor's voltage (V_c). The current paths at $S_1= 0$ (0 stands for the off-state of a switch) are shown in Fig. 2 (b). In this case, the SM is bypassed, the current sign does not affect the capacitor, and the output voltage of SM is zero.

III. Operation of SM With Open-Circuit Fault

In the topology of the half-bridge SM, two switches are employed so that there is a possibility of two classes of open-circuit faults in one SM, i.e., a fault on the upper switch (S_1) and a fault on the lower switch (S_2). The state of SM under different operating conditions is given in Table III. In the case of a fault in S_1, if $I_{arm}<0$ and $S_1 = 1$, the arm current will be forced to pass D_2 instead of S_1. In other cases, the SM behavior will be the same as normal operation. In this way, the capacitor will not have a chance to discharge, and the voltage of the defective SM capacitor will always be higher than other SMs. In the occurrence of the fault in S_2, when $I_{arm} > 0$ and $S_1 = 0$, the arm current will pass through D_1 instead of S_2. Therefore, in an S_2 fault, the capacitor charging time will be longer than the discharge. In other cases, the flow path is similar to the normal operation of the SM. In this way, the voltage of the defective SM capacitor is higher than the other SMs in both fault modes. According to Table I, the fault detection in S_1 and S_2 is not simultaneous and requires the specified conditions to be met.

IV. Sensor Configuration and Proposed Fault Detection Method

A. Configuration of Voltage Sensors and Group Measurement of Capacitor Voltages

For normal MMC operation, it is critical to sustaining the SM capacitors' voltage balance. Achieving this goal requires instantaneous information about the capacitor voltages. Hence, the existence of many voltage sensors is mandatory for balancing the capacitor voltages in usual control methods. As a result, the system's intricacy and expense will rise as the number of measuring components increases. In this study, a new scheme for group measurement of the capacitor voltages is proposed to reduce the voltage sensors. The proposed scheme's configuration of voltage sensors is depicted in Fig. 3(a), where each arm is divided into groups consisting of two SMs. Individual sensors are eliminated from the capacitors, and one voltage sensor is installed at the output of each group as the group monitoring sensor. Each group's capacitor voltages are estimated using the group monitoring sensor for the capacitors voltage balancing. Also, by comparing monitoring sensor values across consecutive sampling times, the open-circuit defect can be detected. Fig. 3 (b) displays the *ith* (i = 1, 2, …, N/2) group in the MMC, which is comprised of two HBs (HB_{i1} and HB_{i2}) connected in series. The HB_{ij} (j = 1, 2) consists of one capacitor (C_{ij}) and two switches (S_{uij}, S_{lij}), and the switches gate signal is controlled by the switching function S_{ij}.

The basic equations for implementing the group measurement method with fewer voltage sensors are mentioned in (1) to (6). The mathematical model of the proposed estimation method is created using simple equations based on switching signals and capacitors voltage. In this way, the value of the monitoring sensor in each group is as follows:

$$V_{G_{u,l}i} = V_{HB_{i1}} + V_{HB_{i2}} \quad (1)$$

where $V_{Gu,li}$ is the voltage of the group, V_{HBij} is the voltage of HB_{ij}. The group estimated voltage $\hat{V}_{G_{u,l}(i)}$ equals the summation of HB_{ij} estimated

voltages. The voltage of each HB_{ij} can be written based on the estimated capacitor voltage of each SM ($\hat{V}_{Cij}$) and its switching state (S_{ij}). Hence, the output voltage of each group can be written as:

$$\hat{V}_{G_{u,l(i)}} = S_{i1}\hat{V}_{ci1} + S_{i2}\hat{V}_{ci2} \quad (2)$$

By rewriting (2) based on discrete sampling time, all variables have been changed based on time step x as follows:

$$\hat{\mathrm{V}}_{\mathrm{G_{u,l(i)}}}(\mathrm{x}) = \mathrm{S_{i1}}(\mathrm{x})\hat{\mathrm{V}}_{\mathrm{ci1}}(\mathrm{x}) + \mathrm{S_{i2}}(\mathrm{x})\hat{\mathrm{V}}_{\mathrm{ci2}}(\mathrm{x}) \quad (3)$$

Estimating capacitor voltages in each sample time requires the estimated group voltage discrepancy. The group voltage discrepancy in step *k* is calculated using the estimated capacitor voltages of step *k-1*, which have been stored in an algorithm memory, and the measured value of the monitoring voltage sensor in step *k*:

$$\widehat{\Delta V}_{G_{u,l(i)}}(k) = V_{G_{u,l(i)}}(k) - \sum_{j=1}^{2} S_{ij}(k-1)\hat{V}_{cij}(k-1) \quad (4)$$

The voltage of the capacitors used in a group voltage construction has been changed by flowing current through them. The new voltage of each capacitor in a group $(\hat{V}_{ci1}(k), \hat{V}_{ci2}(k))$ is estimated by dividing the group voltage variation $(\widehat{\Delta V}_{G_{u,l(i)}}(k))$ between the capacitor voltages of the last step $(\hat{V}_{ci1}(k-1), \hat{V}_{ci2}(k-1))$. Hence, the capacitor voltages in step k are estimated as follows:

$$\hat{\mathrm{V}}_{\mathrm{ci1}}(\mathrm{k}) = \hat{\mathrm{V}}_{\mathrm{ci1}}(\mathrm{k\text{-}1}) + \left[\frac{\mathrm{S_{i1}(k\text{-}1)}}{\mathrm{S_{i1}(k\text{-}1)+S_{i2}(k\text{-}1)}}\right]\widehat{\Delta \mathrm{V}}_{\mathrm{G_{u,l(i)}}}(\mathrm{k}) \quad (5)$$

$$\hat{\mathrm{V}}_{\mathrm{ci2}}(\mathrm{k}) = \hat{\mathrm{V}}_{\mathrm{ci2}}(\mathrm{k\text{-}1}) + \left[\frac{\mathrm{S_{i2}(k\text{-}1)}}{\mathrm{S_{i1}(k\text{-}1)+S_{i2}(k\text{-}1)}}\right]\widehat{\Delta \mathrm{V}}_{\mathrm{G_{u,l(i)}}}(\mathrm{k}) \quad (6)$$

Therefore, using (5) and (6), the present voltage of both capacitors in a group is estimated by the latter sample time (*k-1*) capacitor voltages and switching signals. In the estimation process, two essential features help the stability of the system and control the estimation error as follows:

Feature 1: One SM activation in the groups (HB_{i1}=0 & HB_{i2}=1 or HB_{i1}=1 & HB_{i2}=0)

When the modulator sends the command to produce one voltage level in each group, just one capacitor cooperates in the voltage generation. In this operation, the monitoring voltage sensor measures the capacitor voltage directly, which is exactly the same as the estimated value. Therefore, the estimation error in each cycle converges to zero, and the cumulative error will be eliminated.

When the capacitor estimated voltages depart from the standard range, the sorting process tries to bring them back within the acceptable sorting range and minimize the deviation between the estimated and measured voltages. In the case of incremental estimation error, when the capacitor's estimated voltage is greater than the measured value, the capacitor only participates in the switching process with the negative arm current. In this case, the capacitor voltage decreases and nears the measured value. In the decreasing estimation error, when the estimated voltage of one capacitor is lower than the measured value, the capacitor only participates in the switching process with the positive arm current, and its voltage is raised. Therefore, the capacitor voltages will be balanced and never exceed the standard range using the sorting process.

Feature 2: Balancing of estimated voltages with the sorting process

As a result, the estimation procedure is done with the straightforward process of dividing the voltage difference equally among the capacitors participating in a switching operation. Additionally, with the two features mentioned above, the estimation error in each sampling time is converged to zero, and capacitor voltage balancing is done with fewer voltage sensors.

B. Proposed Fault Detection Method

This section identifies the defective switch in MMC using an optimized fault detection process with reduced voltage sensors. According to Fig. 3 (b), the MMC arms are divided into several groups consisting of two SMs with the proposed sensor reduction scheme. The proposed fault detection algorithm constantly searches for the defective switches in each group. The fault detection process is Considering the arm's current sign (I_{arm}), the voltage accomplished by comparing the group voltage ($V_{Gu,l}i$) in normal and faulty operation modes. According to the information in Table III, finding the fault in the special switch depends on the activation of one SM in the group. In this case, the group monitoring sensor measures the capacitor voltage of the active SM. When a fault occurs in a switch, there is a difference between the measured and predicted voltage, and the defective switch can be detectable.

Fig. 4 shows the algorithm flowchart, where the algorithm starts by activating one SM in the group. measured by the group monitoring sensor is compared with one of the voltage thresholds (V_{thmin}, V_{thmax}). In the proposed algorithm, the lower (V_{thmin}) and upper (V_{thmax}) equal $\frac{1}{2}V_{ref}$ and $\frac{3}{2}$Vref, and V_{ref} is the capacitor balancing voltages ($\frac{V_{dc}}{N}$). According to different states in Table IV, if the $V_{Gu,l}$(i) exceeds the threshold values, the fault can be detected in different switches. Moreover, the fault counter (n_{iz}, z=1,2,3,4) has been prepared in the algorithm to prevent the detected faults caused by measuring noise. If the fault is

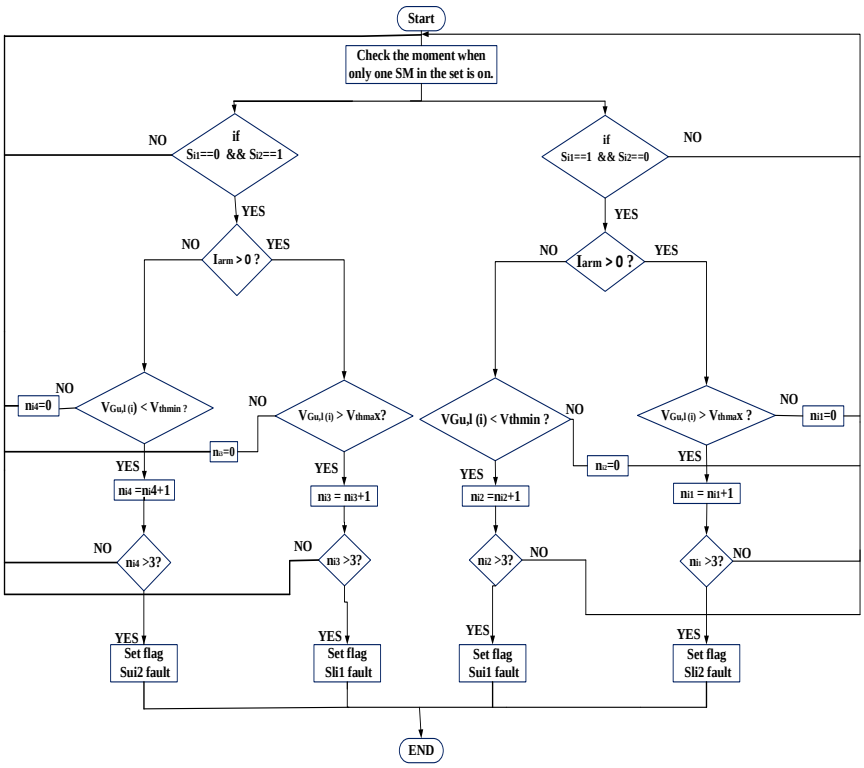

Fig. 4. Flowchart of the proposed fault detection method.

TABLE IV. EFFECT OF SWITCH FAULT ON GROUP OUTPUT VOLTAGE IN DIFFERENT SWITCHING STATES

status			$V_{Gu,l}\,i$				
S_{i1}	S_{i2}	I_{arm}	*Normal state*	*Open-circuit fault*			
				S_{ui1}	S_{li1}	S_{ui2}	S_{li2}
1	1	>0	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$
		<0	$V_{ci1}+V_{ci2}$	V_{ci2}	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$
1	0	>0	V_{ci1}	V_{ci1}	V_{ci1}	V_{ci1}	$V_{ci1}+V_{ci2}$
		<0	V_{ci1}	0	V_{ci1}	V_{ci1}	V_{ci1}
0	1	>0	V_{ci2}	V_{ci2}	$V_{ci1}+V_{ci2}$	V_{ci2}	V_{ci2}
		<0	V_{ci2}	V_{ci2}	V_{ci2}	0	V_{ci2}
0	0	>0	0	0	V_{ci1}	0	V_{ci2}
		<0	0	0	0	0	0

repeated three times, the counter approves the open-circuit fault in the system. The proposed method is implemented identically for all groups, and the algorithm can quickly detect several faulty switches while the number of voltage sensors has been significantly decreased.

V. SIMULATION STUDIES

To assess the viability of the proposed design, a single-phase MMC featuring 14 SMs in each arm is simulated in the MATLAB/Simulink environment. The modulation of the MMC switches is achieved using the phase-carrier-shift (PSC)-PWM modulation method. Key system parameters and threshold values are compiled in Table V. The efficacy of the proposed method is scrutinized across various scenarios, as elaborated in the subsequent cases.

A. Evaluation of proposed scheme under normal condition

Fig. 5 illustrates the performance of the converter employing the proposed scheme under normal conditions, with a constant R-L load applied. In Fig. 5(a), the MMC output voltage and current are displayed, featuring 15 voltage levels in the output voltage and a smooth waveform in the output current. The voltage waveform of the upper and lower arm capacitors is presented in Fig. 5(b), showcasing well-balanced capacitor voltages at the reference value of 2000 V. Fig. 5(c) exhibits the measured and estimated values of the capacitor voltage C_{u1} (the capacitor of the first SM of the upper arm), demonstrating that the estimated value appropriately tracks the measurement. The estimation error of the capacitor voltage

TABLE V. CRITICAL PARAMETERS OF SIMULATION AND EXPERIMENTAL STUDIES

PARAMETER		***Simulation values***	***Experimental values***
Capacitance (C_{ij})		6.8 mF	1.5 mF
DC Link Voltage (V_{dc})		28 kV	120 V
Modulation index (m_a)		0.95	0.85
Fundamental frequency (f)		50 Hz	50 Hz
Switching frequency (f_s)		1 kHz	500 Hz
Number of SM per arm (N)		14	4
Arm inductor (L_{arm})		5.5 mH	4.9 mH
Load	inductor (L_o)	15 mH	17 mH
	Load resistor (R_o)	30 Ω	30 Ω
Sampling period		1e-5 Sec	2e-4 Sec
V_{thmax}		42 kV	45 V
V_{thmin}		14 kV	15 V

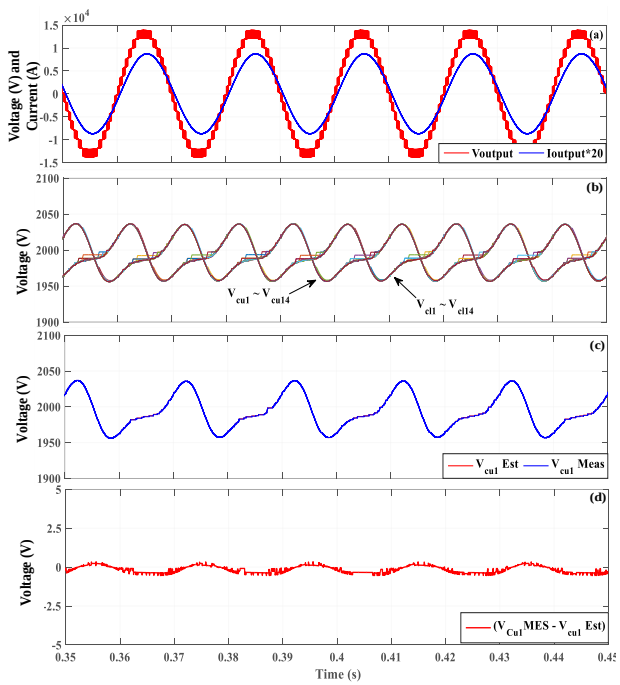

Fig. 5. Performance of the proposed scheme in normal conditions. (a) output voltage and current, (b) upper and lower arm capacitor voltage, (c) measured and estimated voltage V_{cu1}, (d) error of the estimated capacitor voltage V_{cu1}.

V_{cu1} (measured value minus estimated value) is depicted in Fig. 5(d), and its minimal value confirms the efficacy of the proposed scheme. Consequently, the simulations affirm that reducing the number of sensors does not compromise the normal performance of the converter.

B. evaluation of the proposed scheme with deviation in capacitance, and modulation index change

To further investigate the proposed scheme, the capacitance of the upper arm capacitors is simulated in a wide range of deviations. The capacitance deviation values of C_{u1} ~ C_{u14} are selected as follows: -30%, +5%, -7%, -10%, +10%, +5%, -15%, -12%, -6%, +13%, +20%, -3%, +7%, and +20% which results in the values of Cu1~Cu14 as: 4790 µf, 7140 µf, 6324 µf, 6120 µf, 7480 µf, 7140 µf, 5780 µf, 5984 µf, 61392 µf, 7684 µf, 8160 µf, 6596 µf, 7276 µf, and 5440 µf, respectively. Also, the modulation index decreases to 0.7 at t = 0.5 s. The simulation results, in this case, are shown in Fig. 6 and Fig. 7. The output voltage and current waveform under these conditions are shown in Fig. 6. The output voltage initially creates 15 voltage levels well, and after decreasing the modulation index, the number of levels has reduced to 11 levels. The output current waveform is completely sinusoidal, and after decreasing the modulation index, the value of output current has decreased. Fig. 7 (a) shows the voltage across the upper arm capacitors. The voltage ripple of the capacitors has slightly increased due to large deviations in the capacitance of the capacitors. However, the capacitors remain well balanced in their reference value. Capacitor voltage waveform V_{cu1} is shown in Fig. 7 (b) that despite a 30% deviation in capacitance, the estimated voltage value follows the measured value. Also, Fig. 7 (c) shows the voltage estimation error of capacitor V_{cu1}, which has increased due to deviation in capacitance. According to the results of Fig. 6 and Fig. 7, the presence of deviations in the capacitance of capacitors, MMC performance, was not significantly affected. On the other hand, such large deviations in capacitance (e.g., -30%) are unlikely in practical applications.

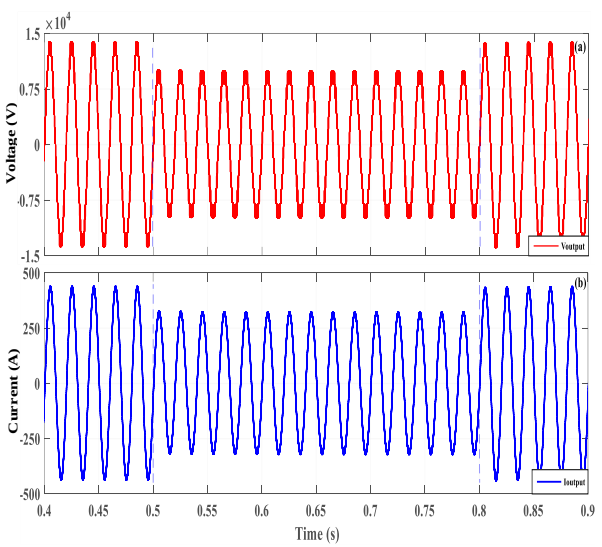

Fig. 6. Performance of the proposed scheme by changing the modulation index and deviation in the capacitance of the upper arm capacitors. (a) output voltage, (b) output current.

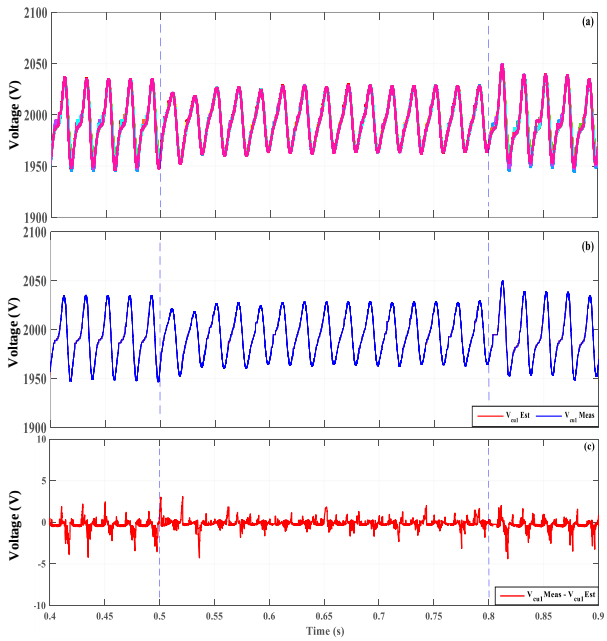

Fig. 7. Performance of the proposed scheme by changing the modulation index and deviation in the capacity of the upper arm capacitors. (a) upper arm capacitor voltage, (b) measured and estimated voltage V_{cu1}, (c) errors of the estimated capacitor voltage V_{cu1}

C. *Evaluation of proposed scheme with open-circuit fault*

The effectiveness of the proposed fault detection method is assessed by inducing open-circuit faults on different switches. At t = 0.4s, an open-circuit fault occurs at the upper switch SM_{u1} (S_{u11}). The simulation results, depicted in Fig. 8 and Fig. 9, underscore the efficacy of the proposed method. Specifically, Fig. 8(a)-(b) portrays the output voltage and current, as well as the arm current, respectively, post the fault occurrence. As anticipated, the output voltage and current experience disruptions and reductions, and the arm current are entirely diverted. In Fig. 8(c), the voltage of the upper arm capacitors is presented. Following the fault in S_{u11}, the capacitor voltages deviate from the reference value, with the defective SM capacitor exhibiting an increase compared to the others. Fig. 9 illustrates the performance of the proposed fault detection method, showcasing switching commands for group G_{u1} (S_{11} and S_{12}) at the fault detection moment in Fig. 9(a) and (b). Fig. 9(c) confirms the proposed method's accurate detection of the defective switch in the upper arm, with a fault detection time of t = 0.41245s, affirming its speed and accuracy in identifying faulty switches.

Fig. 10 displays the assessment results of the proposed fault detection method under an open-circuit fault on the SMu2 lower switch (S_{l12}). The outcomes reveal disturbances in the output voltage and current due to a failure in one of the switches. As illustrated in Fig. 10(b), the arm currents are entirely disrupted owing to power

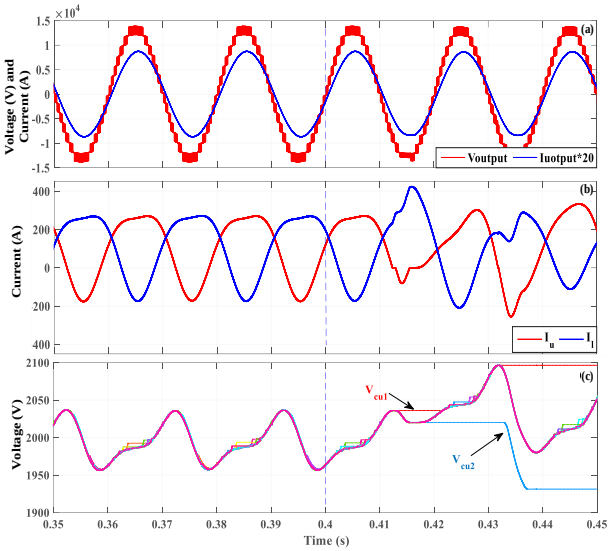

Fig. 8. Performance of the proposed scheme with lower switch fault (a) output voltage and current, (b) upper and lower arm current, (c) upper arm capacitor voltage.

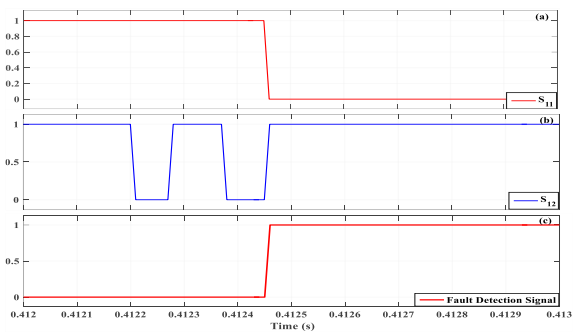

Fig. 9. Performance of fault detection method with a fault in the upper switch (a) switching command signal S_{11}, (b) switching command signal S_{12}, (c) fault detection signal.

imbalances in the arms. Moreover, the capacitor voltage of the defective SM experiences an increase. Fig. 11 demonstrates the performance of the proposed fault detection method in the presence of a fault on S_{l12}. The switching commands for the G_{u1} group are presented in Fig. 11(a) and (b) of the proposed scheme. The fault detection signal in Fig. 11(c) indicates that the proposed method accurately detects the defective switch at t = 0.40004s.

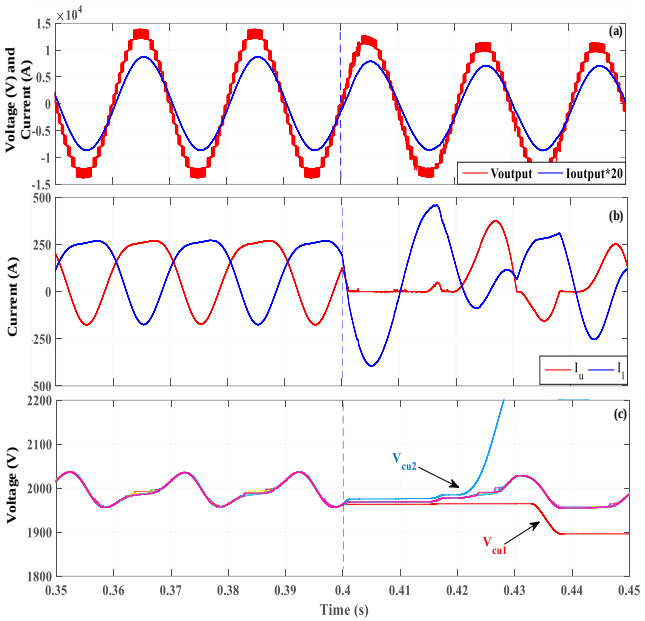

Fig. 10. Performance of the proposed scheme with lower switch fault. (a) output voltage and current, (b) upper and lower arm current, (c) upper arm capacitor voltage.

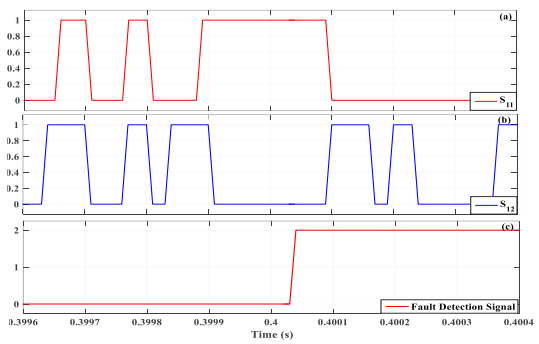

Fig. 11. Performance of the fault detection method a fault in the upper switch. (a) switching command signal S_{11}, (b) switching command signal S_{12}, (c) fault detection signal.

VI. Experimental Studies

For practical validation of the proposed approach, a laboratory prototype of a single-phase MMC with four SMs per arm has been constructed. The components of the laboratory prototype are illustrated in Fig. 5. IRF640N semiconductor switches are employed in the SMs, and the converter is controlled by a DSP TMS320F2812 microcontroller, which also executes the proposed scheme. The key parameters of the laboratory prototype are detailed in Table V.

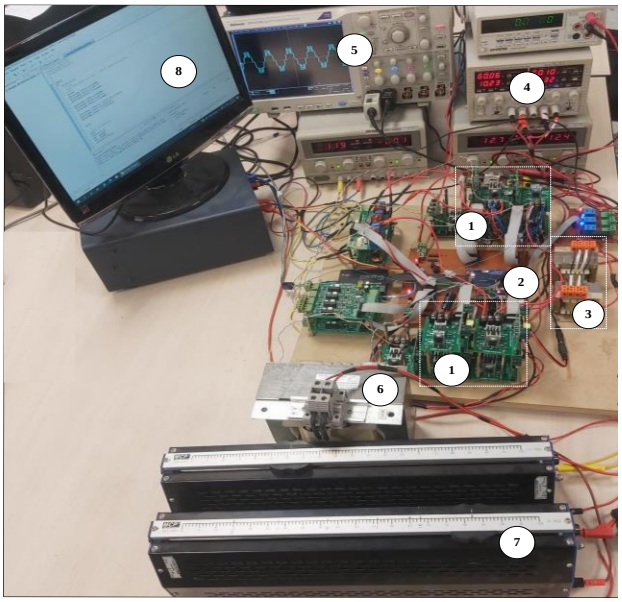

Fig. 12. Experimental topology of single-phase MMC (1) upper and lower arm, (2) DSP tms320F2812, (3) arm inductor, (4) DC source, (5) oscilloscope, (6) load inductor, (7) load resistor, (8) computer.

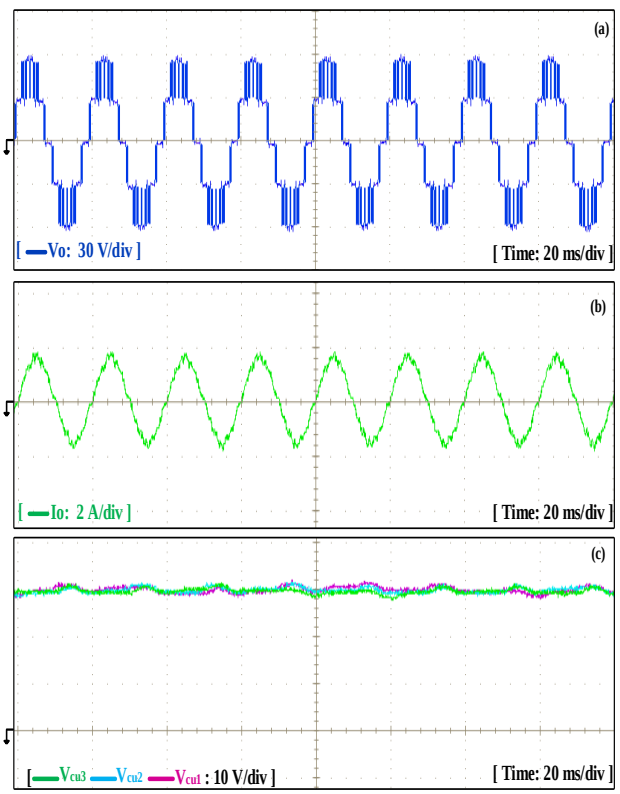

Fig. 13. Experimental results of MMC, under normal conditions (a) AC output voltage, (b) AC output current, (c) upper arm capacitor voltage.

A. Evaluation of proposed scheme under normal conditions

The experimental outcomes under normal conditions are presented in Fig. 13. In Fig. 13(a), the AC output voltage is shown with five levels. Fig. 13(b) displays the output current of the converter, featuring a sinusoidal shape. The voltages of the upper arm capacitors, illustrated in Fig. 13(c), demonstrate a well-balanced state at the reference value of 30V. According to the findings in Fig. 13, it is verified that the proposed scheme does not have a detrimental effect on the normal operation of the MMC.

B. Evaluation of proposed scheme with modulation index change

The experimental results of the proposed scheme are illustrated in Fig. 14, wherein the modulation index is varied from 0.85 to 0.4. In Fig. 14(a) and (b), the output voltage and current are depicted, revealing a reduction to 3 levels in the output voltage and a corresponding decrease in the output current after the modulation index reduction. Fig. 14(c) demonstrates that, despite the modulation change, the voltages across the upper arm capacitors continue to remain balanced.

C. Evaluation of proposed scheme with load change

The experimental outcomes with a sudden load change are presented in Fig. 15. Notably, the output current experiences a decrease following an abrupt increase in load impedance. Nevertheless, the voltages across the capacitors, as depicted in the figure, remain balanced. This observation underscores the effective performance of the proposed scheme under dynamic load conditions.

D. Evaluation of proposed scheme open-circuit fault

The fault detection algorithm relies on the identification of open-circuit faults through a comparison of group voltage output in normal and fault conditions. To validate this approach, an open-circuit fault is induced at time t_0 by manipulating the upper switch of SM_{u4}. This disruption affects the output current and voltage, as well as the voltage balance of the capacitors in the upper arm. The upper arm current is also impacted, and the proposed fault detection method successfully identifies the fault on the upper switch within 20ms, as illustrated in Fig. 16.

The experimental outcomes of applying single open circuit faults to three switches are outlined in Table VI (the fault time is consistent across all cases). As evident, the detection time of defective switches varies based on the switching status.

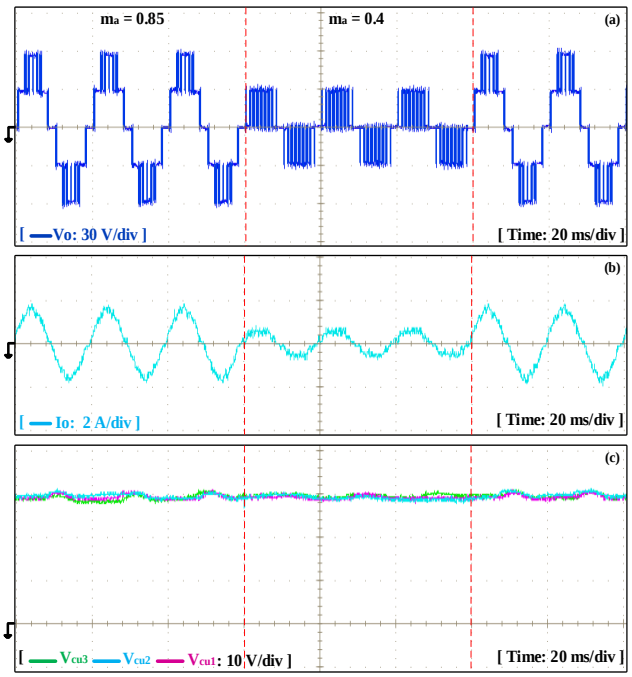

Fig. 14. Experimental results of MMC with changing the modulation index. (a) AC output voltage, (b) AC output current, (c) upper arm capacitor voltage.

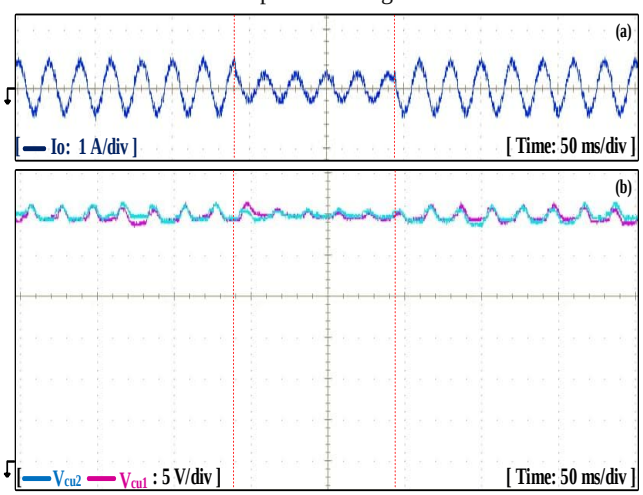

Fig. 15. Experimental results of MMC with a sudden increase in load impedance from 50% to 100% (a) AC output Current, (b) upper arm capacitor voltage.

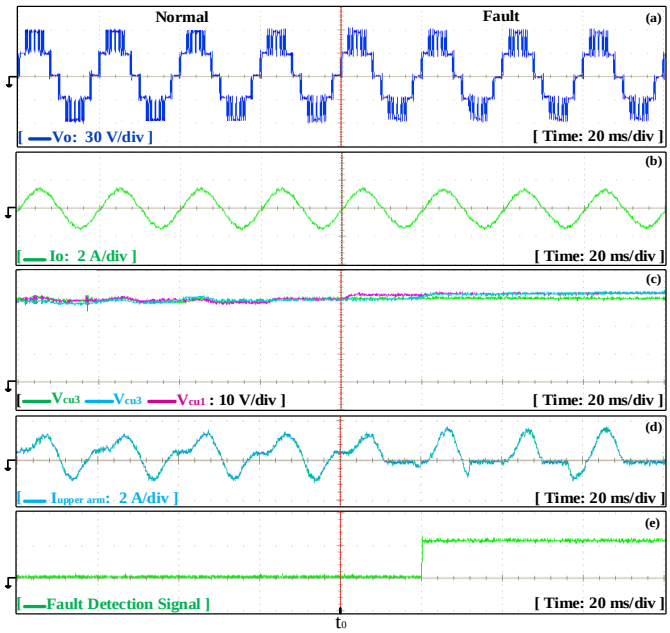

Fig. 16. Performance of the fault detection method with the occurrence of a fault in the upper switch. (a) AC output voltage, (b) AC output Current, (c) upper arm capacitor voltage, (d) upper arm current, (e) fault detection signal.

Table VI. EXPERIMENTAL RESULTS OF FAULT DETECTION

Location	*Detection time (Δt)*
SM_{u1} lower switch	6.2 ms
SM_{u2} upper switch	11.8 ms
SM_{u3} lower switch	9.8 ms

VII. Conclusion

This study introduces a technique aimed at diminishing the number of voltage sensors within SMs of MMC, with a specific focus on open-circuit fault detection. The approach involves halving the total number of voltage sensors through the reorganization of arm submodules and the estimation of capacitor voltages. This reduction in voltage sensors not only cuts down on system costs and complexity but also contributes to an enhancement in system reliability. Furthermore, in the estimation of capacitor voltages, the leverage of circuit relations governing MMC's topology is employed to alleviate computational burdens. The proposed method for fault detection involves a comparison of output voltages from each group of SMs under normal and defective conditions. This streamlined process enables the swift and straightforward identification of an open-circuit fault, surpassing the speed of many preceding methods. The fault detection method achieves remarkable accuracy, identifying open-circuit faults in less than one cycle. This swift detection significantly bolsters system reliability, rendering it more resilient for industrial applications. The proposed scheme exhibits potential for extension to a three-phase structure and is currently under investigation for future research endeavors.

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Design and Implementation of an N-Type Integer Phase-Locked Loop With Low Phase Noise and Two Output Frequencies at 1 and 4 GHz

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ABSTRACT

This article presents the development and implementation of an integer N-type Phase Locked Loop (PLL) module with two output frequencies of 1 and 4 GHz, each having a loop phase noise better than -110 dBc/Hz@10k. The structure has power levels of 0 and 10dBm at 1 and 4 GHz output frequencies, respectively. Having two different outputs of 1 and 4 GHz at once, in addition to the 1.1 and 4.4 GHz output frequencies realized by the capability included in this design in which two additional outputs can be achieved by using the pins A0 to A4 and altering their status, makes this structure a good candidate for mass production. A two-step frequency division is employed in this work. The first step is realized using the frequency divider of order 4, and the second step is implemented inside the HMC440 IC, including a PFD and a counter so that the output frequency approaches the closest to the reference frequency. Compared to the typical methods, this method presents a clean output by suppressing the spurs meant to be manifested using a single-step frequency division. This PLL is constructed in discrete and modular modes and employed in transceivers' up-converter and down-converter blocks, Satellite communications, Cable TV links (CATV), Local Area Networks (LAN), Global Positioning Systems (GPS), test equipment, digital radios, military and commercial communications. For a specific example, the 4-GHz frequency is used to up-converte or down-converte the received signals, and the 1-GHz frequency is usually used for the synthesizer module clock frequency. Advanced Design System (ADS) software was used in the design of the low-pass filter part of the loop, and OrCAD software was used in the schematic design of the phase lock loop module.

I. Introduction

As long as the Digital Signal Processing (DSP) technology is still incapable of directly processing and generating the Radio Frequency (RF) signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of the design of high-frequency wireless communication systems. Wireless transceivers must still be capable of generating a broad range of frequencies to up-convert the output signal for proper transmission and down-convert the received signal for proper processing. Even though there are various techniques for synthesizing the frequency, using the Phase-Locked Loop wireless communications industry. Like most wireless communication technologies, PLL is relatively new [1]. PLL is a control system with various applications in electronics and communications fields. It contains four basic parts: a Voltage Controlled Oscillator (VCO), a Phase-Frequency Detector (PFD), main and reference dividers, and a loop filter. PLLs can be implemented in two different ways: integer-N and fractional-N.

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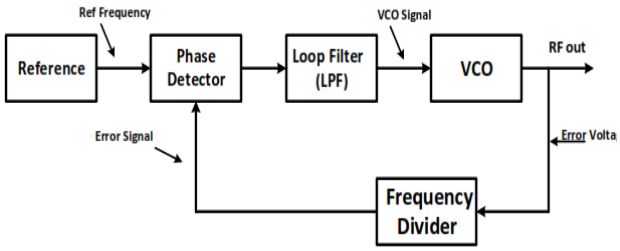

Fig. 1. The conceptual block diagram of a phase-locked loop.

A PLL can produce an output signal, the phase of which is dependent on the input signal. PFD, VCO, and the loop filter are a PLL system's most important and basic building blocks that strongly affect its practicality. In a simple PLL circuit, the reference and the VCO signals are connected to two ports at the input of the PFD circuit. The PFD output, which is an error signal, is applied to the loop filter. Then, the filtered voltage error is fed back to VCO. The diagram of the PLL blocks function is shown in Fig. 1. When the two input signals are small, the PFD block in the PLL circuit is actually a multiplier [2-14].

The two input signals are assumed as

$$v_i(t) = V_s \sin(\omega_i t + \theta_i) \quad (1)$$

$$v_o(t) = V_o \cos(\omega_i t + \theta_o) \quad (2)$$

in which v_i is the input signal applied to PFD, v_o is the PFD's second input from the divider circuit, ω_i is the input signal frequency, θ_i is the input signals phase, and θ_o is the phase of the output signals coming from the divider. The basic loop equation in the diagram shown in Fig. 2 can be achieved as follows:

$$V_d(t) = K_m V_i(t).V_o(t) = \frac{1}{2}K_m V_s V_o \sin(2\omega_i t + \theta_i + \theta_o) + \frac{1}{2}K_m V_s V_o \sin(\theta_i - \theta_o) \quad (3)$$

in which K_m is the multiplying factor in the multiplier with dimensions equal to $[V^{-1}]$. Because of the existence of the low pass filter in the loop, high frequencies can be neglected, and the equation can be rewritten as follows:

$$V_d(t) \approx K_m v_i(t).v_o(t) = \frac{1}{2}K_m V_s V_o \sin(\theta_i - \theta_o) = K_d \sin(\theta_i - \theta_o) \quad (4)$$

in which $K_d = \frac{1}{2}K_m V_s V_o$ is the gain factor of the multiplier in the PFD measured in volts per radian.

According to Fig. 2, the passband of the loop filter can be calculated in the diagram of a PLL system as

$$V_c(s) = v_d(s)F(s) \quad (5)$$

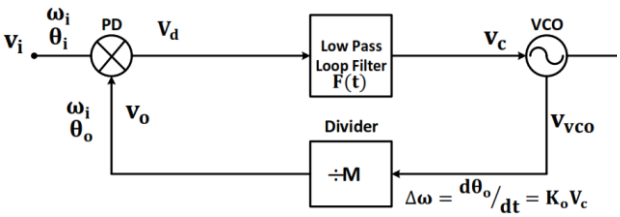

Fig. 2. A PLL diagram with more details.

The phase variations in the VCO circuit are theoretically linear and proportional to the control voltage in the input of the VCO, i.e.,

$$M\frac{d\theta_o}{d_t} = K_o V_c \quad (6)$$

in which K_o depicts the gain factor of the VCO, and M is the dividing order of the divider circuit. Based on the Laplace equations, the basic loop equation can be rewritten as

$$V_d(s) = K_d[\theta_i(s) - \theta_o(s)] \quad (7)$$

$$V_c(s) = v_d(s)\mathrm{F}(s) \quad (8)$$

$$\theta_o = \frac{K_o v_c(s)}{sM} \quad (9)$$

The open-loop transfer function is measured as follows:

$$G(s) = \frac{\theta_o(s)}{\theta_e(s)} = \frac{\theta_o(s)}{\theta_i(s) - \theta_o(s)} = \frac{K_o K_d F(s)}{sM} \quad (10)$$

The phase difference between the two input signals applied to PFD is depicted by θ_e and is measured as

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \quad (11)$$

The closed- loop transfer function of the PLL is achieved as

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d F(s)}{sM + K_o K_d F(s)} = \frac{G(s)}{1 + G(s)} \quad (12)$$

$$1 - H(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{\theta_i(s) - \theta_o(s)}{\theta_i(s)} = \frac{sM}{sM + K_o K_d F(s)} \quad (13)$$

Thus, the input voltage applied to the input of the VCO can be obtained as

$$V_c(s) = V_d(s)F(s) = K_d(s)\theta_e(s)F(s) = \frac{sMK_d F(s)\theta_i(s)}{sM + K_o K_d F(s)} = \frac{sM\theta_i(s)}{K_o}H(s) \quad (14)$$

This Work

This paper presents an integer N-type PLL module with two different output ports, which simultaneously produce two different frequencies of 1 and 4 GHz. The reference frequency of this module is 100 MHz, its bandwidth is 20 KHz, and it is presented as a discrete circuit so that it is implemented by connecting integrated circuits on a board. Based on the requirements, this module possesses two different outputs at the same time according to the required frequency. Also, by designing this module, it becomes possible to achieve two outputs of 1.1GHZ and 4.4GHZ instead of the pre-mentioned outputs by changing the status of pins A0 to A4 in PFD and using the proper VCO, which is suitable for mass production or customer order-based manufacturing of the module. The PCB board is designed with the option of having 4 outputs which are obtainable based on the desirable output between 1, 4 or 1.1, 4.4 GHz. This option is applicable by changing the connection status of the internal counter's pins located inside the PFD chip into voltage or ground and using the proper VCO while mounting the components [15-24].

As the output frequency is considered to be 4 GHz in this PLL, to compare the output frequency with the reference frequency at the input of the PFD, the output frequency must be divided into 40 in a feedback loop by the frequency divider to reach 100 MHz. In the PLL, items like stability, spur cancellation, and phase noise are inevitably important. Thus, for stability, ω_n which is the loop cut-off frequency must be smaller or equal to $0.1\omega_{ref}$ [28].

II. Loop filter

The low pass filter in a PLL block is either passive or active in the second order. H(s) depicts the feedback transfer function, which is, in this case, formed by the divider with the division ratio equal to N = H(s).

The forward transfer function $G_T(s)$ is the loop filter transfer function $G(s) * K_0 * K_d$.

$$Overall\ transfer\ function = \frac{G_T(s)}{1 + G_T(s).H(s)} \quad (15)$$

To obtain a proper control voltage and bandwidth in this module, an active filter is used whose schematics are demonstrated in Fig. 3. To have proper stability, A low frequency zero and pole is used to ensure proper stability. Also, C_2 which is approximately five times smaller than C_1 is used to cancel the reference frequency spurs. Finally, some resistors and some capacitors much smaller than C_1 are added after the filter to cancel all spurs completely.

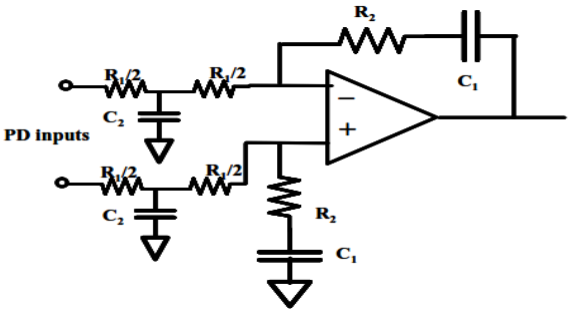

Fig. 3. The active filter structure with OPA211 used in this work.

To obtain a proper control voltage and bandwidth in this module, an active filter is used whose schematics are demonstrated in Fig. 3. To have proper stability, A low frequency zero and pole is used to ensure proper stability. Also, C_2 which is approximately five times smaller than C_1 is used to cancel the reference frequency spurs. Finally, some resistors and some capacitors much smaller than C_1 are added after the filter to cancel all spurs completely. Considering that the number of capacitors added is much lower than C_1, the transfer function is still considered to be of second order with a proper approximation [8, 28-30].

$$\frac{V_o}{V_{in}} = G(s) = \frac{1 + sT2}{(sT1)^2 + 2sT1} \quad (16)$$

The closed-loop PLL [28].

Open-loop gain:

$$LG(s) = \frac{Kd.Ko}{N}.G(s) = \frac{\frac{Kd.Ko}{N}.(1 + sT2)}{(sT1)^2 + 2sT1} \quad (17)$$

Closed-loop gain:

$$H(s) = \frac{\frac{Kd.Ko}{N}.G(s)}{1 + \frac{Kd.Ko}{N}.G(s)} = \frac{1}{1 + \frac{(sT_1)^2 + 2sT_1}{\frac{Kd.Ko}{N}.G(s)(1+sT_2)}} \quad (18)$$

The loop elements are obtained using the characteristics of the VCO, PFD, natural frequency of the loop, division ratio of the loop, and damping factor selected by the designer. These relationships can be expressed in the two following ways.

A) The first method:

Loop filter calculation of R1:

Assumed as Eq. (18)-(24);

$$N = \frac{VCO\ frequency}{Phase\ detector\ frequency} \quad (19)$$

$$\text{Loop bandwidth} = 2\pi.\omega_n \quad (20)$$

$$K_{VCO} = VCO\ sensitivity\ \left(\frac{MHz}{V}\right) \quad (21)$$

TABLE I
RESULTING PHASE MARGINS FROM A GIVEN DAMPING FACTOR

DAMP – FACTOR ξ	Phase Margin (degrees)
0	0
0.5	51.8
0.707	65.5
1	76.3

$$K_{PD} = Phase\ detector\ sensitivity\ \left(\frac{V}{rad}\right) \quad (22)$$

$$\tau_1 = R_1.C_2 \quad (23)$$

$$\omega_n = \sqrt{\frac{K_{VCO}.K_{PD}}{N.\tau_1}} = \sqrt{\frac{K_{VCO}.K_{PD}}{N.R_1.C_2}} \quad (24)$$

Rearrange to get R1 to assume a value for C2;

$$R_1 = \frac{K_V.K_\varphi}{\omega_n^2.N.C_2} \quad (25)$$

Loop filter calculation of R2:
The value of R2 is determined by setting the phase margin of the loop and is related to the damping factor ξ.
The phase margin, which is the difference between the argument of the loop gain and -180° at the frequency where the loop gain becomes unity, is given as

$$\theta = \tan^{-1}\left(\frac{2\xi\omega}{\omega_n}\right) = \tan^{-1}\left[2\xi\sqrt{2\xi^2+\sqrt{4\xi^4+1}}\right] \quad (26)$$

For a range of damping factors, the predicted phase margin can be calculated as shown in Table I [28].

Assuming a damping factor of 0.707 to give us a phase margin of 65°, the value of R2 is given as

$$\xi = \frac{\omega_n.T_2}{2}\ ,\ T_2 = R_2.C_2 \quad \Rightarrow \quad \xi = \frac{\omega_n.R_2.C_2}{2} \quad (27)$$

Loop filter calculation of C1 is obtained as the following assuming that Fc = 10*Fn [28]:

$$\tau_c = \frac{1}{2\pi F_c}\ ;\tau_c = \left(\frac{R_1}{2}\ ||\frac{R_1}{2}\right).c_1\ ;\ \tau_c = \frac{R_1.C_1}{4}$$

$$\Rightarrow \quad C_1 = \frac{4.\tau_c}{R_1} \quad (28)$$

B) The second method:
The above relationships can be summarized to calculate the values of the loop filter elements:

$$C_1 = \frac{k_{VCO}.k_{PD}}{\omega_n^2.N.R_1} \quad (29)$$

$$R_2 = \frac{2\xi}{\omega_n C_1} \quad (30)$$

$$C_2 = \frac{2}{\pi R_1 F_C} \quad ; \quad 10F_N < F_C < F_{PD} \quad (31)$$

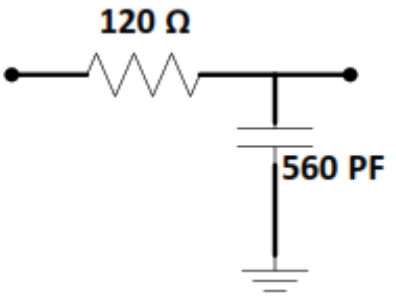

Fig. 4. The low-pass filter with a far pole compared to F_N.

By choosing the value of one of the elements, the values of the other elements of the loop filter are calculated. Since the high-frequency pulses of PFD can cause the nonlinear behavior of the operational amplifier, a low-pass filter is used at the input of the loop filter, and since the structure of the loop filter together with the operational amplifier is an integrator, the input low-pass filter is called a pre-integrator filter that prevents the nonlinear behavior of the operational amplifier by filtering high-frequency pulses.

Generally, the cut-off frequency of the pre-integrator filter is selected at least 10 times the main natural frequency of the circuit so as not to disturb the operation of the main filter. In the above relationships used to calculate the elements of the loop filter, the natural frequency is employed, which is the relationship between the natural frequency of the loop and the F3db bandwidth calculated by choosing ξ. Having known F_{3db}, F_N will be assumed as

$$F_{3db} = F_N\left[1+2\xi^2+\sqrt{1+(1+2\xi^2)^2}\right]^{\frac{1}{2}} \quad (32)$$

Resistance is considered to be $R_1 = 200\Omega$. According to the information included in the information sheet of chips, the parameters of the loop are as follows:

$k_{PD} = 0.3\ \ V/Rad$
$k_{VCO} = 2\pi \times 15\ \ MH/V$
$N = 40$
$F_{3db} = BW = 20\ KHz$
$F_N = 8\ KHz$
$\omega_n = 2\pi \times F_N = 50.24\ KHz$
$\xi = 1$
$C_1 = 10\ nF$
$R_2 = 390\ \Omega$

If $C_2 = 2.7nF$ is selected, the bandwidth of the pre-integrator filter loop will be equal to $F_c = 1.18MHZ$, which is sufficiently larger than $F_N = 8kHz$. Since, in this application, the output frequency of the synthesizer does not change quickly, and there is no high-speed frequency jump, choosing a large value of ξ helps stabilize the loop as much as possible and reduce the unwanted overshoots.

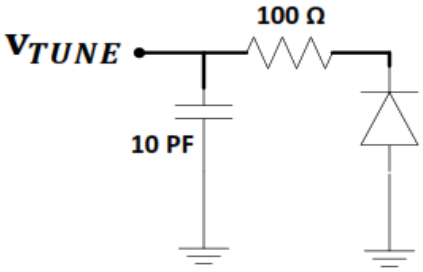

Fig. 5. The internal circuit for the VCO base voltage adjustment.

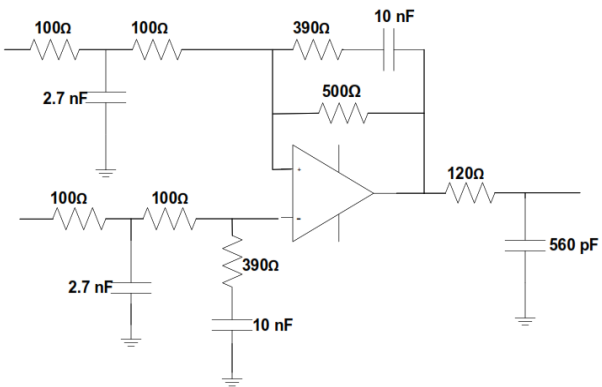

Fig. 6. The final schematic of the loop filter circuit.

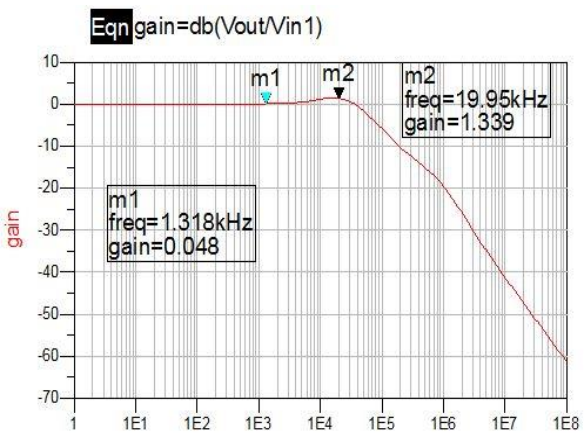

Fig. 7. The frequency response of the simulated active LPF in ADS.

Generally, a low-pass filter with a pole far enough from F_N is used after the main loop filter to prevent the reference signal from settling in the synthesizer output. For this purpose, the circuit of Fig. 4 with $F_{cut} = 2.37\ MHz$ is used.

The important point is that the value of the selected capacitor must be larger enough than the value of the internal capacitor of the next piece, which is actually the VCO so that when these two capacitors are paralleled, the capacitor of the low-pass circuit is dominant.

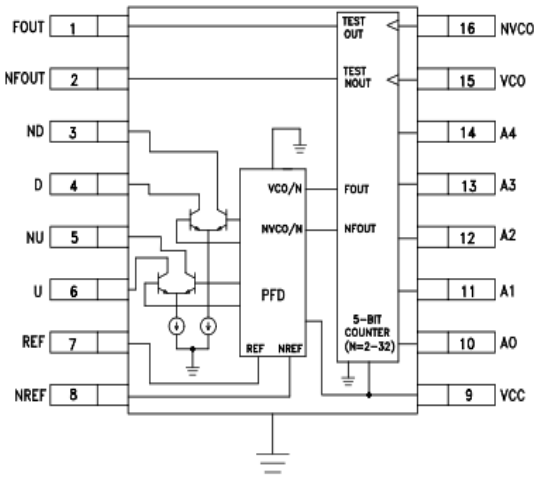

Fig. 8(a).PFD IC internal circuits [35].

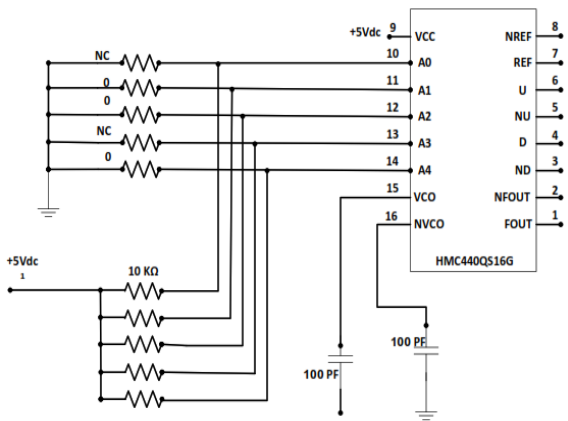

Fig. 8(b).A0-A4 connection.

According to the information sheet of CRO3956A-LF shown in Fig. 5, the base input capacitor of the regulation voltage is equal to 10 pF, as a result of which the value of the low-pass filter capacitor was chosen to be 560pF.

The final phase-locked loop filter is implemented according to Fig. 6. This circuit was first simulated using Agilent Advanced Design System software, and its frequency response is shown in Fig. 7.

III. Frequency divider & pfd

To apply the 4-GHz frequency to the input of the PFD using the feedback loop to be further compared with the reference frequency, the 100-MHz frequency can be achieved by using a frequency divider of order 40. In a single-step frequency division, only one output frequency signal is obtained. Also, a big disadvantage this approach brings to the process is that many spurious tones are created in the single-step division process. In this work, to have two outputs at the same time, the frequency division is realized in two steps, which, in addition to having 2 outputs simultaneously, spurs that were meant to emerge due to the high division order in a single step division are minimized since the frequency division order in the

feedback loop decreases.

In the first step, using the HMC36558GE IC, a frequency divider of order 4, the 4-GHz frequency is divided by 4, thus equaling 1GHz. Given that this frequency divider gives two separate outputs with the same frequency, one is used as one of the two outputs of the PLL with an output frequency of 1 GHZ after amplification.

In the second step, by choosing the order of division using the internal counter within the HMC440 IC, the frequency division circuit is realized by this internal counter, and the order of division is specified by the status of the physical connection of pins A0 to A4 as shown in Fig. 8(b), to ground or voltage. The other 1-GHZ output frequency of the divider mentioned above is, in the first step, divided by 10 and becomes equal to 100 MHz. Then, this 100-MHz frequency is applied to the input of the PFD circuit within the HMC440 IC and compared with the reference frequency. Accordingly, the phase and frequency difference is eventually detected [25-27, 31-34].

IV. PLL design and implementation

Using the technical specifications in datasheet of PFD, OpAmp, VCO, and frequency divider chips and designing the active low-pass filter and according to Equation (33) and all phase noise and loop filter calculator, the product of Peregrine Semiconductor Corporation [46], the estimated phase noise diagram is shown in Fig. 9. The phase noise estimates shown are typical and not exact. Actual phase noise may vary. This value is estimated and obtained according to the calculations from the element datasheet, and it is expected to have worse phase noise after the implementation and measurement. Fvco is the operating frequency of the frequency controller chip with voltage.

According to Figs, 10 and 11, the circuit includes a PLL at 4 GHz, designed for the best achievable phase noise, with the reference input from a 100-MHz OCXO crystal oscillator. The HMC440 chip [36] is used as a PFD in this loop, which has a suitable phase noise. Since the HMC440 chip must bring the output frequency to a value close to the reference frequency in order to compare the output frequency with the reference frequency, the presence of a frequency divider is necessary. For this purpose, a pre-divider by four with chip number HMC365S8G [35] from Analog devices Corporation is used, which consumes less current than similar products of Hittite Microwave Corporation.

As a result to lower current consumption, the total power consumption is lower, thus less heat will be produced.

A VCO with the chip number ROS-3997[37] was also used. It has a good phase noise at 4-GHz frequency. However, it should be noted that there is an expectation that the phase noise measurement results of the implemented module would be worse than the estimated value.

According to the datasheet and calculation[36], the PFD phase noise and the in-loop phase noise are achieved as

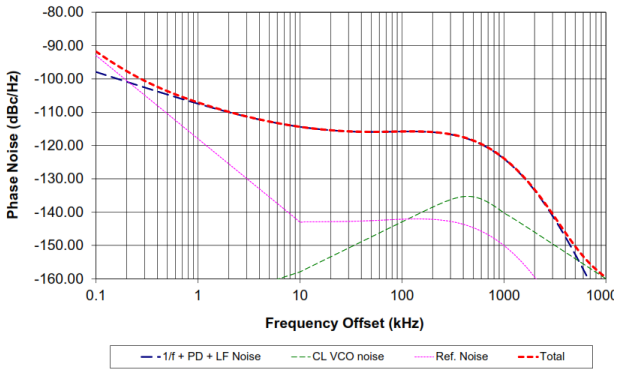

Fig. 9. The PLL phase noise estimated at VCO output (Fvco = 4 GHz; VCO = ZCOMN CRO3956-LF; Ref=Wenzel 100MHz ULN OCXO)

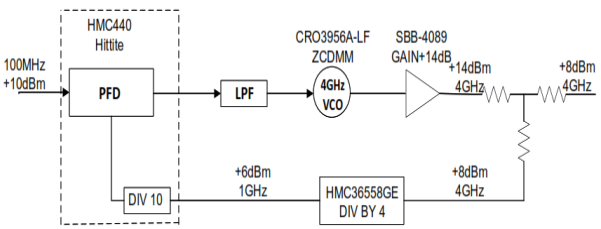

Fig. 10. The proposed PLL block diagram.

$$\text{Phase noise (PFD)} = -153\text{dBc/Hz@10kHz}$$
$$\text{In-Loop Phase Noise} = \text{PFD Noise phase} + 20\log(N) = \text{-121 dBc/Hz @ 10kHz Offset} \quad (33)$$

According to Figs. 11 and 12, the schematics of the PLL module are completed now and simulated using OrCAD.

The output signal of VCO with this structure possesses an output power level of 0 dBm. Then, this output power level is amplified to +14 dBm using an SBB4089 amplifier with a gain equal to +14 dBm. Then, using a resistive power divider, the output frequency is split into two identical branches with frequency and power levels of 4 GHz and +8 dBm, respectively. One of these branches reaches the power level of +10.07 dBm using an SKY65017 [38] amplifier and is reachable using an SMA connector, and the other branch is applied to the frequency divider. On the other hand, the frequency divider used in the feedback loop gives two identical 1-GHz outputs. One is reachable after the required amplification using an SBB4089 [39] amplifier with +1.17 dBm power through an SMA connector. The other output is applied to the input of PFD to be compared to the reference frequency [1, 17, 40-42]. Fig. 13 shows the implemented PLL module and its different building blocks arranged on a board.

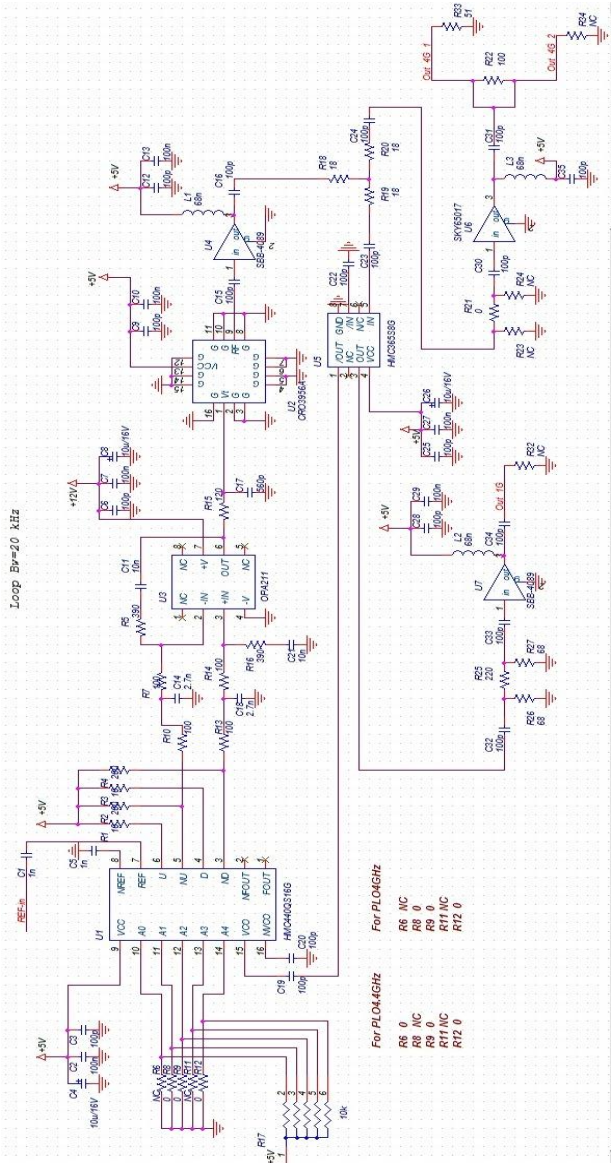

Fig. 11. The completed schematic of the proposed PLL module

Fig. 12. The dimensions of module PLL implemented.

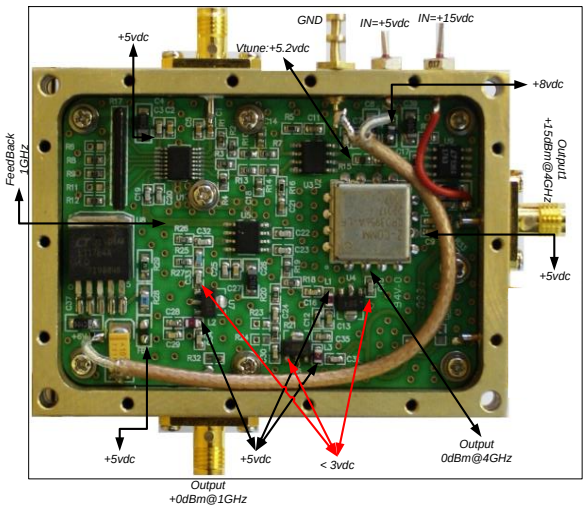

Fig. 13. The final module made with the voltages of the test points.

V. Measurement and results

For testing and commissioning, 15V and 5V power supplies are applied to the module, according to Fig. 13.

Then, a source (i.e., signal generator) gives 100MHz input and 9dBm power to the module, and the module's output is checked in the Spectrum Analyzer. As shown in Figs. 14 and 15, output 1 must have a signal with a frequency of 4GHz with a power of at least 10dBm, and a signal with a frequency of 1GHz with a power of at least 0dBm should be in the output of Output 2. In three span modes, 500 kHz, 10 MHz, and 100 MHz, spur should not be observed in both 4GHz and 1GHz frequencies.

After ensuring the correct operation of the module, the spectrum must be put in Max Hold mode. Then, the module must be put under load for about 12 hours. Spur should not be recorded during this period around the 4GHz signal on the spectrum screen. After the above steps, the following parameters are measured with the spectrum:

1-Signal power

2-Checking spur in three spans: 500 kHz, 10 MHz, and 100 MHz.

3- Phase noise measurement at 10kHz offset

To measure the implemented PLL module parameters, the devices mentioned below were used. The results are explained.

A) Spectrum analyzer Agilent E4407B 9kHz -26.5GHz

B) MXG Analog Signal Generator N5183A 100kHz-20GHz

As can be seen in Figs. 14-17, the measured phase noise and power level in the 4GHz output port are equal to -114.17dBc/Hz and +10.07dBm, respectively, and the phase noise and power level are -117dBc/Hz and 1.17dBm in the 1GHZ output port, respectively.

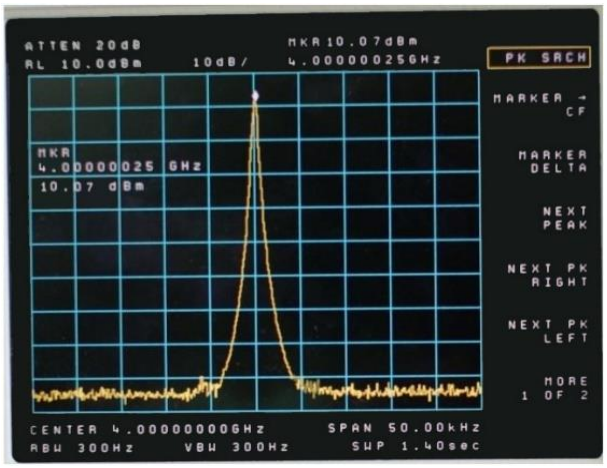

Fig. 14. Measuring the power level of the output port with a frequency of 4 GHz (X-axis= frequency (GHz), Y-axis= power level (dBm)).

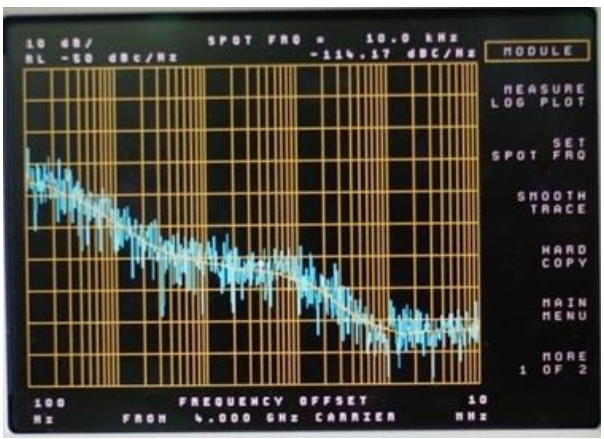

Fig. 15. Output port noise phase measurement with a frequency of 4 GHz (-114.17dBc/Hz @10kHz offset)

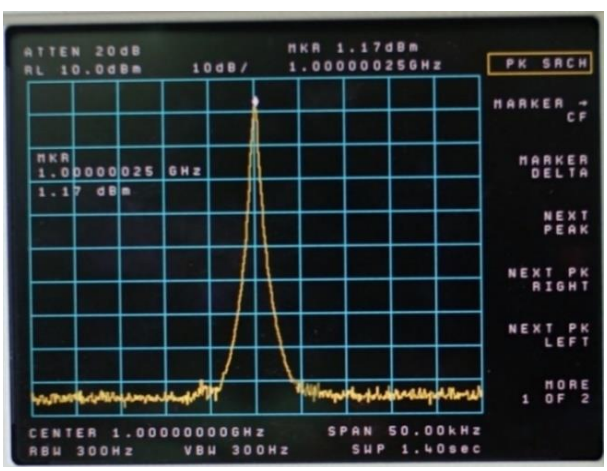

Fig. 16. Measuring the power level of the output port with a frequency of 1 GHz (X-axis= frequency (GHz), Y-axis= power level (dBm)).

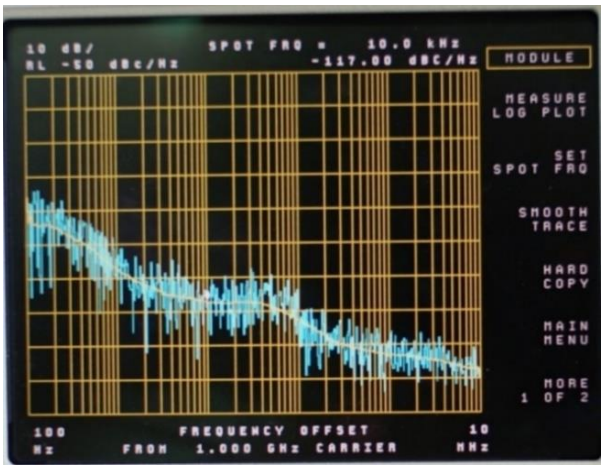

Fig. 17. Output port noise phase measurement with a frequency of 1GHz (-117dBc/Hz @10kHz offset).

The final implemented PLL module with its voltage testing nodes in the circuit is shown in Fig. 13. This module is generally employed in transceiver systems. Detailed experimental results and characteristics of the proposed implemented PLL module are presented in Table II.

According to Table II, this module has two outputs with frequencies of 4 and 1 GHz, each of which has a power level equal to +10.07 and +1.17 dBm, respectively, and a phase noise less than -114 and -117 (dBc@10kHz). The input reference frequency is 100 MHz, and the power level of the input signal is +9 dBm. This module is powered by voltages of +15 and +5 Vdc. It has a current consumption of less than 10 and 1000 mA at the input, respectively. The working temperature of this module is from -40 to +80 ◦C, and it is implemented with the dimensions of 2.91 x 2.12 x 0.39 inches.

Various American companies (including Fairview Microwave [43], Dynamic Microwave [44], Millimeter Wave Products Inc.[47], Raditek Inc.[48], Z-Communication Inc.[49], Lotus Communication systems Inc.[50]) have been active in the field of manufacturing phase-locked modules and have products that can be supplied to customers.

Given that the work presented in this article is discrete (not on-chip), the best comparison would be through comparison with similar products. Therefore, among the products of active companies in this field, a product that is similar to this work in terms of application and frequency range has been selected for comparison, and the results of comparing the technical characteristics of PLL made with similar products have been presented. Table III.

TABLE II
TECHNICAL SPECIFICATION OF THE PLL MOUDULE MADE

Quantity	Description	Specification
Output	Frequency(GHz)	4&1
	Power(dBm)	+10.07 & +1.17
	phase noise (dBc@10kHz)	<-114 & <-117
Reference	Input ref.(MHz)	100
	Input power(dBm)	+9
Electrical	Supply Voltage (Vdc)	+15 & +5
	Input Current (mA)	<10 & <1000
Connector table	15V	Feed Thru
	5V	Feed Thru
	GND	Feed Thru-GND
	REF	SMA-F
Dimension	mm	73 × 53 × 9
Operating temp.	◦C	−40 to +85°C

TABLE III
PERFORMANCE SUMMARY OF THE FOUR PLL

Quantity	This work	[43]	[44]	[45]
PLL Type	INTEGER-N	INTEGER-N	-	INTEGER-N
Output freq. (GHz)	4&1	4	1-50	4 or 5
Out. Power (dBm)	10.07 & 1.17	+7	13-25	-
Phase Noise (dBc/Hz@ 10 KHz)	< -114 & < -117	-110	-110	-111
Rrf Freq. (MHz)	100	100	10 or 5	100
Input power (dBm)	+9	+7	-	+7
Supply Voltage (Vdc)	+15 & +5	+12	+12&+15	2.7
Input Current (mA)	<10 & <1000	150	330	75
Connector	SMA-F	SMA-F	SMA-F	Solder pins
Dimension (mm)	73 × 53 × 9	50.8 × 38.1 × 15.24	57 × 57 × 32	-
Implementation Type	Discrete	Discrete	Discrete	The compact 44-lead (CQFP) PACKAGE
Operating temp.	−40 to +85°C	−30 to +70°C	−55 to +105°C	−40 to +85°C

VI. Conclusions

Design procedures for N-type integer non-integrated modular PLL lead to four different outputs using four external pins. This versatility makes it a good candidate for mass and consumer-based production. The phase noise and the power level of the generated frequency signals are equal to -114.17dBC/Hz and 10.07dBm for the 4GHz output and -117dBC/Hz and 1.17dBm for the 1GHz output, respectively. Compared to the previous works, the designed PLL shows good performance regarding each output's phase noise and power level, as well as power consumption and module size. Also, the low phase noise of the output signals shows that this module is good for the high-precision up/down converting process for K-band signals in K-band transceivers.

VII. Acknowledgment

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Lightweight Structure of Random Key Generation for PRESENT Block Cipher

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ABSTRACT

In this paper, we design a lightweight and modified random key generation for PRESENT block cipher which is applicable in the encryption of the digital signals. In the block ciphers, the master key is used directly in the encryption process for the data (plaintext). But in this work, a master key (initial key) is used to derive the new random master keys (random session keys) and use these keys for the encryption process. The use of random keys will overcome the brute force attack that can be applied to the PRESENT cipher. The random session keys generated will produce different ciphertexts for the same plaintext for every session. In this approach, we take advantage of the block cipher to produce random keys. The PRESENT cipher is shared in both random key generation and encryption process. Therefore, the proposed structure has both random key generation and data encryption in a unified circuit. This property reduces hardware resources. The implementation results, in 180 nm CMOS technologies, show the proposed structure is comparable in terms of area and delay with other works.

I. Introduction

Due to the rapid advancements in communication systems and digital broadcasting, data security in these systems has become a major research challenge. It is essential to develop techniques for providing security. To secure the proprietary, digital signals such as image, sound, ... need to be ciphered before transmission using encryption techniques. The security of encrypted digital signals can always be improved through new encryption methods. Therefore, new encryption schemes that can protect data are efficiently researched. In recent years, many cryptographic techniques such as lightweight block ciphers have been proposed for the security of the digital signals [1]-[2]-[3]. PRESENT [4] is a lightweight block cipher that is standardized in the ISO/IEC 29192-2, with an efficient structure [5]. This cipher is suitable for the realization of crypto-processors. It has the Substitution Permutation Network (SPN) structure with 64-bit block size and 80- and 128-bit key sizes. The number of rounds in the PRESENT cipher is equal to 31. Add round key, substitution layer (S-box), and permutation layer are the main blocks of the PRESENT cipher. In work [6] the identification and classification of recent research practices about the flexible hardware implementation of cryptographic algorithms are presented. The identified researches have been classified according to three design approaches: (1) cryptoprocessor, (2) crypto coprocessor, and (3) multicore crypto processor. Consequently, a comparative analysis of various cryptographic algorithms in terms of flexibility, throughput, area, power, and implementation technology has been presented. Based on work [11] the PRESENT cipher has a reasonable area and time complexities for cryptography applications. This block cipher is suitable for low-cost and ultra-light implementations. The throughput and speed of this block cipher are also important

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factors for hardware implementation. Hardware implementation of a cryptographic system has advantages over software implementation, such as increasing the speed of data processing and increasing the security of that system. On the other hand, random key generation is a very important issue for symmetric key encryption. Therefore, in this paper, we are looking for the optimal hardware implementation of a cryptographic system with the random key generation ability.

The hardware design of block ciphers is an important subject in the literature. The area consumption and time delay of the symmetric key cryptosystems depend on the block ciphers. Therefore, a block cipher is a key subject in determining implementation performance. Several hardware structures of the PRESENT cipher have been reported in works [7]-[16]. In work [8] three structures of the PRESENT consisting of pipelined structure, serial structure, and round structure are proposed. Between these structures, the pipelined structure has the most area compared to the other structures. The serial structure is the slowest compared to the other structures. The round structure has more throughput compared to the serial structure, but it consumes a high area. The PRESENT algorithm is implemented based on a Single-cycle structure in work [9]. An optimized circuit for the S-box is presented in work [10]. In work [11] a low latency and high throughput structure of the PRESENT is proposed based on the loop unrolling technique. Also, the S-box is implemented based on a low-area circuit. In work [12] both key sizes 80- and 128-bit are supported based on a high-throughput and flexible hardware structure of the PRESENT algorithm for IoT applications. In [15] the design of three different types of S-box architectures for the PRESENT cipher to optimize the design parameters for resource-constrained applications are presented. In the previous works, there is no random key generation unit. This subject is the main limitation of existing circuits for PRESENT cipher. In addition, the works [9] and [12] consume high hardware resources for the implementation of the PRESENT cipher. On the other hand, the computation time and the number of clock cycles for generating ciphertext in the works [7]-[8] and [16] are also high. In the present work, we have achieved acceptable hardware results and time specifications compared to previous works. Also, in the proposed system, there is a random key generation unit based on the PRESENT algorithm is used to reduce the hardware.

The encryption of digital signals such as image encryption is needed to perform real-time communication with a random key generator unit. So how to carry out the image encryption has also become a hot issue [17]-[20]. The key generator can improve the security issues of the encryption algorithms and increase the amount of text required for the differential attacks [21]-[22]. Therefore, in this paper, we present a modified random key generation algorithm for the PRESENT cipher. The results, in 180 nm CMOS technology, show that the proposed structure has acceptable hardware resources, timing characteristics, and security properties compared to the other works. The contributions of this paper are as follows:

- In this work, the master key is used to derive the new random master keys (random session keys) and use these keys for the encryption process. In this approach, we take advantage of encryption to produce random keys.
- The PRESENT cipher is shared in both random key generation and encryption processes. This property reduces hardware resources.
- The proposed structure has both random key generation and data encryption in a unified system which can be used in digital signal encryption with a high number of data.
- In the PRESENT cipher, to further reduce the logic gates of the 4-bit S-boxes, we applied further simplifications on the expression terms of the S-boxes for more area optimization. Therefore, a low-cost 4-bit S-box for the PRESENT cipher is achieved. For the 128-bit key, the area consumption, computation time, and throughput of the proposed method are equal to 2583 GEs, 52.928 ns, and 1209 Mbps, respectively, which are acceptable compared to the other works.

The rest of the paper is organized as follows. The PRESENT cipher is summarized in Section 2. The random key generation method is presented in Section 3. In Section 4 the proposed structure of random key generation is described. Security of the proposed structure is presented in Section 5. Section 6 shows a comparison between our structure and related works. Finally, the paper is concluded in section 7.

II. PRESENT Block Cipher

The PRESENT is a 31-round block cipher for low-cost cryptographic applications [4]. In each round, we have a 64-bit round key addition, 16 4-bit substitution boxes (S-boxes), and a 64-bit permutation layer (pLayer). It has a block size of 64-bit and a key size of 80- or 128-bit. The round keys are the 64 most significant bits of the supplied key.

A. S-box

The substitution layer is composed of 16 4×4-bit S-boxes. The S-box used in PRESENT is a 4-bit to 4-bit S-box. The input nibbles (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F) are substituted by the output nibbles (C, 5, 6, B, 9, 0, A, D, 3, E, F, 8, 4, 7, 1, 2), respectively.

B. Proposed Protection Scheme Using DS-DOCRs Considering N-1 Contingency

The PRESENT can support keys with sizes 80- or 128-bit. The key schedule of the PRESENT cipher consists of a left cyclic shift (rotate to left), several S-boxes, and a 5-bit XOR

with the values of the least significant bit of the round counter (RC). Let the main key be $K = k_{127}, k_{126}, \ldots, k_1, k_0$ ($K = k_{79}, k_{78}, ..., k_1, k_0$ for 80-bit). In round i, the 64-bit round key $K_i = \kappa_{63}, \kappa_{62}, ..., \kappa_1, \kappa_0$ consists of the 64 leftmost bits of the current K content. Thus, in round i we have $K_i = \kappa_{63}, \kappa_{62}, \ldots, \kappa_1, \kappa_0 = k_{127}, k_{126}, ... k_{65}, k_{64}$ and $K_i = \kappa_{63}, \kappa_{62}, \ldots, \kappa_1, \kappa_0 = k_{79}, k_{78}, \ldots, k_{17}, k_{16}$ for 80-bit. The key update process for 80-bit keys is as follows:

$$\kappa_{i+1}[79:76] = S - box(\kappa_i[79:76]), \quad (1)$$

$$\kappa_{i+1}[75:20]||\kappa_i[14:0] = \kappa_i[75:20]||\kappa_i[14:0], \quad (2)$$

$$\kappa_{i+1}[19:15] = \kappa_i[19:15] \oplus RC. \quad (3)$$

Also, for the 128-bit keys we have the following key update:

$$\kappa_{i+1}[127:124] = S - box(\kappa_i[127:124]), \quad (4)$$

$$\kappa_{i+1}[123:120] = S - box(\kappa_i[123:120]), \quad (5)$$

$$\kappa_{i+1}[119:67]||\kappa_i[66:0] = \kappa_i[119:67]||\kappa_i[66:0], \quad (6)$$

$$\kappa_{i+1}[66:62] = \kappa_i[66:62] \oplus RC. \quad (7)$$

The operations $\oplus$ and $||$ represent bit-wise XOR and concatenation, respectively.

III. Random Key Generation

The random key generation which is used in this paper is based on work [23]. Here, we modify the random key generation algorithm of work [23] for the PRESENT cipher. The random session keys are generated based on generated random numbers. In the block ciphers, the master key is used directly in the encryption process. But in this work, a master key is used to derive the new random master keys (random session keys) and use these keys for the encryption process. In this method, we take advantage of the encryption process to produce random numbers. The PRESENT cipher is used as the heart of the random number generation. To our knowledge, this paper is the first work to use the PRESENT cipher for the random key generation process. Because this process generates strong random numbers as the random keys. We take advantage of the block cipher to produce random keys. The proposed structure has both random key generation and data encryption in a united circuit. This block cipher is suitable for low-cost and ultra-light implementations. The throughput and speed of this block cipher are also important factors for hardware implementation. Therefore, the PRESENT cipher is shared in both random key generation and encryption processes. This feature reduces hardware resources and the generation of strong random numbers.

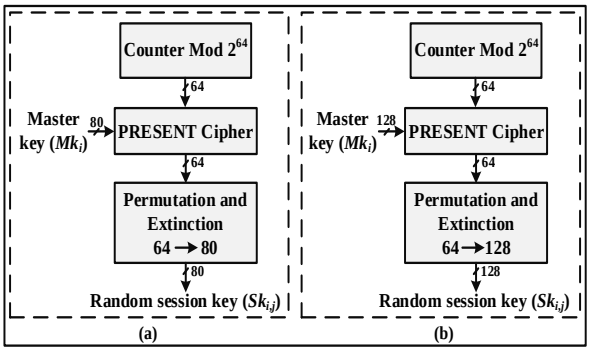


Fig. 1. Random key generation based on the PRESENT cipher for 80-bit key (a) and 128-bit key (b).

A counter with period $N = 2^{64}$ produces input to the encryption as plaintext. This counter is called the modulus counter (MOD counter). It is defined based on the number of states that the counter will sequence through before returning to its original value (0 value). In the random key generation part, a 64-bit counter that counts from 0 to $2^{64} - 1$ in decimal, has a modulus value of $N = 2^{64}$ so would therefore be called a modulo-N, or mod-N, counter. Note also that it has taken N clock cycles to get from 0 to $2^{64} - 1$ values. The session keys are generated from the master keys Km_i as the main key, where i is a natural number and the counter values as plaintexts. It can generate 2^{64} random session keys from each master key. After each session key is produced, the counter is incremented by one. Random key generators based on the PRESENT cipher for 80-bit keys and 128-bit keys are shown in Figs. 1 (a) and (b), respectively.

The hierarchy of key generation from the master key to round keys is summarized in Fig. 2. In this method, we can generate many new master keys by using a secure approach based on the used block cipher in the system. Therefore, the need for the generation of the master keys is simply provided. In brute force attacks, the attacker applies different combinations of keys to hack the system. But this fracture leads to confusion and diffusion. In the PRESENT cipher, the 80- and 128-bit key lengths are to be produced. The proposed procedure of random key generation based on the PRESENT cipher for the 80- and 128-bit key sizes are shown in Algorithms 2 and 3, respectively. In this algorithm, we generate random keys based on PRESENT block cipher as the heart of the process, MOD counter, and expansion/permutation unit. Each of the session key outputs $Sk_{i,j}$ is based on a different counter value and therefore for $i = 1$, we have $Sk_{1,0} \neq Sk_{1,1} \neq Sk_{1,1} \neq \ldots \neq Sk_{1,2^{64}-1}$. It is said that if the cryptographic system (ciphertext) does not have enough details to find plaintext, it is a secure cryptographic system. Because the master key is protected, it is not computable to accurately deduce any of the secret keys through knowledge of one or earlier keys. In this case, the same plaintext can create

Algorithm 1 Random key generation based on PRESENT cipher for 80-bit keys

Input: Counter values Cv_j and the 80-bit master key Mk_i.
Output: Random Session Key $Sk_{i,j}$.
1. **For** i **from** 0 **to** Mkn **do** // The number of Mkn values depends on the number of master keys.
2. **For** j **from** 0 **to** Kn **do** // The maximum value of Kn is $2^{64}-1$.
3. $X = Addkey(Cv_j, Mk_i)$; // Start of the PRESENT encryption.
4. **For** r **from** 2 **to** 32 **do**
5. $Y = S-box(X)$;
6. $W = Permutation(Y)$;
7. $X = Addkey(W, K_r)$; // The K_r are the round keys that are generated from Cv_j by the key scheduling.
8. **End For**;// End of the PRESENT encryption.
9. $Pe = PE_{64\to80}(X)$ // The $PE_{64\to80}(X)$ is permutation and expansion from 64-bit to 80-bit.
10. $Sk_{i,j} = Pe$;
11. **End For**;
12. **End For**;

Algorithm 2 Random key generation based on PRESENT cipher for 128-bit keys

Input: Counter values Cv_j and the 128-bit master key Mk_i.
Output: Random Session Key $Sk_{i,j}$.
1. **For** i **from** 0 **to** Mkn **do** // The number of Mkn values depends on the number of master keys.
2. **For** j **from** 0 **to** Kn **do** // The maximum value of Kn is $2^{64}-1$.
3. $X = Addkey(Cv_j, Mk_i)$; // Start of the PRESENT encryption.
4. **For** r **from** 2 **to** 32 **do**
5. $Y = S-box(X)$;
6. $W = Permutation(Y)$;
7. $X = Addkey(W, K_r)$; // The K_r are the round keys that are generated from Cv_j by the key scheduling.
8. **End For**;// End of the PRESENT encryption.
9. $Pe = PE_{64\to128}(X)$ // The $PE_{64\to128}(X)$ is permutation and expansion from 64-bit to 128-bit.
10. $Sk_{i,j} = Pe$;
11. **End For**;
12. **End For**;

different ciphertexts using random session keys. Fig. 3 shows the generation of different ciphertexts from the same plaintext using random session keys. The plaintext P_0 for master key Mk_0 with session keys $Sk_{0,0}$, $Sk_{0,1}$, $Sk_{0,2}$, ..., $Sk_{0,2^p-1}$ generate the ciphertexts C_0, C_1, C_2, ..., C_{2^p-1}, where p is the size of plaintext. Therefore, brute force attacks will not be able to discover the key.

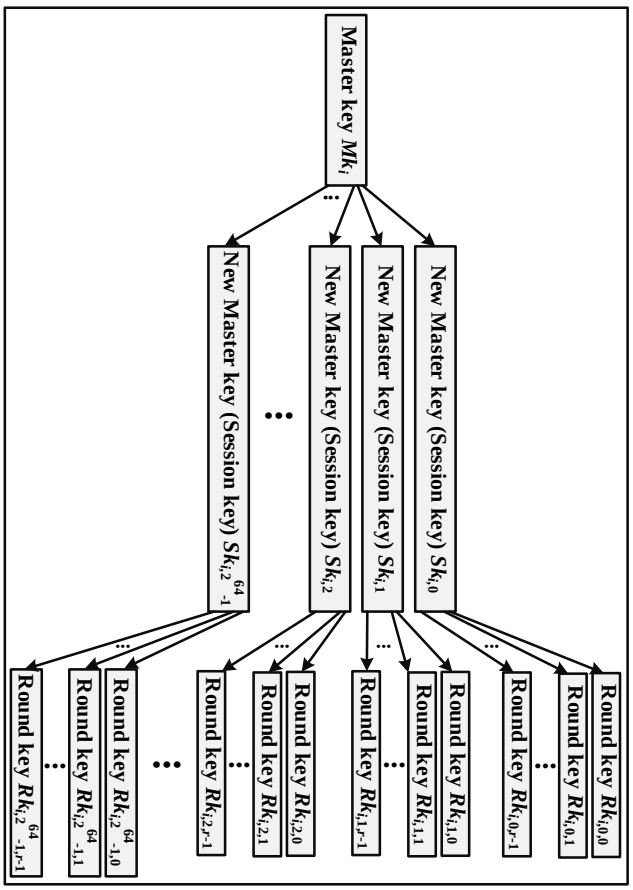


Fig. 2. Hierarchy of key generation from the master key to round keys.

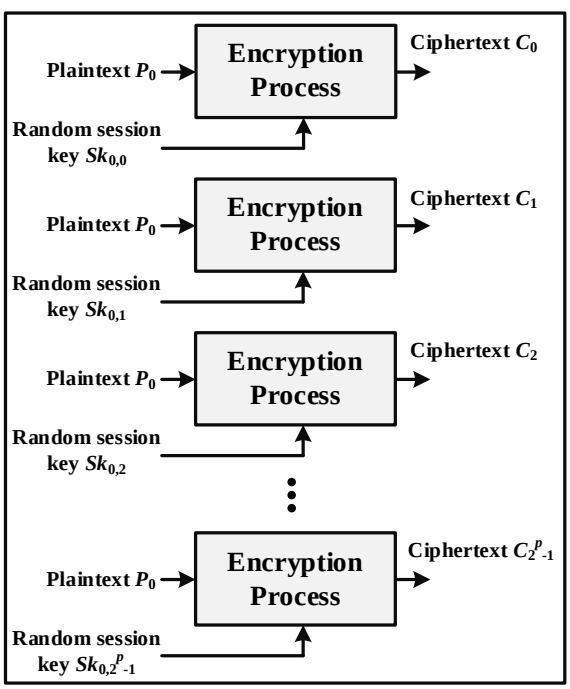


Fig. 3. Generating different ciphertexts from the same plaintext using random session keys.

IV. Proposed Structure of PRESENT Cipher with Random Key Generation

In this section, we present the proposed structure of the PRESENT cipher with random key generation. The reduction of hardware resources for cryptosystems has been achieved in different ways. In the proposed structure, the two methods are used to reduce the hardware resources. These methods include 1- The PRESENT cipher is shared in both random key generation and encryption processes. This property reduces hardware resources. 2- In the PRESENT cipher, to further reduce the logic gates of the 4-bit S-boxes, we applied further simplifications on the expression terms of the S-boxes for more area optimization. Therefore, a low-cost 4-bit S-box for the PRESENT cipher is achieved.

The proposed structure is shown in Fig. 4. The structure is constructed based on round function and key scheduling of PRESENT (includes main blocks such as 16 S-boxes, permutation layer, two registers called Reg $_r$, Reg $_k$), 64-bit counter, permutation and expansion block, and several 2-to-1 multiplexers. This circuit can perform two operating modes (dual-mode circuit). The first mode is the random key generation with RK_ENC='0' and in the second mode encryption operation is performed with RK_ENC='1'. Therefore, in the proposed structure, the PRESENT cipher as the main core is shared between the two modes of the random key generation and the encryption process. In this case, the hardware resource is reduced. We have two procedures for the use of the proposed structure. In the first procedure (Procedure 1) after generating each random session key, we encrypt the input data (plaintext) to generate the ciphertext based on this random session key. In the second procedure (Procedure 2) after generating the all required random session keys and storing these keys in memory we start the encryption process for generating ciphertext based on these stored random session keys.

For generating the first random key, at the first clock cycle, the control signals RK_ENC and Start are set to '0' and '1', respectively, and the first value of the counter (0), as plaintext, and the master key, as the main key, are applied to the structure. In the next clock cycles, the control signal Start is set to '0', and the round computations of the PRESENT are processed. At the end of round computations, the output of register Reg $_r$ (ciphertext) is applied to the permutation and expansion block for generating the first random session key. For producing the second random key, the MOD counter is increased by one and the procedure is similar to the first random key. Also, in the encryption process, at the first clock cycle, the control signals RK_ENC and Start are set to '1'. In this step, in the Procedure 1, the generated random key which is produced in the previous mode (random key generation) is used as a master key for the encryption of plaintext (Procedure 1).

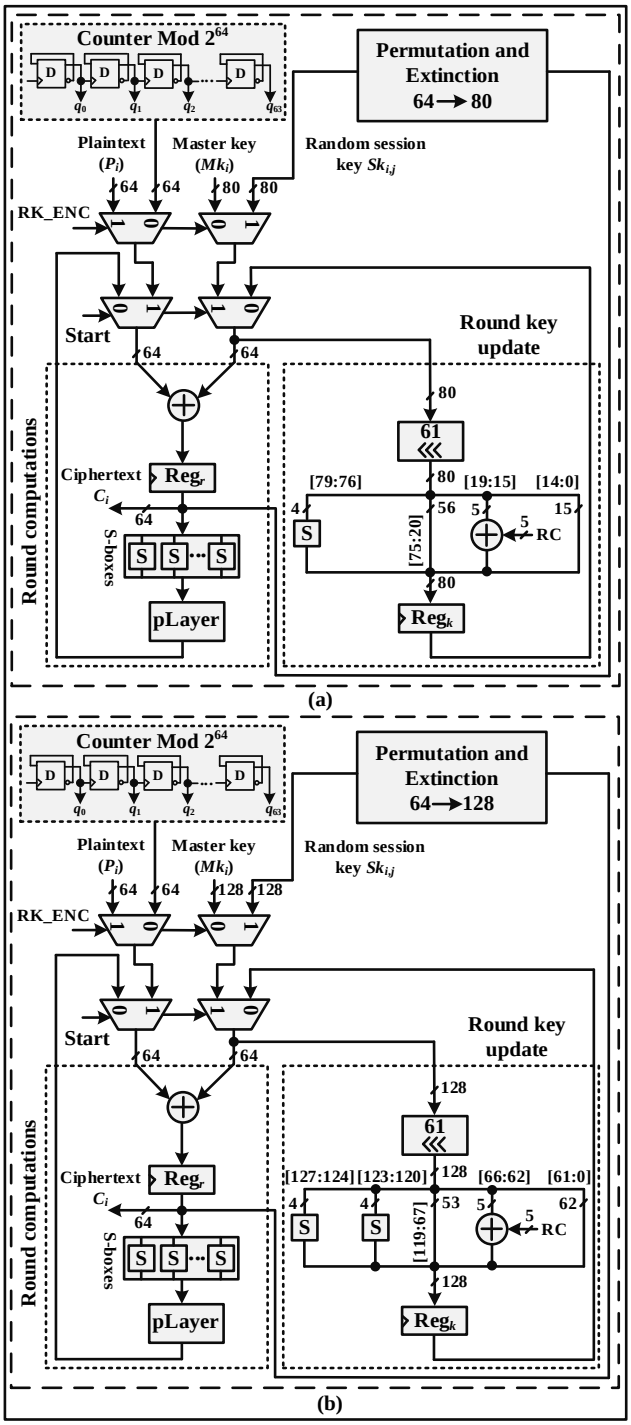


Fig. 4. Proposed structure of PRESENT cipher with random key generation.

After completion of the round computations, the output of register Reg $_r$ is considered as ciphertext. For Procedure 2, the random key (as a master key) can be applied from the memory.

A. Permutation and Expansion

Since the ciphertext in the PRESENT cipher is a 64-bit value and the random session keys that are generated based on the structure have 80- and 128-bit sizes. Therefore, we need the permutation and expansion units for conversion of

TABLE 1: THE BIT PERMUTATION AND EXPANSION $PE_{64\to80}(x)$.

i	0	1	2	3	4	5	6	7
$P(i)$	0	8	16	32	48	1	9	17
i	16	17	18	19	20	21	22	23
$P(i)$	11	19	35	51	4	12	20	36
i	32	33	34	35	36	37	38	39
$P(i)$	22	38	54	7	15	23	39	55
i	48	49	50	51	52	53	54	55
$P(i)$	41	57	10	18	26	42	58	11
i	64	65	66	67	68	69	70	71
$P(i)$	60	13	21	29	45	61	14	22
i	8	9	10	11	12	13	14	15
$P(i)$	33	49	2	10	18	34	50	3
i	24	25	26	27	28	29	30	31
$P(i)$	52	5	13	21	37	53	6	14
i	40	41	42	43	44	45	46	47
$P(i)$	8	16	24	40	56	2	17	25
i	56	57	58	59	60	61	62	63
$P(i)$	19	27	43	59	12	20	28	44
i	72	73	74	75	76	77	78	79
$P(i)$	30	46	62	15	23	31	47	63

64-bit to 80- and 128-bit. The permutation and expansion is an operation for conversion of 64-bit ciphertext of the PRESENT cipher to 80- and 128-bit, for the two key sizes 80- and 128-bit. Therefore, we present two permutation and expansion operations $PE_{64\to80}(x)$ and $PE_{64\to128}(x)$ for the 80- and 128-bit key sizes, respectively. The permutation and expansion operation for 80-bit key size transforms bit x of ciphertext to bit position $PE_{64\to80}(x)$ as follows:

$$PE_{64\to80}(x) = \begin{cases} 0 & x = 0, \\ 8 & x = 1, \\ 16 & x = 2, \\ 32 & x = 3, \\ 64 & x = 4, \\ PE_{64\to80}(x-5)+1 & 5 \le x \le 79. \end{cases} \quad (8)$$

Also, for the generating 128-bit key size, we have the permutation and expansion $PE_{64\to128}(x)$ as follows:

$$PE_{64\to128}(x) = \begin{cases} 0 & x = 0, \\ 12 & x = 1, \\ 18 & x = 2, \\ 24 & x = 3, \\ 30 & x = 4, \\ 36 & x = 5, \\ 42 & x = 6, \\ 48 & x = 7, \\ PE_{64\to128}(x-8)+1 & 8 \le x \le 127. \end{cases} \quad (9)$$

The details of the $PE_{64\to80}(x)$ is given in Table 1.

Proposed structure of 4-bit S-box

The PRESENT S-box compared to other 4-bit S-boxes has a suitable security level for cryptographic applications [24]. In this paper, a low-cost 4-bit S-box for the PRESENT cipher is achieved. The low-cost S-boxes are applicable for area-constrained cryptography applications. It is designed based on a simple combinational logic with acceptable area and delay results. As mentioned before, the main and complex block in the PRESENT cipher is the S-box. It has a key role in the performance of the hardware structure. A low-area approach for the PRESENT S-box is presented in work [25]. The computation of S-box are as follows [25]:

$T_1 = x_2 \oplus x_1,\ T_2 = T_1 x_1,\ T_3 = x_0 \oplus T_2,\ y_3 = x_3 \oplus T_3,\ T_2 = T_1 T_3,\ T_1 = T_1 \oplus Sb_3,\ T_2 = T_2 \oplus x_1,\ T_4 = x_3 + T_2,\ y_2 = T_1 \oplus T_4,\ T_2 = T_2 \oplus x_3,,\ y_0 = y_2 \oplus T_2,\ T_2 = T_2 \oplus T_1,\ y_1 = T_3 \oplus T_2.$

In these equations, the input bits and the output bits are denoted as x_3, x_2, x_1, x_0 and y_3, y_2, y_1, y_0, respectively. In the following, we present an optimized version of these equations:

$$y_3 = x_3 \oplus T_3 = x_3 \oplus x_0 \oplus (x_1(x_2 \oplus x_1)) = x_3 \oplus x_0 \oplus (x_1 x_2,). \quad (10)$$

In the y_2 equation, the terms 1 T_2 and 2 T_1 can be rewritten as follows:

1 $T_2 = (x_2 \oplus x_1)(x_0 \oplus (x_1 x_2,)) \oplus x_1 = ((x_2 x_1, + x_2, x_1)(x_0 \oplus x_1 x_2,) \oplus x_1) + (x_1,(x_0 x_1, x_2 + x_0 x_2 x_1, + x_2, x_1 x_0,)) = x_2 x_1, x_0 + x_1(x_2 + x_0) = x_2(x_0 + x_1) + x_1 x_0.$

2 $T_1 = x_3 \oplus x_2 \oplus x_1 \oplus x_0 \oplus x_1 x_2, = x_3 \oplus x_2 \oplus x_1 x_2 \oplus x_0 = x_3 \oplus x_2 x_1, \oplus x_0.$

In this case, the y_2, y_1, and y_0 equations are present as follows:

$$y_2 = (x_3 + T_2) \oplus T_1 \quad (11)$$

$$y_1 = T_2 \oplus T_1 \oplus x_0 \oplus x_1 x_2 \quad (12)$$

$$y_0 = y_2 \oplus T_2 \oplus x_3 \quad (13)$$

The proposed structure of the PRESENT S-box is shown in Fig. 5. The S-box is implemented using 7 XOR, 3 AND, 4 OR, and 2 NOT gates. Therefore, it is implemented by only 16 logic gates. The critical path delay of the S-box in the structure is equal to $4T_X$, where T_X is the time delay of the 2-input XOR gate. Table 2 shows the results of the proposed structure and other works. The area and delay of

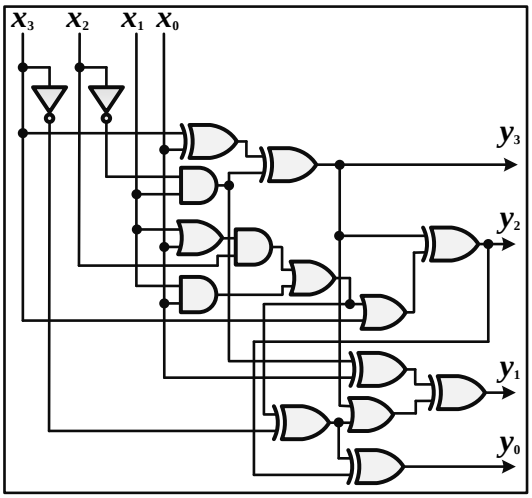


Fig. 5. Optimized structure of 4-bit S-box in the PRESENT cipher.

TABLE 2: RESULTS OF THE PRESENT S-BOX FOR THE PROPOSED STRUCTURE AND OTHER WORKS.

Works	# AND (OR OR)	# NAND (or NOR)	# XOR (or XNOR)	CPD
[26]	43	—	—	$2T_A+3T_O$
[11]	20	—	7	$T_X+T_A+2T_O$
[12]	2	1	10	$6T_X+2T_A$
[13]	39	8NOT	—	$3T_O+T_A+T_N$
[14]	7+8AND3	—	23	$7T_X+3T_A+2T_{A3}$
[15]	28	—	10	$T_X+T_A+3T_O$
TW	7	—	7	$4T_X$

TW: This work; CPD: Critical path delay; T_X, T_A, T_O, T_{A3} are the time delay of the 2-input XOR gate, 2-input AND gate, 2-input OR gate, and 3-input AND gate, respectively.

PRESENT S-box for this work and recent work [12] are equal to (22 GEs and 0.56 ns) and (24 GEs and 1.086 ns), respectively, using Synopsys Design Compiler with 180 nm CMOS technology. As seen from this table, the proposed method has acceptable area and delay parameters.

B. Application of the proposed structure

The proposed structure is more suitable for the encryption of a large amount of digital data. The application domains for the proposed structure of key generation for the PRESENT cipher include image encryption (medical images, industrial images, fingerprint images, ...), voice encryption, and any area that needs to be protected from security breaches. In recent years, more digital images have been transmitted through networks, and most of them have to be transmitted through public networks. To transmit hidden digital images to receivers, digital image encryption technology must be used. Over the past decades, many image encryption algorithms have been proposed [3]. The

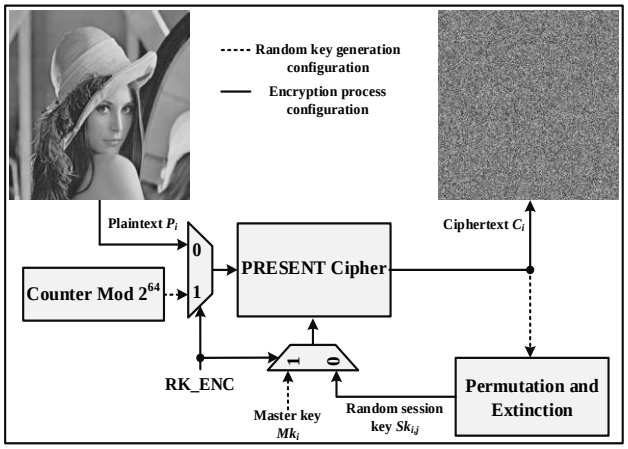


Fig. 6. Configuration of the proposed structure for image encryption.

configuration of the proposed structure for image encryption is shown in Fig. 6. As mentioned before, the system has two configurations including random key generation and encryption process, which are controlled based on the control signal RK_ENC. For data encryption, it is necessary to generate many random session keys, so the proposed structure is suitable for cryptographic applications with a high number of data.

V. Security of the Proposed Structure

The protection of private keys is crucial in private key cryptography, as any disclosure of these keys can be used to decrypt secret messages. To improve the security of private keys, we propose a key generation algorithm that generates the random private key of a user that meets the current security requirements of any private key algorithm. In the proposed structure, the required private random keys are generated by the system itself. This eliminates the system's need to achieve the keys from outside. This protects the produced keys. This is while the previous implementations have not the key generation unit and require receiving the key from outside the system, which reduces the security of the keys.

The main focus of this work is the design and implementation of a lightweight structure of random key generation for the PRESENT block cipher. However, we analyze the security of structures from a hardware point of view. Side-channel attacks are the biggest threats to the security of cryptographic algorithms. These attacks are used to recover sensitive data such as the main key and plaintext. Side-channel attacks on cryptographic devices are non-invasive passive attacks that use certain physical information leaked during normal encryption such as power consumption [27], time delay [28], or electromagnetic radiation [29] to find the secret key. Simple Power Analysis is a method that interprets power consumption

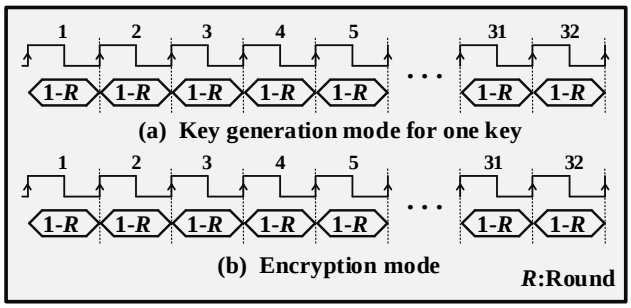


Fig. 7. The computations of key generation mode (a) and encryption mode (b) at each clock cycle.

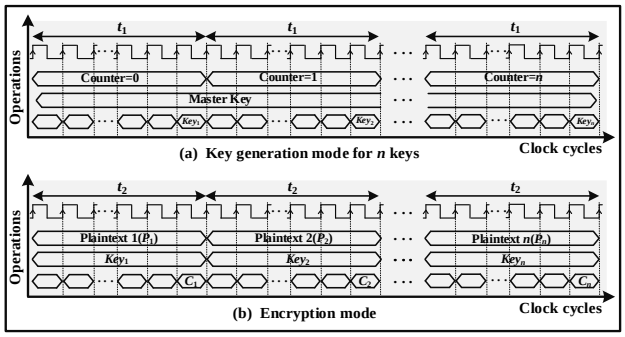


Fig. 8. Waveform of the proposed structure for the computation of key generation and encryption of the plaintexts with the same execution time (t_1=t_2).

measurements during cryptographic operations. It can achieve information about a device's operation as well as the secret key (or plaintext) based on a power trace.

A. Power analysis of the proposed hardware structures

In the proposed structures, at each clock cycle, we have the computation of operations with a similar hardware complexity. In this case, the power consumption at each clock cycle is almost constant. In the proposed structures, the same operations are performed at each clock cycle. For example, at each clock cycle, for both the key generation mode and the encryption mode, we have the computation of a round of the PRESENT cipher. In each round, the computation of S-boxes and permutation layer is performed. Figs. 7 (a) and (b) show the computations of key generation mode and encryption mode, respectively, at each clock cycle. As seen from these figures, at each clock cycle the computations are similar (one round (1-R) at one clock cycle). In this case, the power consumption at each clock cycle is fixed. Therefore, this feature leads to a unified power trace in total clock cycles and the power traces are independent of the key and plaintext message patterns.

B. Power analysis of the proposed hardware structures

The timing attack is another important side-channel attack. In this attack, the time taken to execute a key generation or encryption of plaintext is measured precisely by the attacker [28]. If the execution time for different plaintexts is different, this will lead to the attacker obtaining information about the bit-pattern of a plaintext. Therefore, the implementation of the algorithm must reduce data-dependent timing information. The computation time for each key generation operation or encryption of a plaintext in the proposed structure is fixed. In this case, the structures leak no information about the bit-pattern of the plaintext (or key) bit-pattern. The computation of a random key and encryption of a plaintext takes the same time t_1 and t_2, respectively. Fig. 8 shows the waveform of the proposed structure for a random key and encryption of a plaintext. As seen in this figure, a random key generation takes the same time t_1, and also the encryption of a plaintext takes the same time t_2. On the other hand, because both computations are implemented based on PRESENT cipher, so the time t_1 and t_2 are equal. Therefore, the computation time of the proposed architecture is independent of the key and plaintext being manipulated. In this case, the details of the internal computations of the key generation and plaintext algorithms are hidden.

VI. Results and Comparison

The hardware complexity of the proposed structure of the PRESENT cipher with random key generation and other works are compared in this section. We use the Synopsys Design Compiler tool based on the library of standard cells with 180 nm CMOS technology to achieve the ASIC results. The area and critical path delay, number of clock cycles, throughput, and throughput/area ratio parameters are used for the evaluation of performance. The performance evaluation in terms of throughput/area is useful, where both the constraints of throughput and area are required to be fulfilled at the same time in many cryptographic applications. Table 3 shows the hardware results for the proposed structure and other implementations of the PRESENT cipher. In the other works, available in the literature, only the PRESENT cipher is implemented and the previous structures lack a random key generation unit. But in the proposed work, we have implemented the PRESENT cipher with a random key generation unit. Therefore, this property must be considered in the comparison. Because, in the proposed structure, the parameters such as the number of clock cycles (CCs), time, and throughput are computed for the generation of a random key and data encryption (in other words, it is assumed that a random key is first generated, and subsequently, a plaintext is encrypted using this key to produce ciphertext). But in the other works, these parameters are computed for only data encryption without the random key generation.

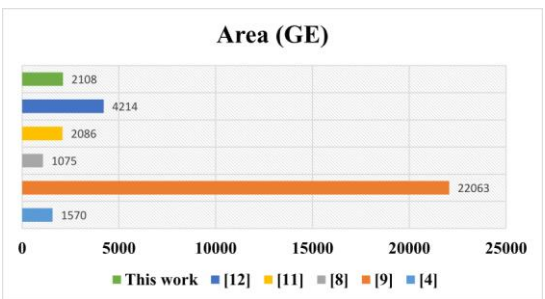
In work [8] three structures of the PRESENT consisting of pipelined structure, serial structure, and round structure are proposed. Between these structures, the pipelined structure has the most area compared to the other structures. The serial structure is the slowest compared to the other

TABLE 3: RESULTS OF THE PROPOSED IMPLEMENTATION AND OTHER WORKS ON THE .PRESENT CIPHER.

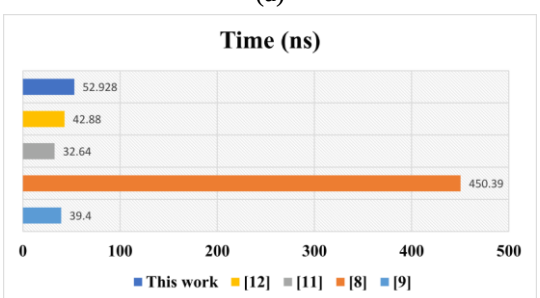
Works	TECHNOLOGY	Area (GE)	#CCs	CPD (ns)	Time (ns)	Thr. (Mbps)	Thr./Area Mbps/GE
[4] K-128	180 nm	1886	—	—	—	—	—
[4] K-80	180 nm	1570	—	—	—	—	—
[9] K-128	180 nm	23005.75	1	38.10	38.10	1,570	0.068
[9] K-80	180 nm	22063.50	1	39.40	39.40	1,510	0.068
[8] S K-80	180 nm	1075	563	0.80	450.39	142.10	0.132
[8] S1 K-128	180 nm	2989	40	3.09	120.98	529	0.177
[8] S2 K-128	180 nm	2900	63	2.83	178.27	359	0.124
[7] S K-128	180 nm	1296	563	2.89	1,627.07	39.33	0.030
[11] K-128, UF=1	180 nm	2305.75	32	1.02	32.64	1,961	0.851
[11] K-80, UF=1	180 nm	2086.30	32	1.02	32.64	1,961	0.940
[12] K-64	180 nm	4214	32	1.34	42.88	1492.54	0.354
[12] K-128	180 nm	4214	32	1.34	42.88	1492.54	0.354
[16] K-64	180 nm	1098	622	—	—	—	—
[16] K-128	180 nm	1879	250	—	—	—	—
TW, K-80	180 nm	2108	64	0.827	52.928	1,209	0.574
TW, K-128	180 nm	2583	64	0.827	52.928	1,209	0.468

TW: This work; S:Serial; GE: Gate equivalents; UF: Unroll factor; K: Keys; CCs: Clock cycles; Thr.: Throughput.

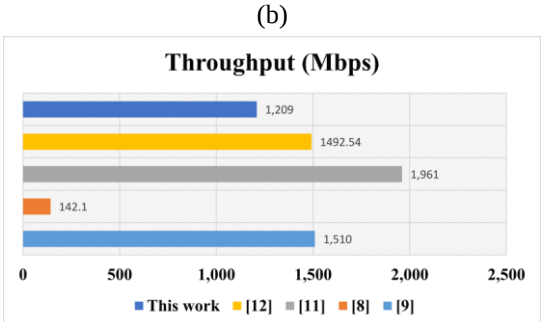
structures. The PRESENT algorithm is implemented based on a Single-cycle structure in work [9]. An optimized circuit for the S-box is presented in work [10]. In work [11] a low latency and high throughput structure of the PRESENT is proposed based on the loop unrolling technique. Also, the S-box is implemented based on a low-area circuit. In work [12] both key sizes 80- and 128-bit are supported based on a high-throughput and flexible hardware structure of the PRESENT algorithm for IoT applications. As seen from the table, the proposed structure has a reasonable implementation cost. This structure can be a good candidate for image encryption with low area consumption and an acceptable security level. We implemented the proposed structure with the 80-bit key, which resulted in 2108 gates with a throughput/area of 0.574 Mbps/GE. This corresponds to 2583 gates with a maximum delay of 0.468 Mbps/GE for the 128-bit key. Figs. 9 (a), (b), (c), and (d) show column diagrams of the area, execution time, throughput, and throughput/area, respectively, for the proposed structure and other works for 80-bit key size. Also, for the case key size of 128-bit, these parameters are shown in Fig. 10. Based on the hardware results, we get acceptable improvement in terms of throughput/area for the PRESENT block cipher with key generation unit.



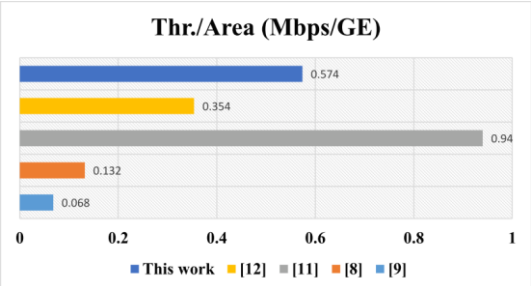
(a)



(b)

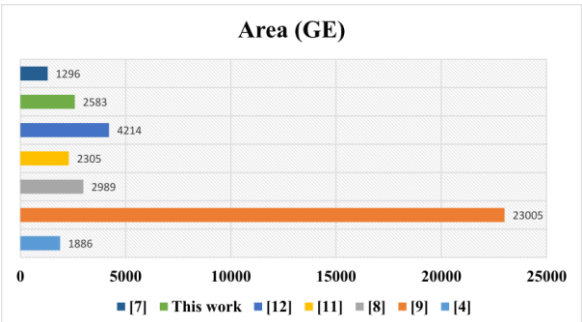


(c)

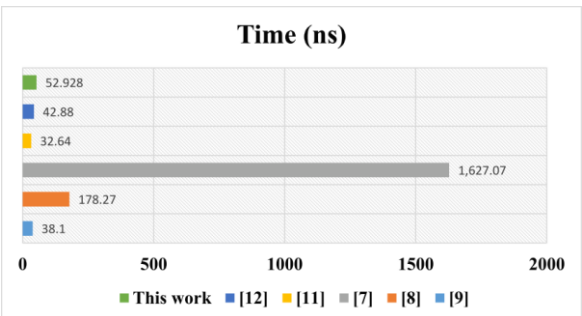


(d)

Fig. 9. Column diagrams of the Area (a), Time (b), Throughput (c), Throughput / Area (d) for the proposed structure and other works for 80-bit key size.



(a)



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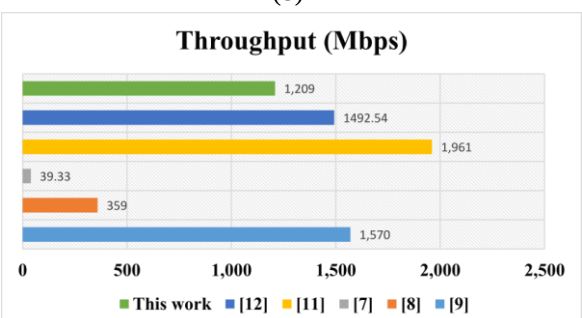
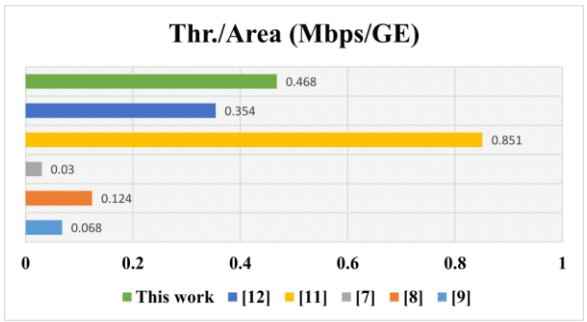


(c)



(d)

Fig. 10. Column diagrams of the Area (a), Time (b), Throughput (c), Throughput / Area (d) for the proposed structure and other works for 128-bit key size.

VII. Conclusions

One of the important issues in many block ciphers is random key generation, especially in the encryption of a high number of digital signals. The use of random keys will overcome the brute force attack that can be applied to a block cipher. In this paper, we design a hardware structure of a modified random key generation for lightweight PRESENT block cipher which is applicable in encryption of the digital signal. In this work, a master key is used to derive the new random master keys (random session keys) and use these keys for the encryption processing. We take advantage of the block cipher to produce random keys. The proposed structure has both random key generation and data encryption in a unified circuit. Therefore, the PRESENT cipher is shared in both random key generation and encryption process. This feature reduces hardware resources. The implementation results, in 180 nm CMOS technologies, show the proposed structure has a suitable area and throughput compared to other works.

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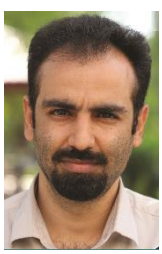

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Sliding Mode Control for Chaotic Systems with Unknown Uncertainties

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ABSTRACT

Objective: In this article, time-varying chaotic systems with uncertainties, including external disturbances, are considered, and sliding mode control (SMC) is used to control such systems. To control these systems, an autonomous differential equation is first introduced. Then, based on this differential equation, a sliding surface is defined to control this chaotic system. This kind of controller is remarkable in that it removes the effects of disturbances, whether bounded or unbounded. Therefore, the system is known to be fixed-time stable. Where the trajectories of this chaotic system are not placed on the sliding surface, we have created creative controllers to place the trajectories on the sliding surface in finite time. Theoretical investigations show that such chaotic systems can be made fixed-time stable by applying the controls proposed in this study. Based on the findings of this study, the controllers are designed to eliminate all disturbances, whether bounded or unbounded. The results can be said to apply to chaotic, time-dependent, and time-independent systems. To further consolidate the results obtained in this article, two examples, namely the time-dependent system of the Gyro and the time-independent system of the Liu, are investigated, and the results were compared with previous works by other researchers.

I. Introduction

Chaos theory is an interdisciplinary scientific study and a branch of mathematics concerned with the underlying patterns and deterministic principles of dynamical systems that are very sensitive to the initial circumstances and were previously assumed to have fully random states of disorder and irregularity [1]. The butterfly effect is a term used in chaos theory to describe this occurrence. It is a simile used to describe how a butterfly may behave in Brazil while flapping its wings under specific conditions, which might then result in a storm in Texas [2]. As a result, it is not imaginable to forecast how these systems will behave in the long run. Although it can be assumed that random dynamics act chaotically, deterministic dynamic systems may also exhibit chaos, demonstrating that chaos need not be the result of an accidental element [3, 4]. It can be shown that chaotic behavior in continuous dynamical systems requires at least three variables. Chaotic movement is a frequent and acceptable nonlinear event that has lately gained increased attention due to its various uses. Some of its industrial applications include data processing, secure telecommunication systems, electrical converters, and chemical processes [5-8]. Since the early 1990s, ample research has been done on how to regulate chaos in the chaotic systems [9]. As a result, a number of researchers have now developed numerous strategies to combat the chaotic behavior in such dynamic systems. Here, we mention several papers. In [10], barrier function-based SMC approaches were used. In [11], stochastic delay methods were applied. In [12, 13], intelligent control methods based on neural networks were handled. In [14], the problem was challenged by using linear

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matrix inequalities. In [15, 16], to control such dynamic systems, sliding mode control (SMC) was introduced. In [17, 18], backstepping control was convincingly used. In [19, 20], adaptive control provided an effective solution. In [21, 22], the optimal control method has provided an efficient solution to the chaotic behavior of such systems. In [23, 24], the backstepping method, as a common method, was used for such chaotic systems. Among the control techniques mentioned above, sliding mode control has been successfully applied in a number of applications to enhance controller performance and address issues including immeasurable modes, input saturation, and others. It is a practical and effective method for dealing with the issue of uncertainty in nonlinear systems [25, 26]. However, simple adaptive control cannot be used to precisely regulate a nonlinear dynamical system with unknown model uncertainties. Additionally, the sliding mode control approach is a reliable and effective tool for engineering study of high-order nonlinear systems, both theoretically and practically. Among the existing control strategies, the SMC is a reliable and successful way for chaos control in chaotic systems [25]. However, the chattering problem, which occurs because the sign function of control input signal is discontinuous, affects the majority of typical SMC techniques. Recently in [26] , the undesirable chattering assumption was eliminated using an innovative chattering-free SMC technique. The design was developed with the hypothesis that the first derivatives and upper bounds of the uncertainty term are known. Unknown upper bounds for the uncertainty and its derivatives have not been studied in this case. SMC methods are frequently used in industrial settings. In [27], some new developments in SMC for networked control systems (NCSs) were investigated. First, a few innovative SMC methods to address NCSs with time delays, uncertainty, and disturbances are briefly described. Next, the issue of SMC for NCSs was covered. A SMC approach is also suggested in [28] for nonlinear systems with time delays and undetermined missing probability. The study by [29] examined nonlinear fractional systems with external disturbances and uncertainties. Using an appropriate sliding surface, they introduced a method for investigating and evaluating stability. They created a robust adaptive fractional sliding mode controller in response to the external disturbances and an unknown upper bound on uncertainties. The study of chaotic dynamics in environmental phenomena was addressed in article [30]. For this fractional-order system, they derived two distinct sliding-mode controllers to manage chaos. They created a new controlled system of equations both with and without uncertainties through this process. Additionally, the new systems' global stability is established. The study by [31] investigated chaos in the Bloch equation. In this work, the Bloch equation with and without delay was studied in relation to the Caputo fractional derivative. They explored the underlying chaos using a sliding-mode controller. The effectiveness of the controller was monitored in the presence of external disturbances and uncertainty.

In most of the studies reported in this paper, the researchers considered common sliding surfaces and then tried to put the trajectories of chaotic dynamic systems on this surface with complicated and challenging techniques. However, the present study presents an innovative sliding surface and controllers that disregard the boundedness of uncertainty and system disturbances in order to solve the upper bounds of unknown uncertainty.

The most significant contributions of the study are as follows:

- It develops a fixed-time controller for the stabilization of chaotic systems, utilizing an innovative sliding-mode surface.
- It offers a technique for establishing a limit on chaotic systems' fixed-time stability. without depending on the starting circumstances.
- It creates controllers without taking into account system disturbances and the uncertainty bound.

The rest of this article is divided into the following sections: A few explanations and definitions are provided in Section 2; the controller structure is both defined and formulated in Section 3; to demonstrate the effectiveness of the suggested control mechanism, simulation results are shown in Section 4; finally, some conclusions are reached in Section 5.

II. Preliminaries and system description

Nonlinear chaotic systems have a dynamic equation that is often expressed as follows:

$$\dot{x} = f(t,x) + d(t,x) + u(t). \tag{1}$$

where $x = [x_1, x_2, \cdots, x_n]^T \in R$ represents the system state vector, $f(t,x)\colon R^+ \times R^n \to R^n$ indicates a nonlinear function, $d(t,x)\colon R^+ \times R^n \to R^n$ is the unknown uncertainty term that denotes model uncertainties mixed by unknown external disturbances and system unmodeled dynamics, and $u(t) \in R^n$ is the control signal. The number of control signals u and the number of state variables are assumed to be equal in the chaotic system equation (1).

Definition 1 [32]**:** An autonomous dynamic equation:

$$f\colon R^n \to R^n, \quad \dot{x}(t) = f\big(x(t)\big), \quad x(0) = x_0. \tag{2}$$

is said to be fixed-time stable if

$$\exists\, t_* \ \forall\, t > t_*\,; \|x(t) = 0\| \ \wedge \ \lim_{t \to t_*} \|x(t)\| = 0. \tag{3}$$

t_* is independent of the initial value of the autonomous differential equation.

Remark 1: In this definition, if we consider the dynamic system as $\dot{x}(t) = f\big(t\,, x(t)\big)$, the concept of fixed-time stability is described in a similar way.

The goal of this article is to develop a sliding surface and controllers for chaotic systems with model uncertainties combined with unidentified external perturbations in order to establish closed-loop systems that are fixed-time stable for any

initial conditions. It indicates that the system's trajectory converges to the origin in a limited amount of time, irrespective of the initial conditions.

Remark 2: It should be noted that system (1) simply turns into this dynamical system:

$$\begin{cases} \dot{x}_1 = f_1(t\,,x) + d_1(t\,,x) + u_1(t), \\ \dot{x}_2 = f_2(t\,,x) + d_2(t\,,x) + u_2(t), \\ \vdots \\ \dot{x}_n = f_n(t\,,x) + d_n(t\,,x) + u_n(t). \end{cases} \tag{4}$$

Lemma 1: Suppose that $K > 0\,, M > 0$ and $x : R \to R$ is a continuous function. If there exists a function $F(x)$ such that:

$$\dot{x} = -K\,F(x). \tag{5}$$

And

$$\forall\, a, b \in R\,, \qquad \left| \int_a^b \frac{dx}{F(x)} \right| < M. \tag{6}$$

then the autonomous differential equation (5) is fixed-time stable and $t_* < \frac{M}{K}$.

Proof: The result of equation (5) is:

$$\frac{dx}{F(x)} = -K\,dt. \tag{7}$$

upon careful evaluation of equation (7), it becomes apparent that:

$$\int_{x(0)}^{x(t)} \frac{dx}{F(x)} = -K \int_0^t d\tau. \tag{8}$$

therefore, it is obtained:

$$\int_{x(0)}^{x(t)} \frac{dx}{F(x)} = -Kt. \tag{9}$$

however, $\forall\, a, b \in R\,,\ \left| \int_a^b \frac{dx}{F(x)} \right| < M$, thus:

$$\left| \int_{x(0)}^{x(t)} \frac{dx}{F(x)} \right| = |-Kt| < M. \tag{10}$$

this gives the result $|t| < \frac{M}{K}$, hence the autonomous differential equation (5) is fixed-time stable and $t_* < \frac{M}{K}$. ■

Corollary 1 [33]**:** Suppose that $K > 0$:

$$A(x) = sign(x)(|x| + 1)\sqrt{(|x| + 1)^2 - 1}. \tag{11}$$

and $x: R \to R$ is a continuous differentiable function that satisfies the following conditions:

$$\dot{x} = -K\,A(x)\ , \quad x(0) = x_0. \tag{12}$$

then the system (12) is fixed-time stable and setting time is $t_* \le \frac{\pi}{K}$.

Fig. 1 shows that if we take $K = 2$ and $x(0) = 5$, the setting time for the solution curve of (12) is $t_* \le \frac{\pi}{2}$. Also, if we take $K = \frac{1}{2}$ and $x(0) = -7$, the setting time for the solution curve of (12) is $t_* \le 2\pi$.

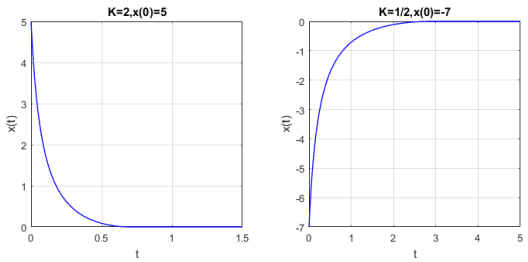

Fig. 1. solution curve for (12)

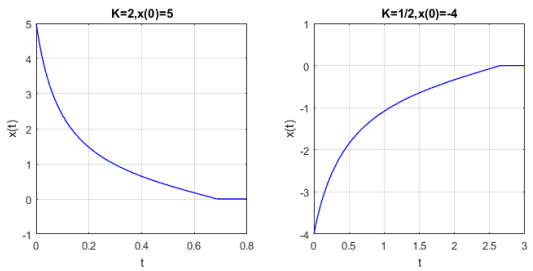

Fig. 2. Solution curves for (14)

Corollary 2: Suppose that:

$$K > 0\ ,\ B(x) = sign(x)\,(x^2 + 1). \tag{13}$$

and $x: R \to R$ is a continuous differentiable function that satisfies the following conditions:

$$\dot{x} = -K\,B(x)\ ,\ \ x(0) = x_0. \tag{14}$$

then the system (14) is fixed-time stable and setting time is $t \le \frac{\pi}{2K}$.

Proof: Assume that $F(x) = B(x)$ thus:

$$\int_{x(0)}^{x(t)} \frac{dx}{F(x)} = \int_{x(0)}^{x(t)} \frac{dx}{sign(x)(x^2 + 1)}. \tag{15}$$

therefore, it is obtained:

$$\int_{x(0)}^{x(t)} \frac{dx}{F(x)} = \frac{tan^{-1}(x)}{sign(x)}\Big|_{x(0)}^{x(t)} = -Kt. \tag{16}$$

however, for any θ , $|\,tan^{-1}(\theta)| < \frac{\pi}{2}$. Lemma 1 concluded that $t < \frac{\pi}{2K}$, hence the autonomous differential equation (14) is fixed-time stable and $t_* < \frac{\pi}{2K}$. ■

Fig. 2 shows that if we take $K = 2$ and $x(0) = 5$, the setting time for the solution curve of (14) is $t_* \le \frac{\pi}{4}$. Also, if we take $K = \frac{1}{2}$ and $x(0) = -4$, the setting time for the solution curve of (14) is $t_* \le \pi$.

III. Controller design by SMC

SMC is employed in the suggested control strategy to address the model uncertainties of the chaos system.

Remark 3: The system uncertainty terms $d_i(t\,,x)$ are assumed to be bounded in article [34], but this article does not make that same assumption.

A novel sliding mode controller is created for this part in order to provide fixed-time stable control over a nonlinear system. Two major steps are involved in the design of the proposed fixed-time controller:

- Constructing an appropriate sliding surface.
- Establishing an effective fixed-time control of the sliding motion within a specified setting time.

The nonlinear sliding mode is constructed in the following way to achieve system control (4) :

$$K > 0, \qquad s_i = x_i + \int_0^t K\, F(x_i). \tag{17}$$

It is clear that $s_i = 0$, $\dot{s}_i = 0$ if the system's trajectories are on the sliding surface.

Theorem 1: Assume that the sliding surface is dynamic (17). In the case where $s_i = 0$, the system is fixed-time stable, and the setting time T_1, is specified $T_1 \le \frac{\pi}{K}$ if $F(x) = A(x)$, or $T_1 \le \frac{\pi}{2K}$ if $F(x) = B(x)$. Its trajectories converge to the equilibrium $x_i(t) = 0$.

Proof: Assuming $s_i = 0$ and $\dot{s}_i = 0$, therefore $\dot{x}_i = -K\, F(x_i)$, Lemma 1 shows the theorem's validity. As a result, $x_i(t)$ converges to the origin, and the setting time T_1 is given $T_1 \le \frac{\pi}{K}$ according to corollary 1 or $T_1 \le \frac{\pi}{2K}$ according to corollary 2.

If $s_i \neq 0$, which indicates that the trajectories of system (4) are outside of the sliding surface, then we should construct a suitable controller to bring the trajectories into the sliding surface and maintain them there continuously. To reach this objective, the following theorem is offered:

Theorem 2: Assume that $K > 0$:

$$u_i(t) = \xi_i - K\, F(x_i) - f_i(t\,, x) - d_i(t\,, x). \tag{18}$$

With

$$\xi_i = -K\, F(s_i). \tag{19}$$

if the trajectories of system (4) are outside of the sliding surface, then the controller (18) brings the trajectories into the sliding surface. And reaching time T_2 is given $T_2 \le \frac{\pi}{K}$ according to corollary 1, $T_2 \le \frac{\pi}{2K}$ according to corollary 2.

Proof: It follows from calculation $\dot{s}_i$:

$$\begin{aligned} \dot{s}_i &= \dot{x}_i + K\, F(x_i), \\ &= f_i(t\,, x) + d_i(t\,, x) + u_i(t) + K\, F(x_i), \\ &= -K\, F(s_i). \end{aligned} \tag{20}$$

thus $\dot{s}_i = -K\, F(s_i)$, Lemma 1 proves the correctness of the theorem 2. As a result, s_i is fixed-time stable, and the setting time T_2 is determined by $T_2 \le \frac{\pi}{K}$ according to corollary 1 or $T_2 \le \frac{\pi}{2K}$ according to corollary 2.

Theorem 3: The state variables of the controlled system (4) can be stabilized into the origin fixed-timely if the controller $u_i(t)$ is defined as (18). The whole process time, T_3 is predicted by $T_3 \le T_1 + T_2$.

Proof: The conclusion of Theorem 3 is clear in light of Theorems 1–2.

Remark 4: The determination of fixed-time stability depends on the existence of a differential equation $\dot{x} = -K\, F(x)$ satisfying the conditions of Lemma 1. Furthermore, the initial conditions and the system characteristics had no effect on the control structure in this investigation. The method described here might be applicable to more kinds of chaotic dynamics.

IV. Numerical simulation

We executed two numerical simulations of the Gyro system and Liu's uncertain chaotic system in order to demonstrate how effectively the suggested technique performed in these two systems.

Example 1: The time-dependent Gyro system is investigated from the viewpoint put out in this article. Gyro system dynamics are described by:

$$f(t,x) = \begin{bmatrix} x_2 \\ b_1 x_2 + b_2 x_2^3 + g(x_1,t) \end{bmatrix}. \tag{21}$$

$$g(x_1,t) = b_3 \sin(x_1) - b_4^2 \frac{\left(1 - cos(x_1)\right)^2}{sin^3(x_1)} + F sin(\omega t) sin(x_1).$$

$$d(t\,,x) = \begin{bmatrix} 1 + sin(x_2) cos(2x_1) \\ sin(x_1) \end{bmatrix}.$$

equation (21) can be considered as follows:

$$\begin{cases} \dot{x}_1 = x_2, \\ \dot{x}_2 = b_1 x_2 + b_2 x_2^3 + g(x_1,t). \end{cases} \tag{22}$$

In [35], the dynamics of (22) were studied. Specifically, the system (22) with the parameters defined by the equations $b_1 = 0.5, b_2 = 0.05, b_3 = 1, b_4 = 10, F = 35, \omega = 2$ can behave chaotically. In Fig. 3 and Fig. 4, the chaos movement of the equation (22) with $x(0) = (-1,3)$ is depicted.

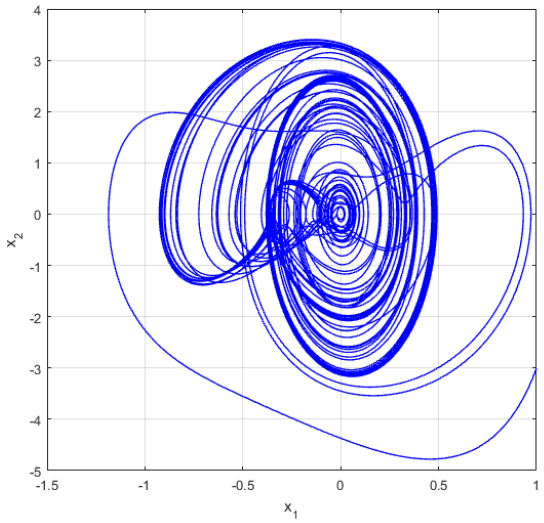

Fig. 3. The chaotic attractor of (22) with $x(0) = (-1,3)$

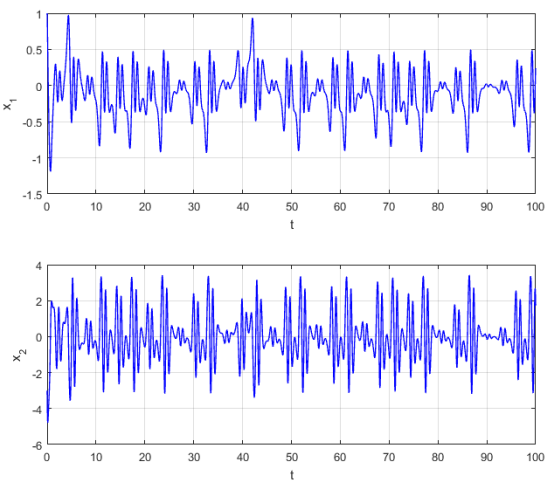

Fig. 4. $x_1(t)$, $x_2(t)$ of system (22)

Control over the chaotic system (22) is given by:

$$\begin{aligned} u_1(t) &= \xi_1 - KF(x_1) - x_2 - d_1(t,x), \\ u_2(t) &= \xi_2 - KF(x_2) - b_1 x_2 - b_2 x_2^3 - g(x_1,t) - d_2(t,x). \end{aligned} \tag{23}$$

That $\xi_1 = -KF(s_1), \xi_2 = -KF(s_2)$, $d_1(t,x) = 1 + \sin(x_2)cos(2x_1)$, $d_2(t,x) = sin(x_1)$ are the uncertainties. It can be observed that in (23), controllers $u_1(t), u_2(t)$ are designed to remove the effects of uncertainties $d_1(t,x), d_2(t,x)$, whether they are bounded or unbounded. Based on the discussed results, we design efficient controllers such that (24) is fixed-time stable.

$$\begin{cases} \dot{x}_1 = x_2 + d_1(t,x) + u_1(t), \\ \dot{x}_2 = b_1 x_2 + b_2 x_2^3 + g(x_1,t) + d_2(t,x) + u_2(t), \end{cases} \tag{24}$$

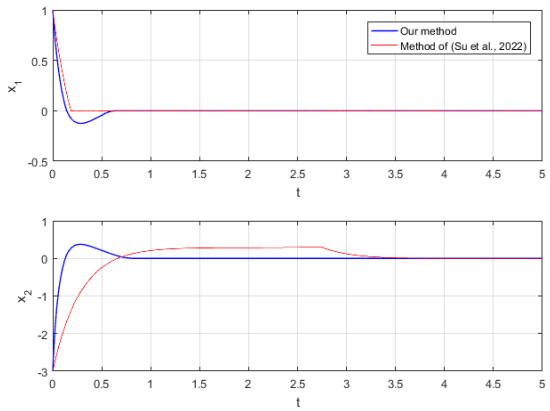

Fig. 5. With assumption $F(x) = A(x)$ and $K= 1$, comparing our method with the method of article [32]

TABLE 1: EVALUTION OF RESULTS

Method	*t*	0	1	2	3	4	5
Our method	x_1	1	-2.8121e-19	-2.8121e-19	-2.8121e-19	-2.8121e-19	-2.8121e-19
	x_2	-3	-2.8121e-19	-2.8121e-19	-2.8121e-19	-2.8121e-19	-2.8121e-19
Method of Ref [32]	x_1	1	9.6686e-5	1.4082e-5	1.7498e-4	1.4867e-4	1.4312e-4
	x_2	-3	0.2085	0.2856	0.1211	6.2350e-4	1.2743e-5

Remark 5: The numerical simulations conducted in the Simulink environment demonstrate that the suggested method is more effective than the one suggested in [32]. Fig. 5 displays the controlled system's trajectories.

Table 1 demonstrates that x_1 and x_2 converge to zero using our strategy in less than a second. However, the convergence happens after three seconds in the technique suggested in [32]. Fig. 5 also reveals that x_1 and x_2 converge to zero in less than a second. However, the convergence occurs after three seconds in the method suggested in [32].

Example 2: In this part, the Simulink environment is used to assess the performance of the recommended method. Consider the Liu system [34], starting with the dynamic equation given below:

$$f(x) = \begin{bmatrix} -10x_1 + 10x_2 \\ -40x_1 + x_1 x_3 \\ 4x_1^2 - 2.5x_3 \end{bmatrix}. \tag{25}$$

$$d(t,x) = \begin{bmatrix} sin(x_1) \\ sin(t) \\ sin(x_1) + sin(t) \end{bmatrix}. \tag{26}$$

The dynamical system can be considered as follows:

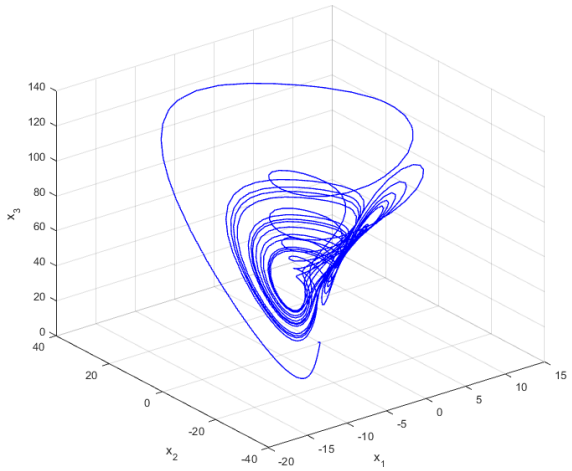

Fig. 6. The chaotic attractor of (27)

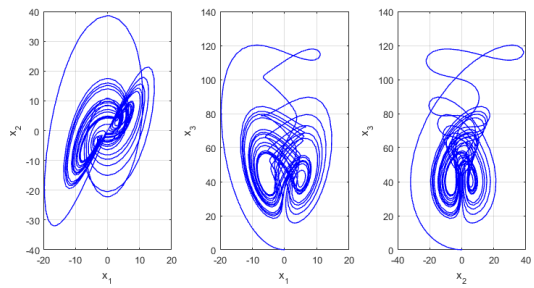

Fig. 7. The phase diagrams of states (27)

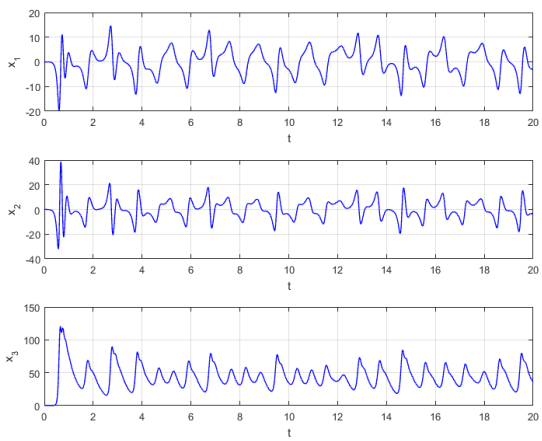

Fig. 8. $x_1(t), x_2(t), x_3(t)$ of (27) without controller

$$\begin{cases} \dot{x}_1 = -10x_1 + 10x_2 + sin(x_1), \\ \dot{x}_2 = -40x_1 + x_1x_3 + sin(t), \\ \dot{x}_3 = 4x_1^2 - 2.5x_3 + sin(x_1) + sin(t). \end{cases} \quad (27)$$

Due to the fact that Liu's chaotic system is a time-independent system, time is not a factor in the dynamics in this case. As a result, in (4), the function $f(x)$ has been utilized rather than $f(t, x)$. However, $d(t, x)$ is a combination of uncertainties and disturbances, and its values are indicated in (26). The chaotic movement of (27) with $x(0) = (-0.2, 0.3, 0.2)$ is shown in Fig. 6 to Fig. 8.

Although in our method, stabilization is possible for any time-dependent or time-independent system with any initial conditions without considering the boundary conditions for uncertainties and disturbances, but in example 2, we considered the initial conditions assumed in article [34]. We did this in order to be able to compare the results obtained in this article with those in [34]. Of course, it should be noted that in a non-linear system, initial conditions are important. A nonlinear system may become chaotic only under certain initial conditions. Therefore, the initial conditions cannot be chosen arbitrarily.

Considering the controllers, (27) can be written as:

$$\begin{cases} \dot{x}_1 = -10x_1 + 10x_2 + sin(x_1) + u_1(t), \\ \dot{x}_2 = -40x_1 + x_1x_3 + +sin(t) + u_2(t), \\ \dot{x}_3 = 4x_1^2 - 2.5x_3 + sin(x_1) + sin(t) + u_3(t). \end{cases} \quad (28)$$

Control over the chaotic system (28) is given by:

$$\begin{aligned} u_1(t) &= \xi_1 - KF(x_1) + 10x_1 - 10x_2 - d_1(t, x), \\ u_2(t) &= \xi_2 - KF(x_2) + 40x_1 - x_2x_3 - d_2(t, x), \\ u_3(t) &= \xi_3 - KF(x_3) - 4x_1^2 + 2.5x_3 - d_3(t, x). \end{aligned} \quad (29)$$

That $\xi_1 = -KF(s_1), \xi_2 = -KF(s_2), \xi_3 = -KF(s_3)$, $d_1(t, x) = \sin(x_1)$, $d_2(t, x) = sin(t)$, $d_3(t, x) = sin(x_1) + sin(t)$ are the uncertainties. It can be observed that in (29), controllers $u_1(t), u_2(t), u_3(t)$ are designed to remove the effects of uncertainties $d_1(t, x)$, $d_2(t, x), d_3(t, x)$ whether they are bounded or unbounded. Based on the aforementioned results, we design robust controllers. The numerical simulations demonstrate that the suggested strategy is more effective than the one suggested in [34]. As a consequence, using the suggested method, Fig. 9 shows the simulation results.

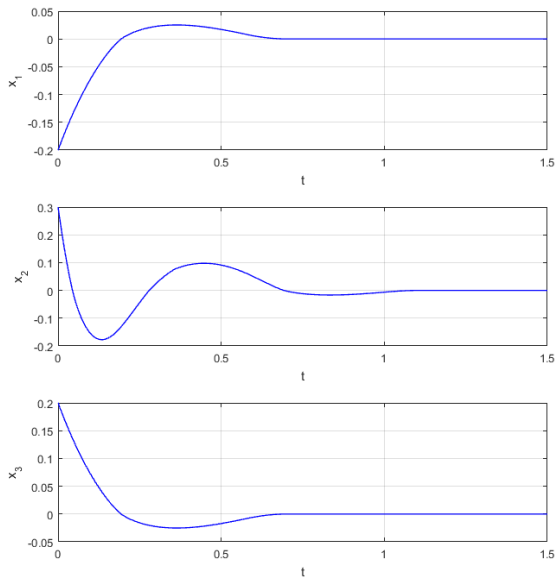

Fig. 9. $x_1(t), x_2(t), x_3(t)$ of (28) with $F(x) = A(x), K = 1$

Remark 6: In [34], a terminal sliding mode control strategy is designed and put into practice for a type of chaotic system with uncertainty. The dynamic uncertainties of the chaotic system were taken into account using sliding mode control (SMC), and the boundary problem of unknown model uncertainties was solved using a mix of SMC and an adaptive control strategy. In [34], by using an adaptive barrier function, chattering is fully removed. But in our method, by designing a suitable sliding surface, the control of Liu's system has been stabilized without any chattering in the control signals or the sliding surface curves of the system. In addition, in our method, the system becomes fixed-time stable. This example shows the effectiveness of our method.

V. Conclusions

In most of the articles mentioned in the references, researchers have considered a common sliding surface and then tried to stabilize a system with bounded uncertainty by using methods in adaptive control, optimal control, backstepping control, the barrier function, etc. Although these methods make the system stable, they often lead to complex calculations and the submission of special conditions to the system. But in this article, we sought to find an efficient sliding surface that is useful for most time-dependent and time-independent systems with uncertainties and disturbances that are not necessarily bounded. As it is clear in the proof of the theorems, using a suitable sliding surface does not require the use of Lyapunov's theorem. In this article, we have shown that in order to find a suitable sliding surface, one should first find the differential equation $\dot{x} = -F(x)$, which applies to condition $\left|\int_a^b \frac{dx}{F(x)}\right| < \infty$. Then, using this function $F(x)$, the sliding surface and controllers should be designed. Upcoming studies may focus on finding such functions. Furthermore, future research may focus on applying the results of this study to stabilize other kinds of dynamic systems with uncertainty and external disturbances.

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Auxiliary Pulse Tripling Circuit with Low kVA Rating to Reduce Input Current Harmonic Distortion in 12-pulse Rectifier

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ABSTRACT

In recent years, to increase the number of pulses in 12-pulse autotransformer rectifiers (12-PARs) and reduce the input current total harmonic distortion (IC-THD) without increasing the cost and complexity, the pulse multiplication circuit technique has been proposed. With this approach, to upgrade the rectifier structure from 12 to 36 pulses, an auxiliary pulse tripling circuit (APTC) with a very small kilovolt ampere rate (a kilovolt ampere equal to 1.34% of the rated load power) is presented. The proposed APTC consists of an unconventional interphase transformer (UIPT) with two diodes in the primary winding and a single-phase diode bridge rectifier connected to the secondary winding. In addition, the 12-phase autotransformer used in the proposed structure is based on a polygon connection with a very low kilovolt-ampere rate.

I. Introduction

With the development of power electronic converters, most DC drives have been replaced by variable frequency induction motor drives [1]. Induction motor drives are widely used in industrial applications. The 6-pulse diode bridge rectifier used in variable frequency induction motor drives causes problems such as power factor reduction and harmonic injection into the main line current due to the locking process. These current harmonics distort the voltage waveform by passing through the impedance of the source. Harmonics generally cause many problems in the power system, equipment, electrical loads, and especially measuring and control devices. Standards such as IEEE-519 and IEC61000-3-2 were developed to reduce the main current harmonics and limit current and voltage disturbances. To reduce harmonics, two methods of using filters and multi-pulse converters have been suggested [2]. Power quality can be improved by using active and passive filters; however, the use of passive filters has problems such as high losses, large required space, and the dependence of efficiency on frequency changes. Active filters also have problems such as complexity and high cost. Therefore, the method of increasing the number of pulses in the converter can be proposed and used as an efficient method for improving the power quality indicators, reducing the current passing through the power electronics, and reducing the kilovolt-ampere rate of the transformer. In recent years, multi-pulse rectifiers due to low harmonic distortion, low output voltage ripple, simple configuration, strong robustness, and correction of inherent power factor have

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been successfully used to improve power quality indicators in industrial applications [3]. To reduce line current harmonics, various designs of 12- and 18-pulse rectifiers have been reported in [4-6], but in these designs, the current harmonic reduction is more than 5%. To improve the power quality indicators, increasing the number of output phases of the phase shift transformer is the main solution. However, rectifiers with more pulses require a transformer with more size and volume, which increases the KVA rating and the total cost of multi-pulse rectifiers. [7-10 and 33].

The 40-pulse rectifier [9] includes a 20-pulse rectifier based on a 10-phase autotransformer and a circuit to upgrade the 20-pulse rectifier to 40-pulse. Note that the structure of the 10-phase autotransformer is very complex, and the kVA rating of the 40-pulse rectifier is very high and is equivalent to 64% of the nominal load. As a result, in industrial applications, 12-pulse rectifiers are mainly used because of the lightness and simplicity of the transformer, and as a result, the kilovolt-ampere rate and low cost. However, the total harmonic distortion of the input current in conventional 12-pulse rectifiers is theoretically approximately 15%, and without filtering, they cannot meet the requirements of the IEEE-519 standard. To reduce the harmonics and meet the requirements of the standards by reducing the weight, dimensions, and kilovolt-ampere rate of the multi-pulse rectifier, several methods based on active or passive auxiliary circuits in 12-pulse rectifiers have been reported in [11-13].

To reduce the harmonics in [14-21], several active auxiliary circuits are present in the DC link of the rectifier. In [14], an active interphase reactor with an auxiliary circuit, in [15] a DC-side current injection circuit, and in [16-17] an active interphase reactor is used to reduce harmonics. In [18, 19], the active interphase reactor along with an additional secondary winding is connected to an auxiliary modulation circuit, which leads to increased complexity, loss, and overall cost. The use of an active power filter [20] and a Vienna rectifier [21] can also increase the power quality of multi-pulse rectifiers. However, these methods have limitations such as computational complexity, complex control strategies, and accuracy in measuring control variables. In [22-24], a 12-pulse rectifier using a passive auxiliary circuit installed in the DC link is presented. In this method, the interphase reactor is replaced with a tapped interphase reactor. In [23], a 12-pulse rectifier connected in parallel with a two-tap interphase reactor and two diodes is proposed. When a double-tap inductor is used, the sum of the current passing through two diodes connected to the double-tap interphase reactor is equal to the load current, which leads to an increase in losses passing through the diodes in large load currents. To improve the power quality indicators in [25], a 20-pulse rectifier is proposed although its kVA rate is 35.3% of the load.

In [26], a 44-pulse rectifier based on a 22-phase polygon transformer is presented. This structure requires 44 diodes and a very complex transformer with several turns. Therefore, the method for reducing harmonics using an APTC is a simple, inexpensive method to achieve the above goal. In addition, because the magnetic part of the transformer used in multi-pulse rectifiers constitutes a major part of the dimensions, weight, and cost of multi-pulse rectifiers, in most non-isolated applications of the autotransformer due to the reduction of the magnetic part by about 80% compared to the transformer and as a result reducing dimensions, weight, losses, and cost of multi-pulse rectifier is used. With this approach, a 12-pulse rectifier based on a polygonal autotransformer with a low kVA rating is designed. This 12-pulse rectifier is then upgraded to an optimal 36-PAR using a low-complexity APTC. In terms of technical and economic indicators, it has been improved compared with the existing 36-PARs [27-29]. The comparison of existing multi-pulse rectifiers

TABLE 1
COMPARISON OF THE EXISTING MPRS

Part	20-Pulse [8]	20-Pulse [10]	20-Pulse [31]	24-Pulse [22]	24-pulse [24]	36-Pulse [15]	36-Pulse [28]	40-pulse [9]	40-pulse [36]	40-pulse [14]	44-Pulse [26]	48-pulse [35]	Proposed 36-pulse
% of THD	3.04	3.70	3.71	6.74	5.25	3.12	3.9	2.55	0.8	2.67	1.55	3.13	1.44
Total kVA Rating of the Autotransformer (Load Rating %)	40.27	45.47	44.48	39.7	115.00	30.30	44.15	63.98	31.88	30.8	42	31.57	24.08
Diode	20	20	20	10	14	16	36	42	28	20	32	30	18
Approximate total cost ($)	226.2	249.6	245.2	201.2	549.7	172.5	279.5	382.4	206.5	183.6	261	209.5	148.8

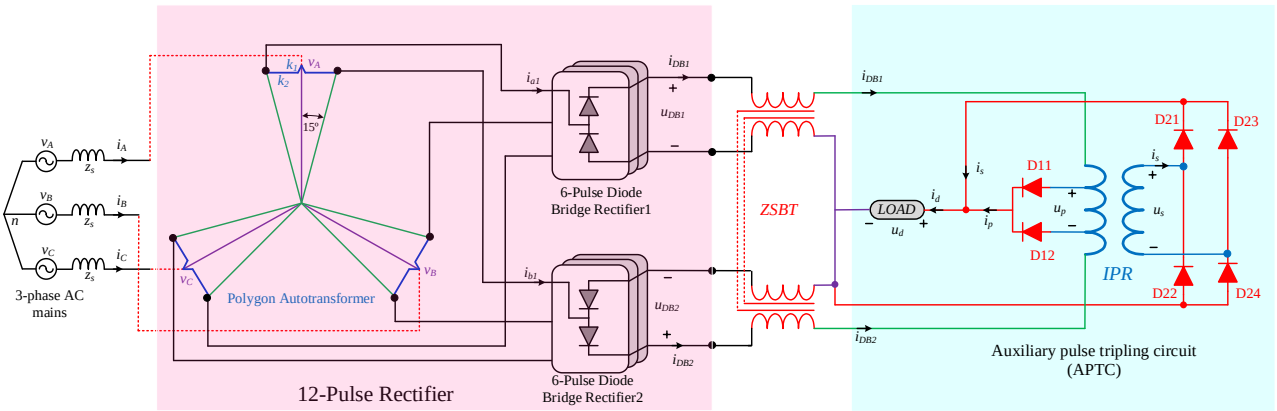


Fig. 1. 12-PAR with APTC

(MPRs) in terms of input current THD percentage, kVA rate, number of diodes, and approximate cost is presented in Table 1. Note that to estimate the cost of MPRs in this table, similar to the thumb estimation method in [36], it is calculated by multiplying the percentage of the kilovolt-ampere rate by 4.5. In addition, the cost of each diode is estimated to be $2.25. As can be seen in Table 1, with the increase in the number of pulses, the ability to reduce the harmonic distortion of the input current increases so that the 40-pulse rectifier [36] has a THD of the input current less than 1%. Note that transformer-based MPRs [24] have a kilovolt-ampere rate of more than 100%; as a result, they are more expensive than autotransformer-based MPRs. Also, the proposed 36-PAR has the lowest kilovolt-ampere rate equal to 24.08% of the load power, and as a result, the lowest cost is equal to 148.8.

II. Proposed 36-PAR design

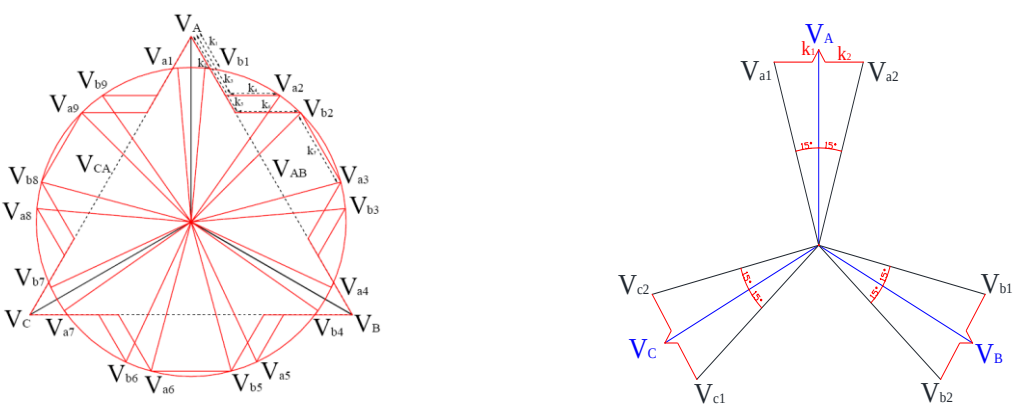
The proposed 36-PAR consists of two parts (as shown in Fig. 1). The first part of the 12-PAR is based on a six-phase polygon connection, and the second part is the APTC to upgrade the structure of the 12-PAR to 36-PAR.

A. Six-phase autotransformer design based on polygon autotransformer

The 18-phase polygon autotransformer [28] used in conventional 36-PAR is shown in Fig. 2 (a). As can be seen in this figure, the autotransformer has two 9-phase voltage series with a 10-degree phase shift. The structure of this autotransformer is very complex and includes several windings, which increases the kilovolt ampere rate of the autotransformer. The connections of the polygon autotransformer used in 12-PAR are shown in Fig. 2 (b). As can be seen in Fig. 2, the structure and number of windings of the 6-phase autotransformer in the 12-PAR is much simpler and lighter than the structure of the conventional 36-PAR [28].

The 12-PAR is based on a six-phase polygon autotransformer with a low kilovolt-ampere rate and a small weight and size. The minimum phase shift required to remove inappropriate harmonics is shown in equation (1):

$$\text{phase shift} = \frac{\text{Number of six pulse rectifiers}}{60^{\circ}} \quad (1)$$



(a) (b)

Fig. 2. Connections of the polygon autotransformer in (a) conventional 36-PAR [28] and (b) 12-PAR

Considering that in the 12-PAR, two conventional 6-pulse rectifiers have been used, according to equation (1), the phase shift between two series of voltages should be considered 30 degrees. The six-phase autotransformers produce 2 sets of three phases with 30 phase shifts for each diode bridge of six pulses.

The three-phase voltage of the source is as follows:

$$V_A = V_S\angle 0^\circ, V_B = V_S\angle -120^\circ, V_C = V_S\angle +120^\circ \quad (2)$$

Two voltage series with 30-degree phase shift output of the 6-phase autotransformer:

$$V_{a1} = V_S\angle 15^\circ, V_{b1} = V_S\angle -105^\circ, V_{c1} = V_S\angle 135^\circ, V_{a2} = V_S\angle -15^\circ, V_{b2} = V_S\angle -135^\circ, V_{c2} = V_S\angle 105^\circ \quad (3)$$

V_{a1} and V_{a2} are expressed as follows according to the winding ratio of the autotransformer:

$$\begin{cases} V_{a1} = V_A + K_1 V_{CA} - K_2 V_{BC} \\ V_{a2} = V_A - K_1 V_{AB} + K_2 V_{BC} \end{cases} \quad (4)$$

Considering equations 2 to 4, the constant values of K_1-K_2 are calculated. Due to the performance of the proposed 36-PAR, the DC link voltage is approximately 1.03% equal to the DC link voltage of the conventional 6-pulse rectifier. To use the proposed converter in alternative applications (applications that require exactly the DC link voltage equal to 6-pulse diode bridge rectifiers), the design of the proposed converter should be modified appropriately. For this purpose, the output voltage level of the polygon autotransformer should be 0.03 Decrease. The modified values of the coefficients for the performance of the proposed rectifier in alternative applications are calculated as follows:

$$K_1 = 0.0472, K_2 = 0.1201 \quad (5)$$

The above equations show the values of the constants K_1-K_2 (number of winding turns) as a fraction of the effective input voltage of the autotransformer. These values are used to simulate and build the autotransformer. the proposed polygon autotransformer. As can be seen in this figure, the output voltage of the autotransformer is a two-voltage series with a phase angle of 30 degrees. These two voltage series are connected to two conventional six-pulse diode bridges, which leads to the creation of a 12-PAR rectifier, which is then upgraded to a 36-PAR using an APTC.

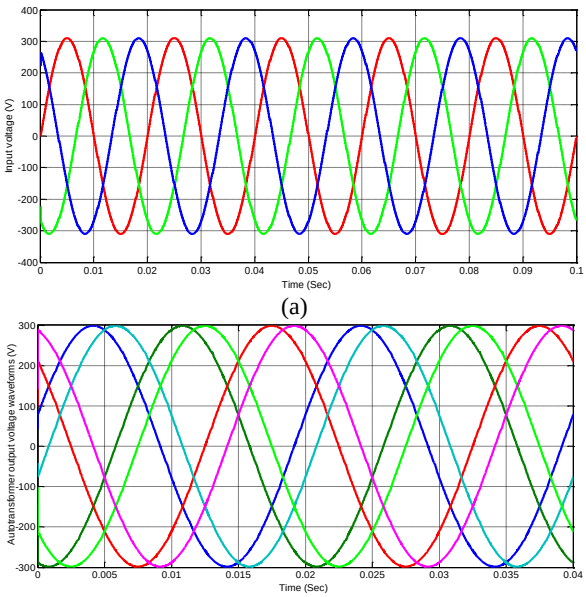


Fig. 3. (a) input and (b) output voltages of the autotransformer

B. *Design of the proposed APTC*

As shown in Fig. 1, the proposed APTC is used to

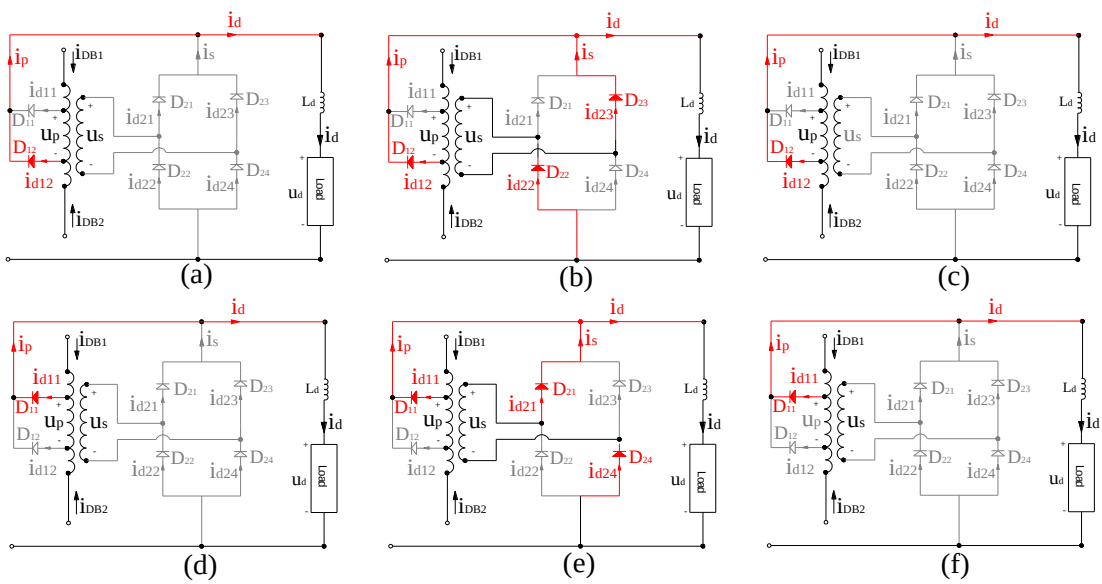


Fig. 4. Operating modes of the proposed APTC

upgrade the 12-PAR to the 36-PAR. this APTC consists of an unconventional interphase transformer (UIPT) with two diodes in the primary winding and a single-phase diode bridge rectifier connected to the secondary winding.

When $u_p>0$, diode D_{11} is on, and when $u_p<0$, diode D_{12} is on. In addition, when $|u_s|<u_d$, diodes D_{21}, D_{22}, D_{23}, and D_{24} are in reverse bias and off. When $u_s>u_d$, diodes D_{21} and D_{24} are forward biased and on, and diodes D_{22} and D_{23} are reverse biased and off. When $-u_s>u_d$, diodes D_{21} and D_{24} are in reverse bias and off, and diodes D_{22} and D_{23} are in forward bias and on. Therefore, based on the above points, as shown in Fig. 4, the proposed APTC has six operating modes. The mathematical relationships related to the working modes of the APTC (Fig. 4) are presented in Table 2. Note that the coefficients α and m in this table are the tap winding ratio and the turn ratio of the UIPT, respectively.

III. Modeling and simulation of the proposed 36-PAR

This section includes the software modeling and simulation of the 6-phase autotransformer based on polygon connection and the APTC to achieve the proposed 36-PAR in MATLAB-Simulink software. In the simulation, a source with a line voltage of 460 V and a frequency of 50 Hz and a load with a power of 30 kW and a voltage of 600 V are considered. In addition, the sum of the source impedance and the leakage inductance of the autotransformer is approximately equal to 5 mH. The sum of the inductances of ZSBT and UIPT is also considered to be approximately 20 mH. As shown in Fig. 5, the autotransformer structure of the proposed 36-PAR (Fig. 5-b) is much simpler and lighter with a lower kilovolt-ampere rate than conventional 36-PARs (Fig. 5-a). In addition, the number of diodes used in the structure of the proposed 36-PAR is less, and as a result, the conduction loss in the proposed rectifier is less than that in the conventional 36-PAR.

The results of the simulation completely confirm the performance of the different parts of the proposed design (the performance of the 6-phase autotransformer as well as the performance of the APTC). Figs. 6 and 7 show the input and output current and voltage waveforms of the proposed APTC, respectively. Note that in the APTC, the ratio of the turns of the transformer winding with an unconventional winding is approximately equal to 12 (Fig. 6), which leads to a decrease in the current passing through the secondary

TABLE 2.
WORKING MODES OF THE APTC

Mode	Fig.	KVL	KCL	Diode11	Diode12	Diode21	Diode22	Diode23	Diode24
1	4 (a)	$u_d = 0.5(u_{DB1} + u_{DB2})$	$\begin{cases} i_{DB1} = 0.5i_d - \alpha i_d \\ i_{DB2} = 0.5i_d + \alpha i_d \end{cases}$	Off $i_{D11} = 0$	On $i_{D12} > 0$	Off $i_{D21} = 0$	Off $i_{D22} = 0$	Off $i_{D23} = 0$	Off $i_{D24} = 0$
2	4 (b)	$\begin{cases} u_d = -u_s = \frac{2m}{2m+1-2\alpha} u_{DB2} \\ u_{DB1} = \frac{2m-1-2\alpha}{2m+1-2\alpha} u_{DB2} \\ u_p = -\frac{2}{2m+1-2\alpha} u_{DB2} \end{cases}$	$\begin{cases} i_s = \frac{1-2\alpha}{2m+1-2\alpha} i_d \\ i_{DB2} = \frac{2m}{2m+1-2\alpha} i_d \\ i_{DB1} = 0 \end{cases}$	Off $i_{D11} = 0$	On $i_{D12} > 0$	Off $i_{D21} = 0$	On $i_{D22} > 0$	On $i_{D23} > 0$	Off $i_{D24} = 0$
3	4 (c)	$u_d = 0.5(u_{DB1} + u_{DB2})$	$\begin{cases} i_{DB1} = 0.5i_d - \alpha i_d \\ i_{DB2} = 0.5i_d + \alpha i_d \end{cases}$	Off $i_{D11} = 0$	On $i_{D12} > 0$	Off $i_{D21} = 0$	Off $i_{D22} = 0$	Off $i_{D23} = 0$	Off $i_{D24} = 0$
4	4 (d)	$u_d = 0.5(u_{DB1} + u_{DB2})$	$\begin{cases} i_{DB1} = 0.5i_d + \alpha i_d \\ i_{DB2} = 0.5i_d - \alpha i_d \end{cases}$	On $i_{D11} > 0$	Off $i_{D12} = 0$	Off $i_{D21} = 0$	Off $i_{D22} = 0$	Off $i_{D23} = 0$	Off $i_{D24} = 0$
5	4 (e)	$\begin{cases} u_d = u_s = \frac{2m}{2m+1-2\alpha} u_{DB1} \\ u_{DB2} = \frac{2m-1-2\alpha}{2m+1-2\alpha} u_{DB1} \\ u_p = -\frac{2}{2m+1-2\alpha} u_{DB1} \end{cases}$	$\begin{cases} i_s = \frac{1-2\alpha}{2m+1-2\alpha} i_d \\ i_{DB1} = \frac{2m}{2m+1-2\alpha} i_d \\ i_{DB2} = 0 \end{cases}$	On $i_{D11} > 0$	Off $i_{D12} = 0$	On $i_{D21} > 0$	Off $i_{D22} = 0$	Off $i_{D23} = 0$	On $i_{D24} > 0$
6	4 (f)	$u_d = 0.5(u_{DB1} + u_{DB2})$	$\begin{cases} i_{DB1} = 0.5i_d + \alpha i_d \\ i_{DB2} = 0.5i_d - \alpha i_d \end{cases}$	On $i_{D11} > 0$	Off $i_{D12} = 0$	Off $i_{D21} = 0$	Off $i_{D22} = 0$	Off $i_{D23} = 0$	Off $i_{D24} = 0$

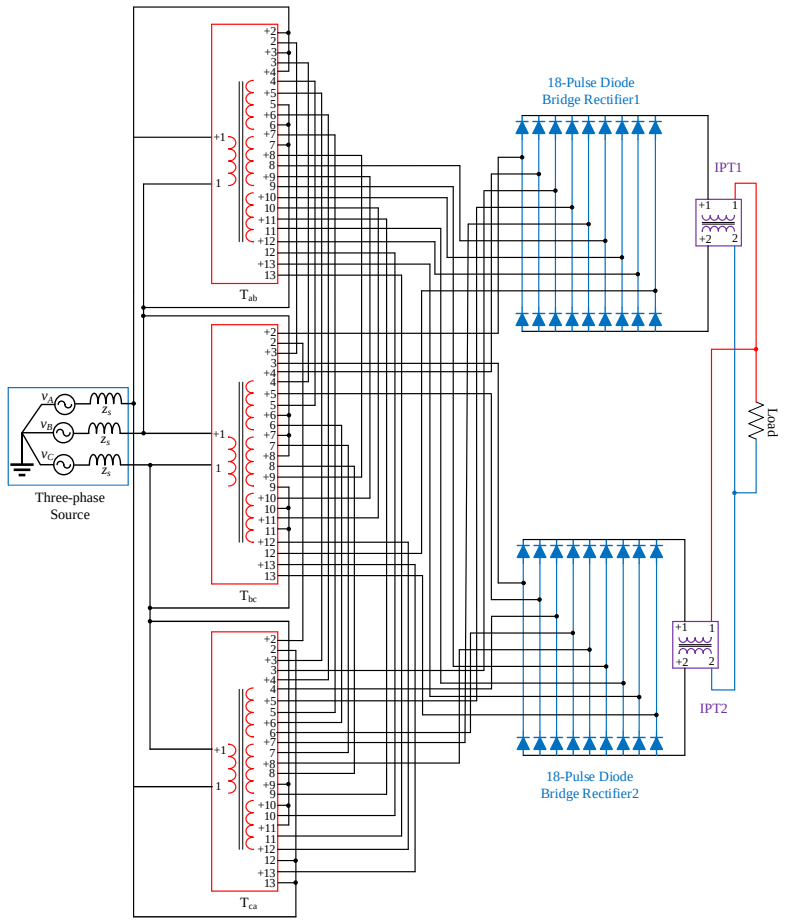
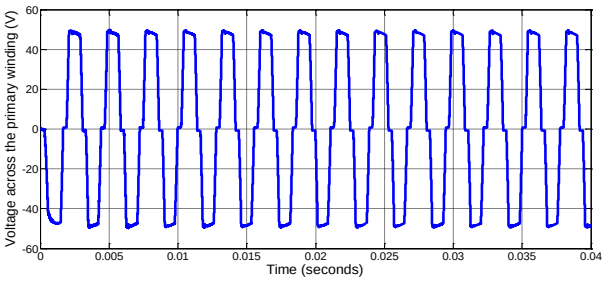
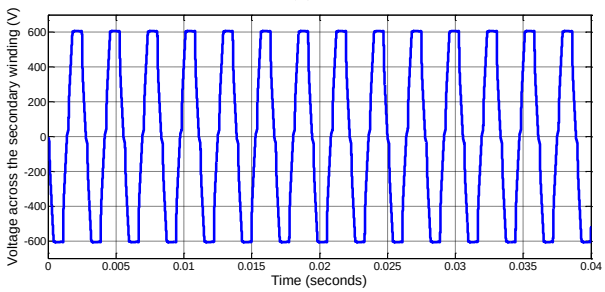


Fig. 5. MATLAB-Simulink model: (a) conventional 36-pulse rectifier [27] and (b) proposed 36-pulse rectifier

winding of the UIPT winding (Fig. 7-b). This form confirms the accuracy of the design and modeling of the APTC. The output voltage waveform of two conventional six-pulse diode bridges with a phase difference of 30 degrees is shown in Fig. 8, and the output voltage/current of the proposed 36-PAR is shown in Fig. 9. As can be seen in Fig. 9, the DC voltage/current of the proposed rectifier has 36-pulse in the output and is almost smooth with very little ripple, which confirms the performance of the different parts of the proposed rectifier.

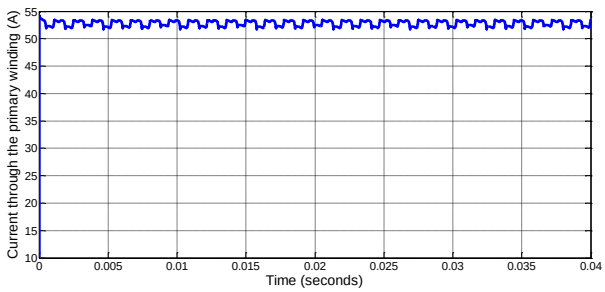


(a)

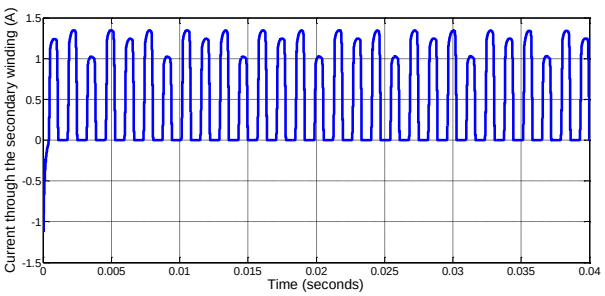


(b)

Fig. 6. (a) Input and (b) output voltage waveforms of the APTC



(a)



(b)

Fig. 7. (a) Input and (b) output current waveforms of the APTC

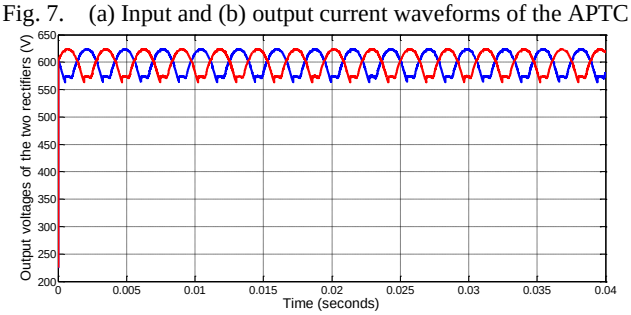
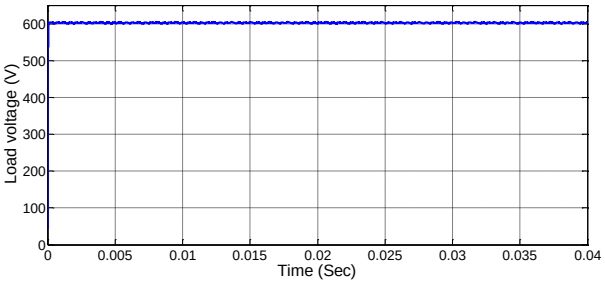
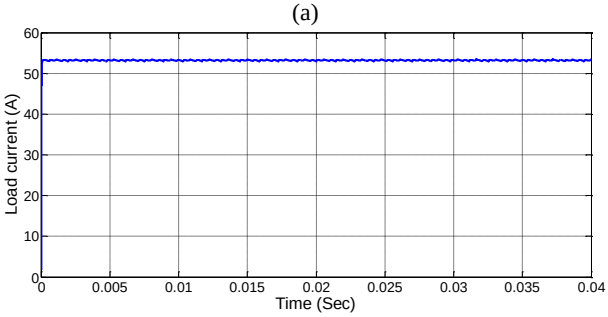


Fig. 8. Output voltage waveform of the two six-pulse diode bridges

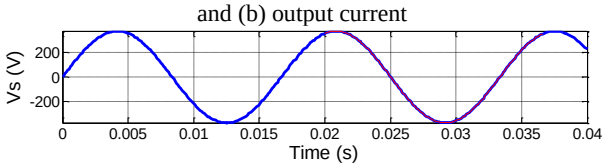


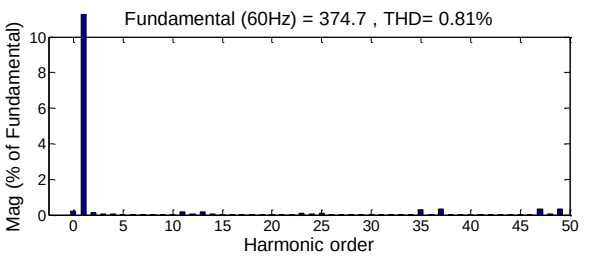
(a)



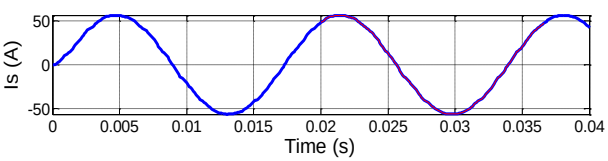
(b)

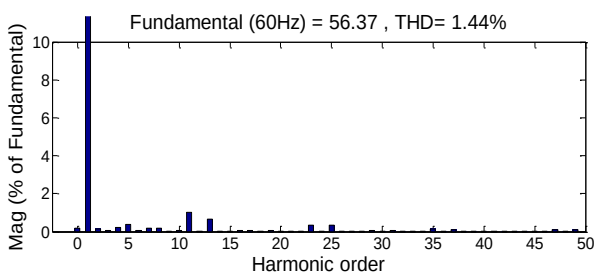
Figure 9. Waveforms of the proposed 36-PAR: (a) output voltage and (b) output current





(a)

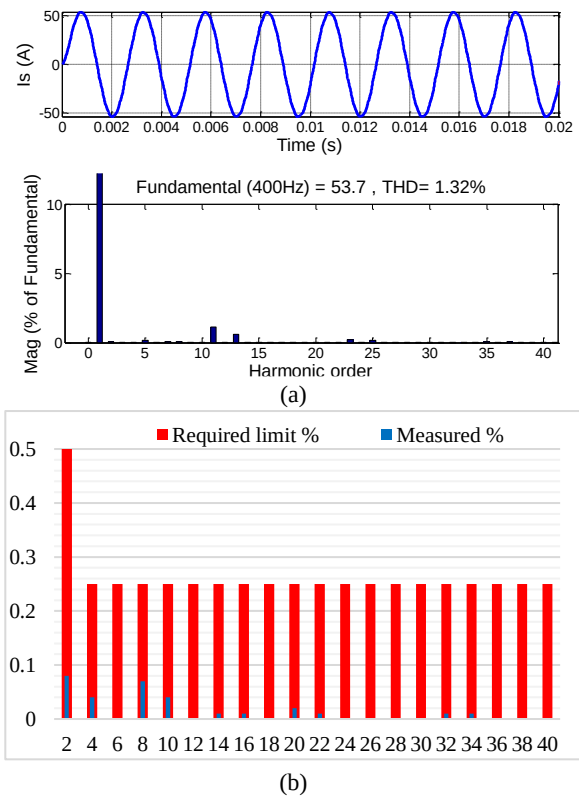




(b)

Fig. 10. Waveform and harmonic spectrum of the proposed 36-PAR at full load: (a) input voltage and (b) input current

The current THD in the six-pulse rectifier [33] is 3.3%. Fig. 10 shows the input current and voltage with the harmonic spectrum of the proposed 36-PAR. As can be seen in this figure, the harmonic distortion of the voltage is equal to 1.03% and that of the current is equal to 1.4%. The results show that the proposed rectifier performs well in reducing the harmonic distortion of the input current and voltage. To reduce the IC-THD in aviation applications, a 20-pulse rectifier and an 18-pulse rectifier are proposed in [31]. However, it should be noted that both of these rectifiers require the use of input and output filters to meet the requirements of the DO-160G standard. If the IC-THD in the proposed 36-PAR based on the APTC is less than 3% and without the need for a filter, it can meet the requirements of the DO-160G standard. To check the feasibility of using the proposed rectifier in aviation applications, the results of the harmonic distortion of the current by separating the odd and even harmonic orders and considering the allowed values of the DO-160G standard are shown in Fig. 11 for the source frequency of 400 Hz and Fig. 12 for the frequency 800 Hz source. As shown in Figs. 11 and 12, the proposed 36-PAR can meet the requirements of the DO-160G standard in even- and odd-order harmonics without the need for a filter. The results confirm the high efficiency of the proposed rectifier in aviation applications.



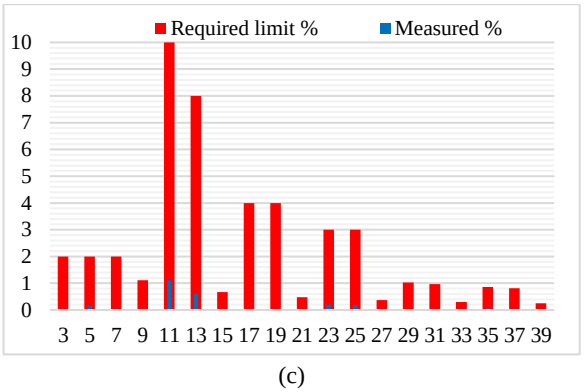
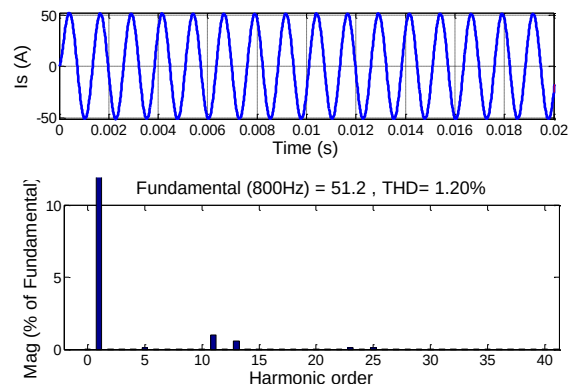


Fig. 11. (a) Input current along with its harmonic spectrum at a source frequency of 400 Hz, (b) even-order harmonics, and (c) odd-order harmonics compared to the DO-160G standard limit.



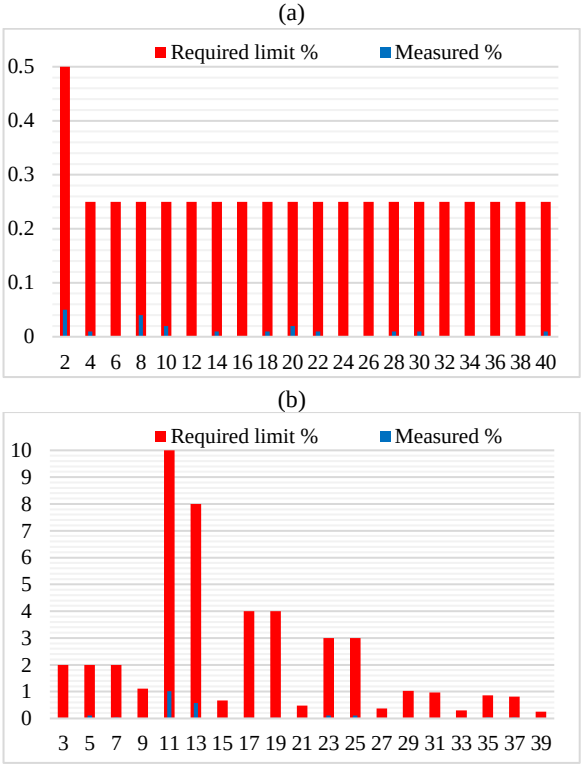


Fig. 12. (a) Input current along with its harmonic spectrum at a source frequency of 800 Hz, (b) even-order harmonics, and (c) odd-order harmonics compared to the DO-160G standard limit.

IV. kilovolt-ampere rate

The rms values of the winding voltage and current of the six-phase polygon autotransformer, the zero sequences blocking circuit (ZSBT), which is used to isolate the output voltages of two six-pulse rectifiers, and the rms values of the winding voltage and current of the UIPT winding for a 10 kVA load were calculated by software simulation. Based on these values and equation (6), the kilovolt-ampere rate of the proposed rectifier is calculated.

$$S = 0.5 \sum V_{winding} I_{winding} \quad (6)$$

The kilovolt-ampere rate of the polygon autotransformer is equal to 1809.39 volts, ZSBT is equal to 464.72, and UIPT is equal to 134.77. In total, considering the rated load power of 10 kV, the kilovolt-ampere rate of the proposed 36-PAR is equal to 24.08% of the rated load power. Fig. 13 shows a comparison of the proposed 36-PAR with conventional 36-PARs [27-30] in terms of the kilovolt-ampere rate and harmonic distortion percentage of the total current at full and light loads (equivalent to 20% of full load). As can be seen in this figure, the kilovolt-ampere rate of the proposed rectifier is far lower than that of conventional 36-PARs. The kilovolt-ampere rate of the proposed rectifier is approximately 19.14%, 19.84%, 37.82%, and 6.43% lower than the kVA rating of 36-PARs [27], [28], [29], and [30], respectively. In addition, the harmonic distortion of the current in conventional 36-PARs [27-30] under light load is more than 3%, whereas, in the proposed 36-PAR, the harmonic distortion of the current is always less than 3% and conforms to MIL-STD 704F and IEEE-519 standards. This confirms the high technical and economic capabilities of the proposed rectifier compared with conventional 36-PARs.

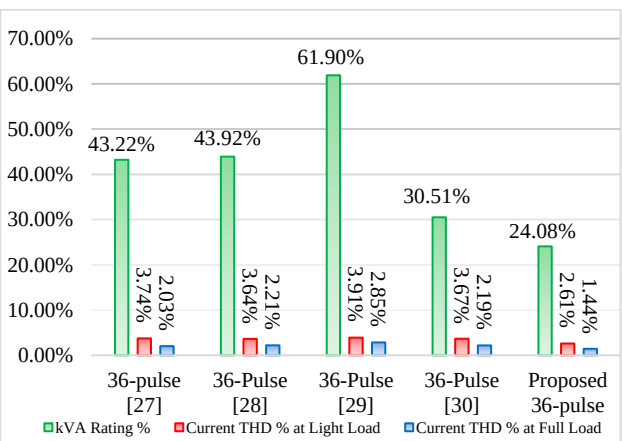
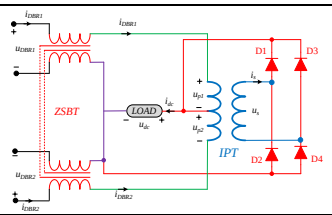
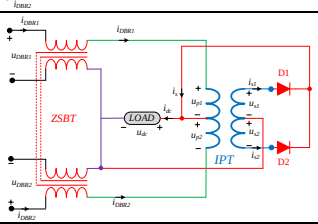
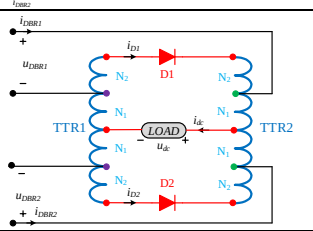
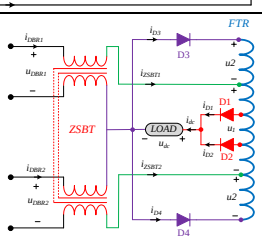


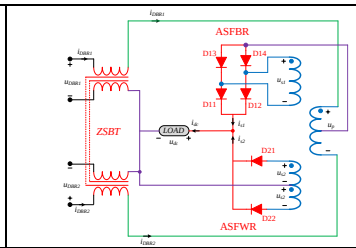
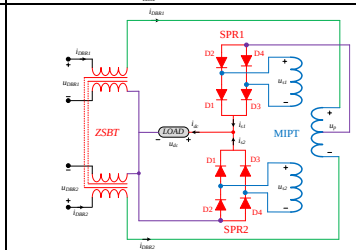
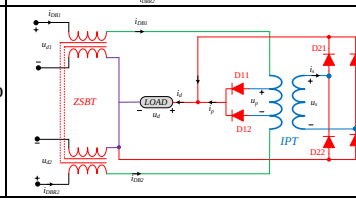
Fig. 13. Comparison of the kVA and current harmonic distortion in the proposed 36-pass rectifier with conventional 36-PARs

V. Comparison of the proposed APTC with existing harmonics-reducing circuits

In this section, to evaluate the structure of the APTC used in the proposed 36-PAR with existing harmonic reducing circuits, the structure of various types of harmonic reducing circuits along with the kilovolt-ampere rate and the number of diodes of each of the structures are listed in Table 3. As can be seen in this table, the existing harmonic reducing circuits have 2 to 8 diodes, and in this sense, the proposed APTC includes 6 diodes. In addition, the kilovolt-ampere rate of the proposed APTC is equal to 5.99% of the full load power, which is lower than the kilovolt-ampere rate of the existing harmonic reduction circuits. The approximate cost of the proposed APTC is $40.5, which is acceptable compared to the cost of existing harmonic reduction circuits.

TABLE 3.
COMPARISON WITH SIMILAR HARMONIC REDUCTION CIRCUITS

References	Topologies	Total kVA rating (%)	Number of Diodes	Total Cost ($)
[22]		9.84	4	53.3
[24]		8.04	2	40.7
[34]		11.27	2	55.2
[34]		6.97	4	40.4

[35]		7.57	6	47.6
[36]		6.98	8	49.4
Proposed		5.99	6	40.5

VI. Conclusion

In this paper, a proposed 36-PAR based on a 6-phase autotransformer with an APTC with a low kilovolt-ampere rate is presented. These two advantages have led to savings in the size and cost of the proposed 36-PAR compared to other conventional 36-PARs. The simulation results show that in addition to meeting the requirements of the IEEE 519 standard, the IC-THD in the proposed 36-PAR is less than 3% and conforms to the MIL-STD standard. Also, the results confirm the performance of the proposed 36-PAR under the requirements of the DO-160G standard in aviation applications without the need for a filter. The proposed 36-PAR kilovolt-ampere rate is 24.08% of the rated load power. In general, the proposed 36-PAR is superior both technically and economically compared to other conventional 36-PARs.

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Designing and Fabrication of High Frequency Ultra-wideband Passive Phase Shifters with Single Layer Microstrip Structure and Unequal Source and Load Impedances

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ABSTRACT

In this paper, a method is presented to design and implement ultra-wideband phase shifters, in frequency ranges higher than 10 GHz, with fractional bandwidth near a hundred percent. The phase shifter is constructed from microstrip transmission lines and short circuit stubs. In comparison with conventional phase shifters which are composed of microstrip coupled lines and multilayer structures, the proposed phase shifter has advantages from the implementation and fabrication viewpoint. The design and optimization method is in such a way that arbitrary phase shift, source and load impedances may be considered in the design. To optimize the circuit dimension, a computer code is written, and two design examples are considered. The computer code is based on closed form equations for microstrip transmission lines and available circuit models for it and utilizes microwave network equations. Its results are then improved with electromagnetic full-wave packages to consider the parasitic effects of microstrip T-junctions. Two design cases are included, in the first design, the case of a 45 degrees phase shifter with a standard 50 ohms source and load impedances is investigated. In the second design case, the case of a 90 degrees phase shifter with 50 ohms input impedances and 75 ohm non-standard output impedances is considered. By observing the full-wave simulation results as well as the fabrication and measurement results in these examples, it is clear that the design goals are highly satisfied by this method.

I. Introduction

The technology and engineering revolution seeks to improve the quality of human life and actualize social development. Challenges in social conditions are also extended to physical sciences and engineering. In other words, today's development is intertwined with research related to technology. The answer and solution to the issues and problems for the development of societies lies in electronics and telecommunications. Rarely is there a situation in electronics and telecommunications where the concept of phase changes is not discussed. Basically, in many cases, the main information is in the phase that needs to be extracted. In measurement systems, comparing the phase of signals helps improve the accuracy, quality and reliability of data. Many processes are performed on the phase in the diagnosis and imaging. In engineering, the phase of the reflection coefficient is very useful in detecting the type and geometry of objects by the reflection of electromagnetic waves. Among other applications of phase shifters, it is possible to refer to the cases of power combiners and power dividers, amplifiers, mixers, and radars, especially phased array radars. The ideal phase shifter is an adapted two-port network or

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circuit without losses, which can change the phase of a specific signal at the desired working frequency with respect to its reference state. Of course, none of the phase shifters are without loss in practice. But it is expected that the losses be low and constant. Phase shifters are divided into, analog or digital, made of integrated or discrete circuit, two-dimensional or three-dimensional circuits and integrated or discrete. working frequency of phase shifters are radio, microwave and millimeter waves. various design and construction methods are presented according to frequency, bandwidth, compatibility with technology, cost, commercial quality and optimality criteria [1-3].

Phase shifters have many applications in communication systems like in any ultra- wideband array antennas with beam steering abilities and ultra-wideband radars with abilities to track transmitters in ultra -wideband frequency ranges. In digital systems, the speed of information transfer is very important. High speed in these systems is equivalent to wide bandwidth in analog systems. Therefore, ultra-wideband phase shifters are one of the main components of great importance. In the structure of the mixer, from the combination of signal RF and LO, signal IF is obtained, with the performance of the mixer depending on the phase shifters RF and LO in the frequency band.

Ultra-wideband (UWB) phase shifters and impedance transformers are key elements in transmitter, receiver communication circuits and array antennas. Phase shifters have been used in multi-beam antennas [4] and multi-channel amplifiers [5]. In differential phase shifters, the signal phase delay passing a main path is compared with corresponding one passing from another path called reference path. An electronically controllable active phase shifter is designed and implemented in Ku band [6]. Passive phase shifters are more stable and have lower costs than active counterparts. So far many designs have been presented to implement differential passive wide-band phase shifters. The most famous one was introduced by Schiffman in 1958 [7], in which he utilized strip line coupled transmission lines in implementing wideband phase shifters. In [8], microstrip coupled line transmission lines are used to obtain Schiffman phase shifter and study the effects of differences between the phase velocities of even and odd modes of the microstrip coupled lines, on the specification of Schiffman phase shifter, This study showed that due to the differences between even and odd mode propagation constant in microstrip coupled transmission lines, the usage of microstrip coupled transmission lines instead of coupled striplines in Schiffman phase shifter will definitely affect its performance. The usage of multi section coupled transmission lines increase the bandwidth of directional couplers and Schiffman phase shifters and with this technique wideband 90 and 180 degree phase shifters are implemented [9]. In [10] asymmetric coupled lines are employed to increases the amount of coupling and bandwidth of coupled-line couplers. In that design, one of the components of coupled line structure is interdigital transmission line and the other is conventional microstrip transmission line.

The common problem with all of the above mentioned works is that for increasing the level of edge coupling in wideband applications, it is required that the distance between the coupled lines be very small, or very narrow transmission lines be used in implementing interdigital transmission lines, which may lead to fabrication difficulties, and the etching tolerances practically limits the operation of these designs to frequencies below 10 GHz.

Other structures are invented that do not utilize microstrip coupled lines to realize phase shifters. In [11], multi-layer structure is used to realize UWB phase shifter in the frequency range 1.3-5.9 GHz. In this design, the above layer is coupled to the bottom one through a slot made in the ground plane between them. This design may have fewer applications in monolithic microwave integrated circuit (MMIC) designs which usually are designed as single layer prototypes. In [12], another UWB phase shifter is designed by means of microstrip to slot line coupling structure in the frequency range 3.1-10.6 GHz and with phase shift in the range 4-27 degrees. No design is introduced out of this phase shift range in that work. The slot lines are made by removing metallic surface from ground plane partially, so it is needed to apply the etching process on both the surfaces above and below the substrate. Also due to the presence of defected ground, that design has radiation loss especially at higher frequencies. In another article [13], microstrip transmission lines and half wavelength open circuited stubs are used to achieve a wideband phase shifter. The phase shift amount was $90^{\circ} \pm 6.4^{\circ}$. The advantages of the design include elimination of coupled lines and remaining of the ground plan unaltered. But the design bandwidth is not enough for covering UWB applications and the high lengths of half wavelength open stubs, result in a larger circuit size. The T-shaped open circuited stub is used to decrease the circuit size in that work. In [14], two multi-sectional radial transmission lines are used instead of T-shaped open circuited stub to increase the bandwidth. The phase shift amount was $90^{\circ} \pm 9^{\circ}$. However these designs have dealt with realizing just 90 degrees phase shifters and seemingly they failed to design circuits that consider the phase shifts below 90 degrees.

On the other hand, wideband impedance matching is inevitable in communication circuits, since the input and output impedances of transmitters, receivers and phase shifters may not necessarily be the standard 50 ohms values. As far as the authors know, all of the works done so far on phase shifters,

are based on standard 50 ohms source and load impedances. For example, none of the studies can apply to a case with the load impedance of 75 ohms. Extra UWB matching circuit is needed after designing the phase shifter, and this will lead to a complicated design process and increased circuit size. The points related to the integration using the theory of transmission lines have been attended in studies [15-17]. Also to the best of author knowledge, the works done on phase shifters so far, support frequencies up to 10.6 GHz, and at higher frequencies no design has yet been presented.

In the current research, a method is illustrated to design and implement the UWB differential phase shifter in the frequency range 6-18 GHz. The proposed method does not use any coupling structure and the ground plane also is not altered. The proposed structure is in single layer type and the design method can satisfy different design goals like arbitrary phase shift values as well as arbitrary source and load impedance levels. The suggested structure uses a simple combination of microstrip transmission lines along with short circuited quarter wavelength stubs. In the part II, below some explanations are given about the theoretical analysis and the phase shifter structure used in this work. Two design cases are presented in parts III and IV the fabrication and simulation results are depicted which further describes the design process.

II. THEORETICAL ANALYSIS

This section shows that combination of two microstrip transmission lines and a quarter wavelength short circuited stub, presents similar phase behavior with Schiffman phase shifter which is constructed from couple striplines [7]. Consider the structure of figure 1. This figure illustrates the base building block of the proposed phase shifter, which has a main path and a reference path. In this figure the characteristic impedances of all transmission lines are assumed to be 50 ohms and the electrical length of all transmission lines in the main path is θ. The input and output impedances of all ports are 50 ohms.

When cascading two-port networks, the overall ABCD matrix is equal to the product of the individual ACBD matrix. in Figure 1, the network consists of three two ports. First, a transmission line, second, a short-circuit parallel transmission line, and third, a transmission line. Their transfer matrix is as follows:

$[ABCD1] = \begin{bmatrix} cos\theta & iz_o sin\theta \\ iy_0 sin\theta & cos\theta \end{bmatrix}$, [ABCD2]=$\begin{bmatrix} 1 & 0 \\ y & 1 \end{bmatrix}$,

[ABCD3]= $\begin{bmatrix} cos\theta & iz_o sin\theta \\ iy_0 sin\theta & cos\theta \end{bmatrix}$

The admittance of the parallel short circuit branch is $y = -iy_o \frac{cos\theta}{sin\theta}$ The product of these three matrices is obtained as

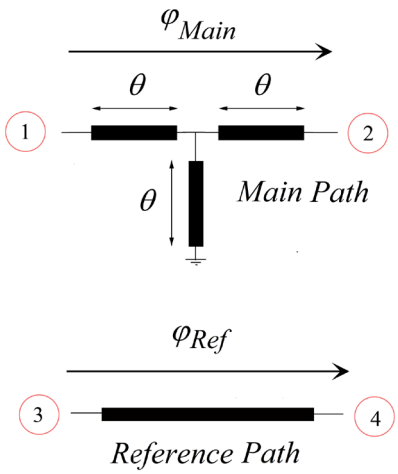

Figure 1- Main and reference paths in the building block of the proposed phase shifter.

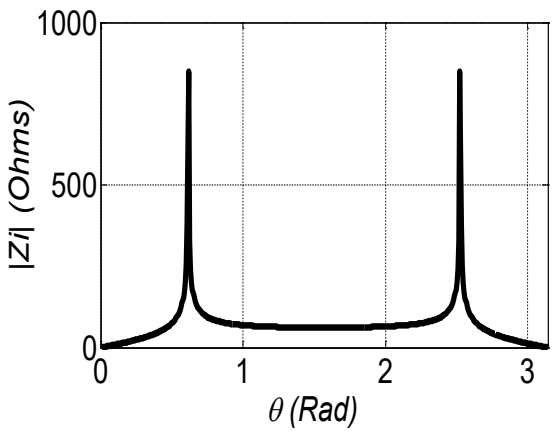

Figure 2- Magnitude of image impedance for the main path in figure 1.

$$[ABCDT] = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = [ABCD1][ABCD2][ABCD1]$$

$$= \begin{bmatrix} 2-3sin^2(\theta) & i75\,sin(2\theta) \\ i\dfrac{2cos(\theta)-3cos^3(\theta)}{50\,sin(\theta)} & 2-3sin^2(\theta) \end{bmatrix} \quad (1)$$

Considering symmetry in figure 1, we have A=D in (1) and the image impedance is obtained from,

$$Z_{i1} = \sqrt{\frac{AB}{CD}} = \sqrt{\frac{B}{C}} = \sqrt{\frac{7500\,sin^2(\theta)}{3sin^2(\theta)-1}} \quad (2)$$

where A, B, C and D are the elements of transmission matrix in figure 1 and are obtained in (1). Magnitude of image impedance is plotted in figure (2). As it can be seen, it is approximately constant equal to 50 ohms in a relatively large bandwidth.

The amount of attenuation α and phase delay ϕ_{Main}, in the main path from port 1 to 2, can be found from $= \alpha + j\beta$.

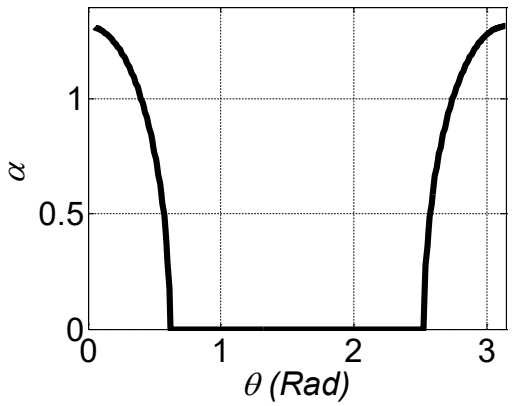

Figure 3- Attenuation amount of the main path in figure 1, obtained by image theory.

where γ is the complex propagation coefficient, α is the attenuation coefficient and β is the propagation constant. The relationship between γ and the elements of transmission matrix, using image theory [18], is as follows,

$$\cosh\gamma = \sqrt{AD} \qquad (3)$$

In figure 3, main path attenuation is provided. Frequency ranges in which $\alpha = 0$, correspond to pass band and the others in which $\alpha \neq 0$, resemble stop band regions. Figure 4, presents the phase delay in the main path ϕ_{Main} and reference path ϕ_{Ref}. Considering that in figure 1, a single transmission line is used in the reference path, which its physical length is proportional to the physical length of one of the transmission lines composing the main path, the electrical length of the reference path ϕ_{Ref} would be proportional with θ, so ϕ_{Ref} versus θ would be a linear function. In figure 4, the ratio ϕ_{Ref} to θ is adjusted in such a way that $\phi_{Ref} - \phi_{Main}$ becomes constant in a relatively wide frequency range. It is concluded that in this figure, ϕ_{Ref} / θ is a little greater than 2.

Comparing the phase difference behavior of the structure in figure 1 and Schiffman phase shifter [7] seems interesting. In figure 5, the Schiffman phase shifter is shown. As is stated in section 1, Stripline coupled transmission lines are used in Schiffman phase shifter. ϕ_{Main} is obtained from [7],

$$\cos(\varphi_{Main}) = \frac{\frac{Z_{0e}}{Z_{0o}} - \tan^2(\theta)}{\frac{Z_{0e}}{Z_{0o}} + \tan^2(\theta)} \qquad (4)$$

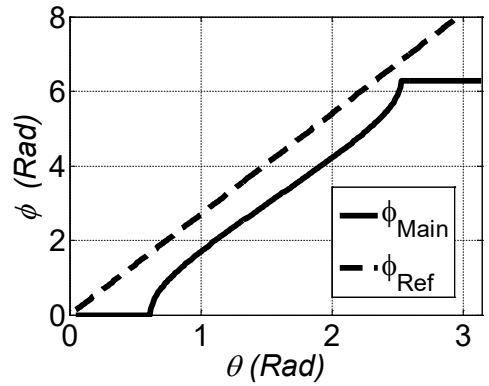

Figure 4- Phase delays in the main path ϕ_{Main} and in the reference path ϕ_{Ref} in figure 1.

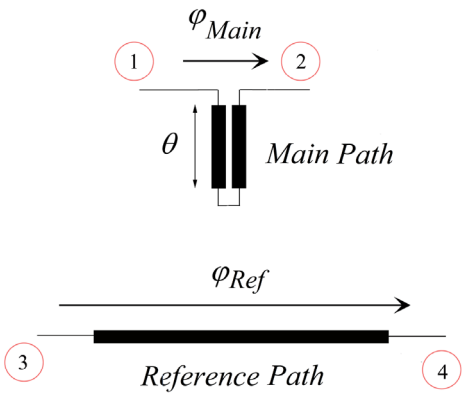

Figure 5 - The structure of differential Schiffman phase shifter

Z_{0o} is odd mode impedance is defined as characteristic impedance of a transmission line with driven signals of the same amplitude and opposite polarity and Z0e is even mode impedance with same amplitude and polarity. ρ is the ratio of these two impedances.

For the case with $\rho = \frac{Z_{0e}}{Z_{0o}} = 10$, which corresponds to tight coupling, and the edge coupled transmission lines must be very close to each other, ϕ_{Main} and ϕ_{Ref} are sketched in figure 6. The length of the reference path is adjusted in such a way that the phase difference $\phi_{Ref} - \phi_{Main}$ becomes nearly constant in a broad bandwidth. In this case, the ratio ϕ_{Ref} / θ becomes approximately 6. Comparing figures 4 and 6, it is apparent that, the bandwidth of figure 1 is better than that of figure 5, and for keeping $\phi_{Ref} - \phi_{Main}$ constant $\phi_{Ref} - \phi_{Main}$ in a wide frequency range, the required length of the reference path in figure 1 can be half the length of the reference path in figure 5, resulting in a reduced dimension for the reference path.

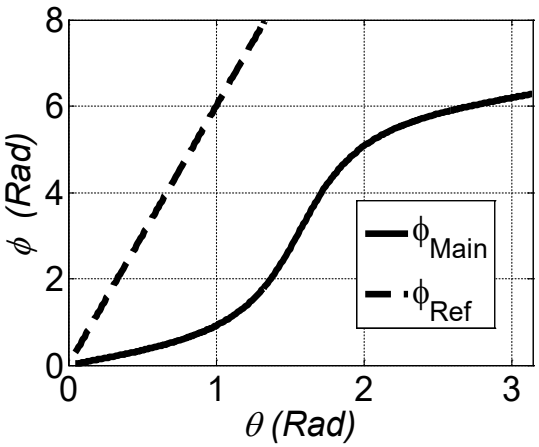

Figure 6 - Phase delays in the main path, ϕ_{Main} and in the reference pat , ϕ_{Ref} , in figure 5.

The problem with the phase shifter structure introduced in figure 1, is that its bandwidth is not still enough to cover UWB applications. Also, this structure is used in a very special case where the impedance of all transmission lines and ports are assumed to be equal to 50 ohms. Also, the electrical length of all transmission lines in the main path are considered equal. In succeeding parts of this paper, extra sections to the configuration of figure 1 are added and the reference path is altered. Moreover, the electrical length and characteristic impedances of composing transmission line of this structure are adjusted. Then, the possibilities of improving the bandwidth of this structure, realizing arbitrary phase shifts and input/output impedances are investigated. In the first example, the case of standard 50 ohms input/output impedance is considered while the phase shift is assumed to be 45 degrees. In the second example, the case of 90 degrees phase shift is presented along with nonstandard 75 ohms output impedances.

III- First Design Example: Phase Shifter with 50 Ohms Input/Output Impedances and 45 Degrees Phase Shift

Figure 7 shows the geometric structure of the proposed phase shifter. In this design the input/output port impedances are assumed to be standard 50 ohms, and 45 degrees phase shift in 6-18 GHz is desired. The reflection coefficient from input ports of the main and reference paths must be as low as possible. In this work, RT-Duroid 5880 substrate with dielectric constant 2.22 and 15 mil thickness is used to realize microstrip transmission lines.

This structure is a multi-section version of the structure in figure 1 to increase its bandwidth, and the reference path

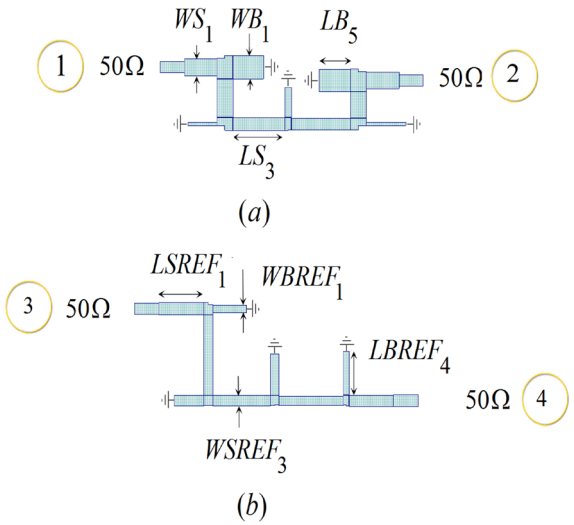

Figure 7- Geometric structure of the proposed phase shifter in the first design example, (a) main path ,(b) reference path.

structure is also considered similar to the reference path one. The number of sections in the main path is 5 and for the reference path is 4. The lengths and widths of all transmission lines are considered as variables in the optimization process. The lengths and widths of transmission lines that are connected in series in the main path are named as LS_i and WS_i, respectively and the ones that belong to the reference path are similarly named as $LSREF_j$ and $WSREF_j$, also The lengths and widths of short circuited stubs that are used in the main path are indicated by LB_i and WB_i and those of the reference path are illustrated by $LBREF_j$ and $WBREF_j$. In figure7, dimensions of some of the exemplary transmission lines are depicted. For ease of fabrication and connecting 50 ohms SMA connectors to the circuit, 50 ohms microstrip transmission lines with length 3 mm and width 1.175 mm are connected to each port. To optimize the dimensions of figure 7, a computer code is written using MATLAB [19]. The following error function is considered,

$$Error = 2\sum_{n=1}^{40}\left[20\,log\left|\bar{S}Main_{11,n}\right| + 30\right]^2 + \sum_{n=1}^{40}\left[20\,log\left|\bar{S}REF_{11,n}\right| + 30\right]^2 + \sum_{n=1}^{40}\left[\left(\angle\bar{S}Main_{21,n} - \angle\bar{S}REF_{21,n}\right) - 45^\circ\right]^2 \quad (5)$$

In (5) it is aimed that the normalized reflection coefficients for the main path and reference path, i.e., $\bar{S}Main_{11,n}$ and

$\bar{S}REF_{11,n}$ become as low as -30 dB. Phase difference between the main path and reference path, i.e., $\left(\angle\bar{S}Main_{21,n} - \angle\bar{S}REF_{21,n}\right)$ must become 45 degrees. Frequency range 6-18 GHz is assumed to be divided into 40 equidistance discrete points. In this special example the emphasis is on reducing the reflection coefficient of the main path rather than the reference path, so the weighting factor in the first term is assigned twice the second term in (5) and section numbers of the reference path is selected less than the main path. In general, assigning weighting factors are somehow experimental and depends on special application.

The normalized scattering matrix coefficients $\left[\bar{S}\right]$ used in (5), can be calculated from non-normalized $[S]$ from,

$$\begin{bmatrix} \bar{S}_{11} & \bar{S}_{12} \\ \bar{S}_{21} & \bar{S}_{22} \end{bmatrix} = \begin{bmatrix} S_{11} & \frac{\sqrt{Z_2}}{\sqrt{Z_1}} S_{12} \\ \frac{\sqrt{Z_1}}{\sqrt{Z_2}} S_{21} & S_{22} \end{bmatrix} \quad (6)$$

Non-normalized scattering matrix for each of the networks in reference and main paths, i.e., $[SREF]$ and $[SMain]$, may be obtained from their transmission matrix, i.e., $\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{REF}$ and $\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Main}$. Neglecting parasitic effects of T-junctions in initial design step, transmission matrix for the main path can be obtained from multiplication of transmission matrixes of the composing elements of the network, i.e., series transmission lines and short circuit stubs, as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Main,f} = \left(\prod_{i=1}^{5} [TS_{i,f}][TB_{i,f}]\right)[TS_{6,f}] \quad (7)$$

Where $\left[TS_{i,f}\right]$ is transmission matrix of the i'th series transmission line at frequency 'f ', and is gotten from [12],

$$[TS_{i,f}] = \begin{bmatrix} \cosh\gamma S_{i,f} LS_i & ZS_{i,f} \sinh\gamma S_{i,f} LS_i \\ \frac{1}{ZS_{i,f}} \sinh\gamma S_{i,f} LS_i & \cosh\gamma S_{i,f} LS_i \end{bmatrix} \quad (8)$$

Where $\gamma S_{i,f} = \alpha S_{i,f} + j\beta S_{i,f}$ is the propagation constant , $ZS_{i,f}$ and LS_i are the characteristic impedance at frequency *'f'*, and physical length of i'th series transmission line . $\gamma S_{i,f}$ and $ZS_{i,f}$ are functions of transmission line dimensions and substrate specifications. In the computer program, closed form equations for microstrip transmission lines which are valid to 60 GHz and consider all frequency dispersion and attenuation effects [18]. In (9), $\left[TB_{i,f}\right]$ is the transmission matrix for the i'th short circuited stub at frequency *'f'* and is obtained from,

$$\left[TB_{i,f}\right] = \begin{bmatrix} 1 & 0 \\ \frac{1}{ZB_{i,f} \tanh\gamma B_{i,f} LB_i} & 1 \end{bmatrix} \quad (9)$$

Where $\gamma B_{i,f} = \alpha B_{i,f} + j\beta B_{i,f}$ is the propagation constant and $ZB_{i,f}$ and LB_i are the characteristic impedance at frequency *'f'*, and physical length of i'th short circuited stub.

Normalized scattering matrix for the reference path may be calculated through the same method as applied in the above for the main path. This network is considered as a 4 section one, so its transmission matrix is obtained as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{REF,f} = \left(\prod_{i=1}^{4} [TSREF_{i,f}][TBREF_{i,f}]\right)[TSREF_{5,f}] \quad (10)$$

Where in this equation, similar to (8), (9)

$$[TSREF_{i,f}] = \begin{bmatrix} \cosh\gamma SREF_{i,f} LSREF_i & ZSREF_{i,f} \sinh\gamma SREF_{i,f} LSREF_i \\ \frac{1}{ZSREF_{i,f}} \sinh\gamma SREF_{i,f} LSREF_i & \cosh\gamma SREF_{i,f} LSREF_i \end{bmatrix} \quad (11)$$

$$\left[TBREF_{i,f}\right] = \begin{bmatrix} 1 & 0 \\ \frac{1}{ZBREF_{i,f} \tanh\gamma BREF_{i,f} LBREF_i} & 1 \end{bmatrix} \quad (12)$$

Where $\gamma SREF_{i,f} = \alpha SREF_{i,f} + j\beta SREF_{i,f}$ is the propagation constant , $ZSREF_{i,f}$ and $LSREF_i$ are the characteristic impedance at frequency *'f'*, and physical length of the i'th series transmission line in the reference path and $\gamma BREF_{i,f} = \alpha BREF_{i,f} + j\beta BREF_{i,f}$ is the propagation constant , $ZBREF_{i,f}$ and $LBREF_i$ are the characteristic impedance at frequency *'f'*, and physical length of the i'th short circuited stub in the reference path.

After obtaining the elements of scattering matrix for the networks in the main path and reference path from the above relations, the error function in (5) must be minimized. To start the optimization, initial values must be considered for all variables. In the first design example, since input/output impedances are assumed to be 50 ohms, in order to apply

impedance matching conditions at center frequency, the initial physical lengths for all transmission lines located in the main path, are assumed to be a quarter wavelength at center frequency, i.e., 12 GHz, and initial characteristic impedances of all transmission lines in the main and reference paths are considered equal to 50 ohms. In order to set $\left(\angle\bar{S}Main_{21} - \angle\bar{S}REF_{21}\right)$ equal to 45° at center frequency, total physical length of the reference path is considered longer than main path in which the length difference becomes equivalent to - 45 degrees phase shift at the center frequency. Then the length of all transmission lines in the reference path are assumed the same. Optimization is done with the following flowchart.

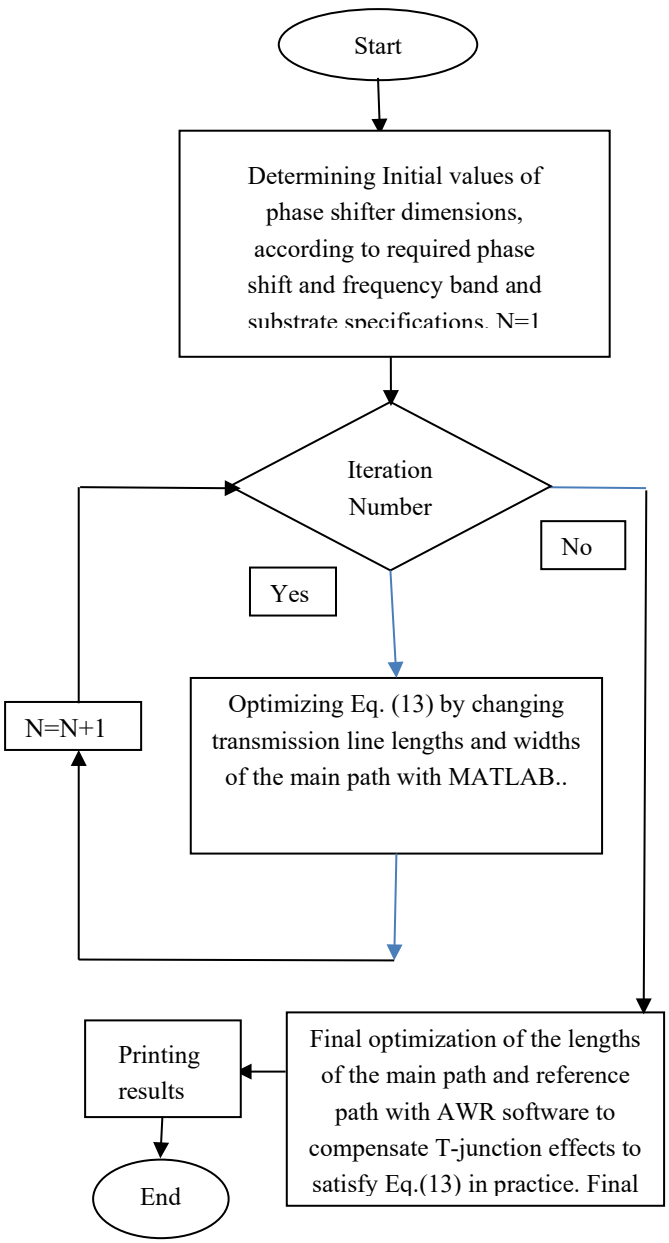

Table 1- dimensions of the designed phase shifter in the first design example obtained by computer program and fine tuning by EM softwares.

	*	**		*	**
WS_1	1.81	1.81	LS_1	4.27	4.18
WS_2	1.99	1.99	LS_2	4.35	3.4
WS_3	1.36	1.36	LS_3	5.98	7.24
WS_4	1.28	1.28	LS_4	6.03	7.23
WS_5	1.95	1.95	LS_5	3.73	2.61
WS_6	1.81	1.81	LS_6	4.25	3.8
WB_1	2.42	2.42	LB_1	4.09	3.75
WB_2	0.38	0.38	LB_2	3.31	3.64
WB_3	0.83	0.83	LB_3	3.26	2.95
WB_4	0.38	0.38	LB_4	4.10	4.93
WB_5	2.38	2.38	LB_5	4.14	3.95
$WSREF_1$	1.27	1.27	$LSREF_1$	4.43	5.49
$WSREF_2$	1.13	1.11	$LSREF_2$	7.62	8.34
$WSREF_3$	1.08	1.06	$LSREF_3$	7.45	7.01
$WSREF_4$	1.13	0.94	$LSREF_4$	7.66	7.82
$WSREF_5$	1.35	1.14	$LSREF_5$	3.87	5.39
$WBREF_1$	0.53	0.8	$LBREF_1$	3.99	4.12
$WBREF_2$	1.15	1.08	$LBREF_2$	3.69	3.65
$WBREF_3$	1.16	1.07	$LBREF_3$	3.77	4.32
$WBREF_4$	0.66	0.69	$LBREF_4$	3.88	4.56

* Circuit dimensions obtained by computer program (mm)
** Circuit dimensions after fine tuning with EM softwares

While optimization is running, some limitations are imposed on the transmission line lengths and widths, in such a way that the designed structure be practically implementable. This strategy, also prevents creation of T-junctions with large parasitic effects. The computer program is run on a core(TM) i3 system with CPU clock 2.13 GHz and after 5600 (s) (less than 2 hours), gives the results. The initial error function value is decreased from initial value 58458 to final value 5128. The circuit dimensions which are obtained by the program, are mentioned in table 1. The designed structure is then analyzed by AWR [20] and HFSS [21] full-wave EM softwares. To partially compensate the parasitic effects of T-junctions, assuming that main path transmission line widths be constant, physical lengths of transmission lines are fine tuned. The final dimensions are outlined in table 1.The simulated structure in HFSS software is shown in figure 8. This design is fabricated which its photograph is presented in figure 9. The scattering matrix of this design is measured using Agilent 8722ES Network Analyzer and the measurement results are compared with outcomes of full-wave simulations and computer program.

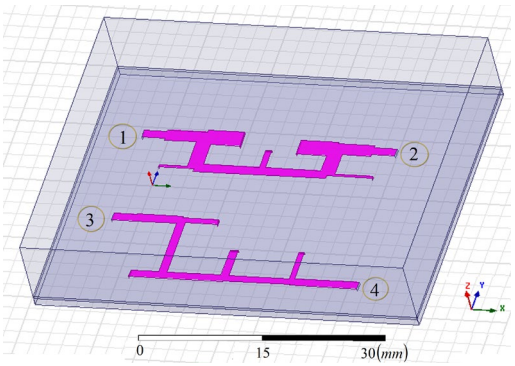

Figure 8- simulated structure for the first design example in HFSS software.

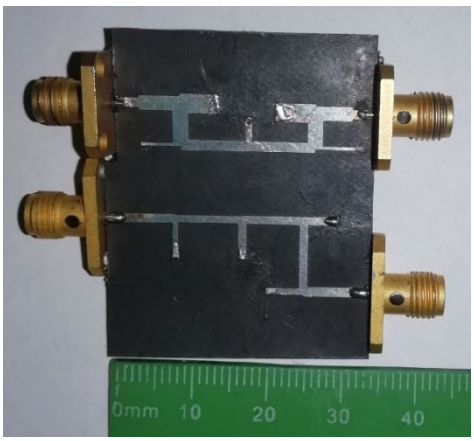

Figure 9- Photograph of the fabricated structure for the first design example.

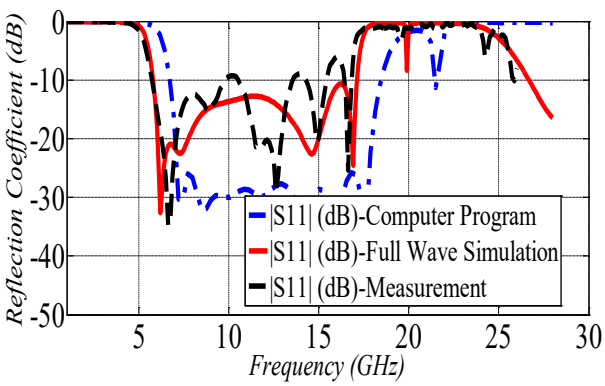

Figure 10- Computer program, full-wave simulation and measurement results for reflection coefficient of the main path.

Figures 10 to 13 are plots of computer program results, full-wave simulations and measurements for transmission and reflection coefficient for the main and reference paths respectively.

Figure 14 shows the comparing results of the computer program, full-wave simulation and measurement for the phase difference between the main and reference paths.

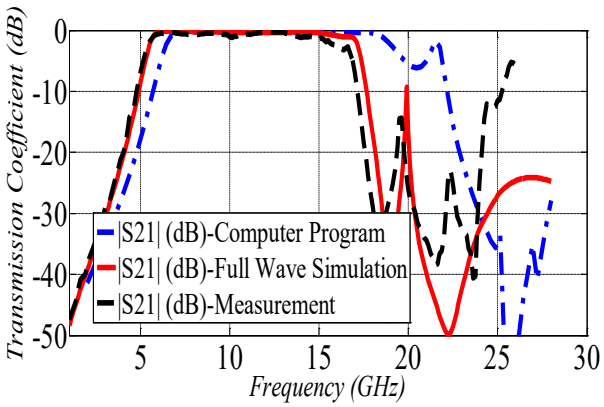

Figure 11- Computer program, full-wave simulation and measurement results for transmission coefficient of the main path.

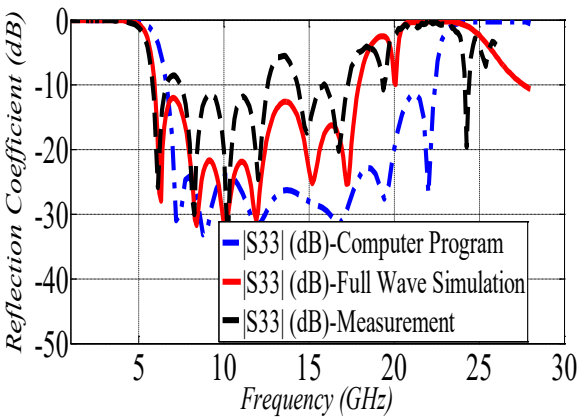

Figure 12- Computer program, full-wave simulation and measurement results for reflection coefficient of the reference path.

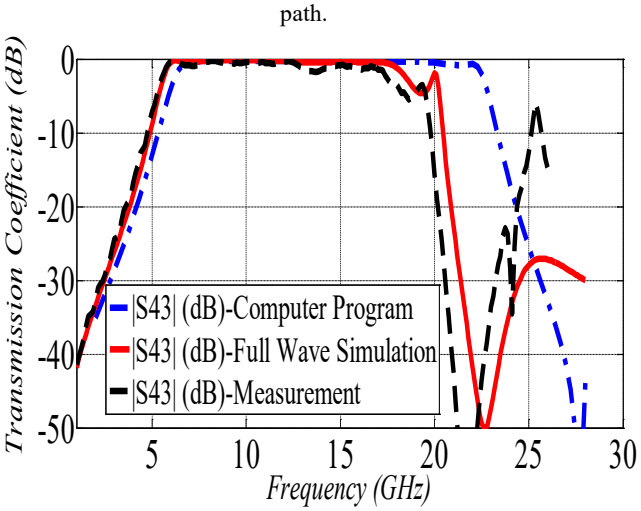

Figure 13- Computer program, full-wave simulation and measurement results for transmission coefficient of the reference path.

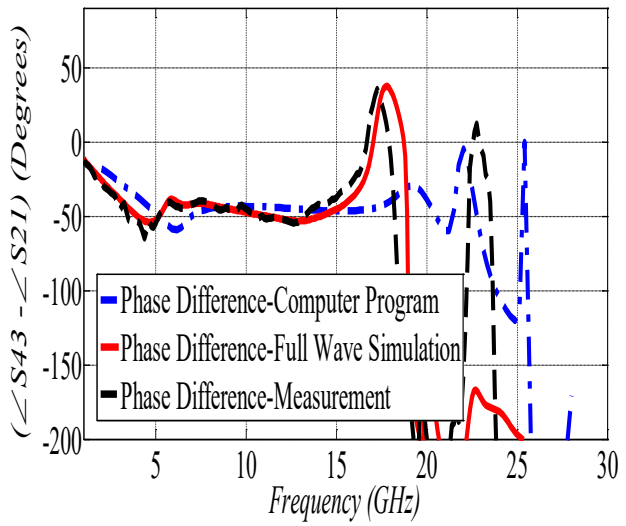

Figure -14 - Comparing results of the computer program, full-wave simulation and measurement for the phase difference between the main and reference paths.

In this design example, full wave simulation results for the main and reference paths reflection coefficient are better than -10 dB in the frequency range 6-18 GHz. The obtained full wave simulation phase shift in frequency band 5-17 GHz is $-45^{\circ} \pm 8^{\circ}$. Differences between full-wave simulation and circuit model analysis are due to the presence of parasitic effects in which are not completely modeled in the computer program and couldn't be exactly fine tune by EM software. Measurement results are in good correspondence with simulation results and minor discrepancies may arise from fabrication tolerances, connector losses, non-ideal short circuits, measurement errors, etc. As is stated in (5), in this special example, the emphasis on reducing the main path reflection coefficient is considered twice that of the reference path. In applications which the reflection coefficient of the reference path must be reduced in the same way as the main path, equal weighting factors must be considered in the error function and more sections may be included in the reference path.

IV- SECOND DESIGN EXAMPLE

In this example, we show the ability of the proposed method in considering nonstandard input/output impedances in designing phase shifters. In this example, it is assumed that impedances of input ports 1 and 3 be 50 ohms and the impedances of output ports 2 and 4 be 75 ohms. The phase difference between main and reference paths is aimed to be -90 degrees in the range 6-18 GHz. The main path and reference path structure of this example is seen in figures 15(a) and (b), respectively. Structures of the main path in the first and second

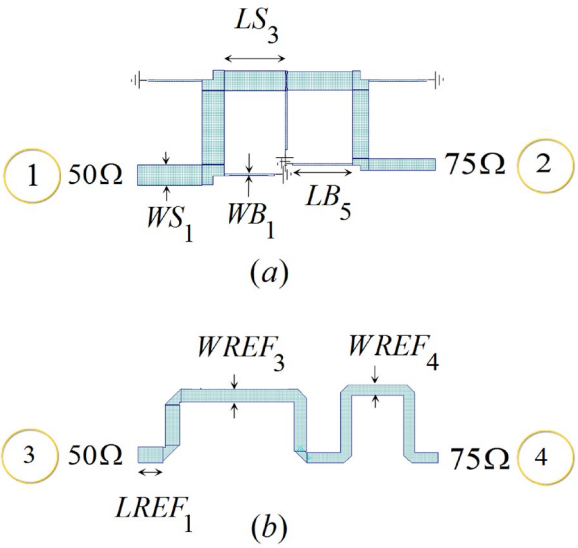

Figure 15- (a) and (b) show main and reference paths in the second phase shifter design example, respectively.

design example is similar and have 5 sections, but in current example, in the reference path, a 4 section impedance transformer is used. Dimensions of some exemplary transmission lines are illustrated in figure 15.

The following error function is employed to optimize circuit dimensions in this example,

$$Error = 4\sum_{n=1}^{40}\left[20\,log\left|\bar{S}Main_{11,n}\right| + 30\right]^2 + \sum_{n=1}^{40}\left[20\,log\left|\bar{S}REF_{11,n}\right| + 30\right]^2 + \sum_{n=1}^{40}\left[\left(\angle\bar{S}Main_{21,n} - \angle\bar{S}REF_{21,n}\right) - 90^{\circ}\right]^2 \quad (13)$$

Considering (13), the weighting factor of reflection coefficient reduction in the main path is considered 4 times more than the reference path. In here to start optimization, initial values are needed too. In the main path, the characteristic impedances of all transmission lines in short circuited stubs are assumed to be 50 ohms, and their electrical length is considered quarter a wavelength at the center frequency. These stubs so, are seen as open circuit at their inputs in the center frequency and would have no impact on input signal. Then to match input and output port impedances, the impedance of all series transmission lines are set equally as $\sqrt{ZL1 \times ZL2}$ and their electrical lengths are also selected equal to quarter a wavelength at center frequency. The main path is composed of 6 series transmission lines, so the phase delay from port 1 to 2 would be $-6 \times 90^{\circ} = -540^{\circ}$, at center frequency. The reference path, is realized using 4 series transmission lines. The initial characteristic impedances of all these lines are chosen equal to $\sqrt{ZL1 \times ZL2}$. In this

Table 2- Circuit dimensions of the designed phase shifter in the second example after optimization with computer program and fine tuning with EM softwares.

	*	**		*	*
WS_1	1.4	1.4	LS_1	4.40	4.40
WS_2	1.52	1.52	LS_2	5.03	5.03
WS_3	1.36	1.36	LS_3	4.19	4.19
WS_4	1.27	1.27	LS_4	4.45	4.45
WS_5	1.09	1.09	LS_5	4.67	4.67
WS_6	0.81	0.81	LS_6	4.54	4.54
WB_1	0.15	0.15	LB_1	4.48	3.40
WB_2	0.12	0.12	LB_2	4.46	3.71
WB_3	0.12	0.12	LB_3	4.84	4.03
WB_4	0.11	0.11	LB_4	4.68	3.99
WB_5	0.11	0.11	LB_5	4.63	4.11
$WREF_1$	1.10	1.10	$LREF_1$	4.49	1.69
$WREF_2$	0.97	0.97	$LREF_2$	4.60	2.80
$WREF_3$	0.85	0.85	$LREF_3$	18.29	11.89
$WREF_4$	0.73	0.73	$LREF_4$	4.62	18.20

* Circuit dimensions obtained by computer program (mm)
** Circuit dimensions after fine tuning with EM softwares (mm)

example, the relation $\left(\angle\bar{S}Main_{21,n} - \angle\bar{S}REF_{21,n}\right) = 90^\circ$ must be satisfied. So it is necessary that total phase delay in the reference path from port 1 to 2, becomes $-7\times 90^\circ = -630^\circ$, at center frequency. So initial lengths of all transmission lines in the reference path are set equally with $630^\circ / 4 = 157.5^\circ$. The computer program after running on the same computer system in previous design example, gives results after 1094 seconds; less than an hour. The initial error function is 5711224 and the final one is 364. The circuit dimensions after optimization with computer program are listed in table 2. The designed circuit is then simulated with full wave methods and to compensate parasitic effects of T-junctions and microstrip bends, dimensions of the structure is adjusted, in which corrections can be seen in table 2. Final dimensions are very close to the results of computer program and solely some of the transmission line lengths are altered. Figure16 presents the simulated structure in HFSS software.

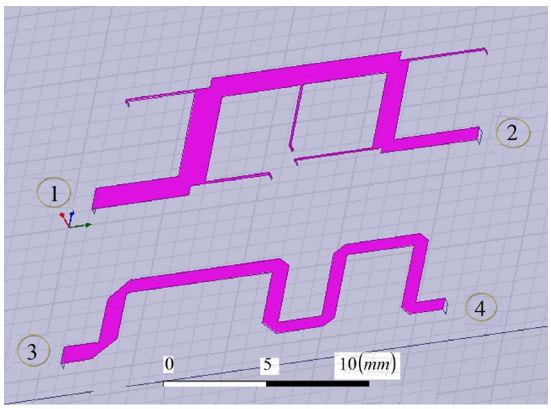

Figure 16- Simulated structure in HFSS software for the second design example.

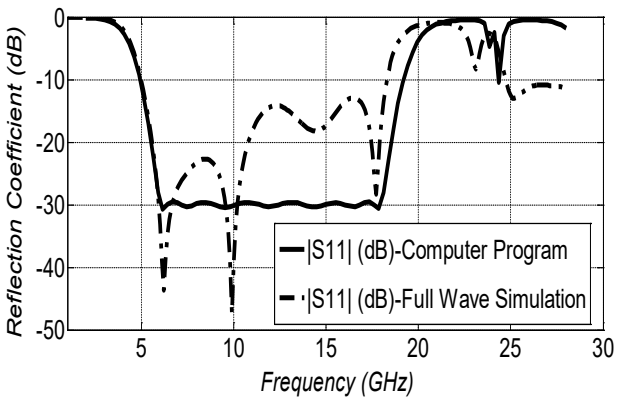

Figure 17- Computer program and full-wave simulation results of the reflection coefficient for the main path in the second design example.

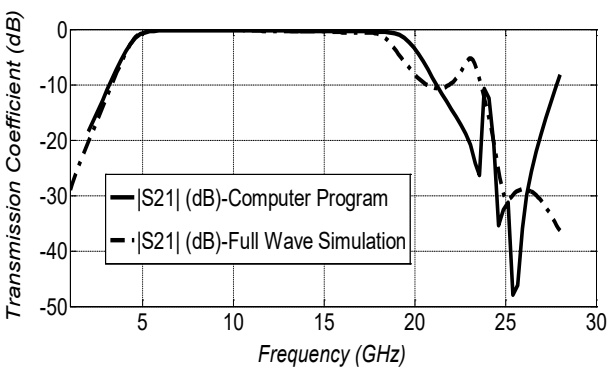

Figure 18- Computer program and full-wave simulation results of transmission coefficient for the main path in the second design example.

Computer program and full-wave simulation results of the reflection and transmission coefficients for the main and reference paths are respectively illustrated by figures 17,18,19,20. Figure 21 compares the phase difference among the main and reference paths obtained by computer program and HFSS simulations.

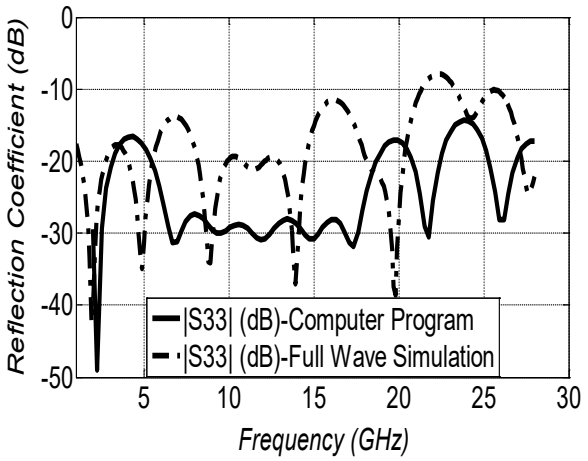

Figure 19- Computer program and full-wave simulation results of the reflection coefficients for the reference path in the second design example.

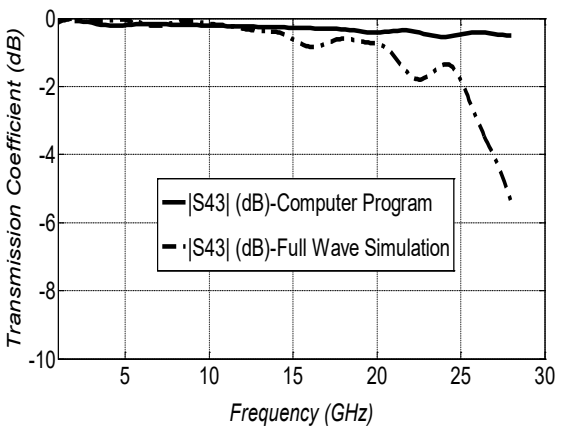

Figure 20- Computer program and full-wave simulation results of the transmission coefficient for reference path in the second design example.

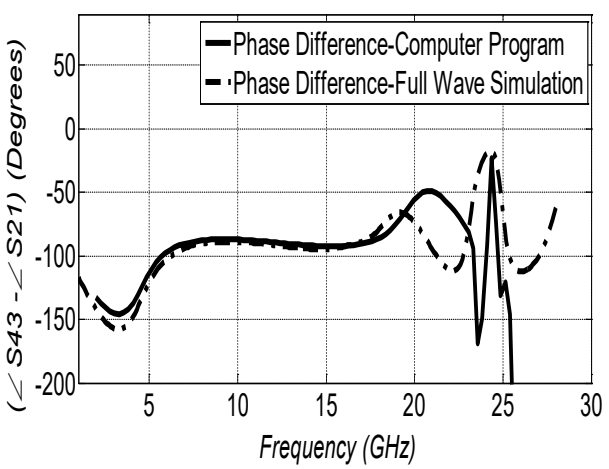

Figure 21- Computer program and full-wave simulation results of the phase difference between main and reference paths in the second design example.

In this example, full wave simulation of the reflection coefficient for the main and reference paths better than -10 dB in 6-18 GHz are acquired and the phase shift $-90^{\circ} \pm 8^{\circ}$ is obtained in 6.5-17.7 GHz. The designed circuit as well as creating almost constant phase shift with fractional bandwidth near to a hundred percent, successfully matches input 50 ohm source impedance to output 75 ohm load impedance. From the above figures it is clear that computer program results are very close to full wave simulations for the final fine tune structure. It is deduced that the written computer program works correctly and the existing differences between the results arise from parasitic effects that are ignored to be modeled completely in the written code. Any other phase shifters with phase shift values other than the above mentioned examples and with arbitrary source and load impedances in arbitrary frequency ranges may be designed by the written computer program in a relatively fast time.

V- CONCLUSION

In this paper, two UWB phase shifters with applications in 6-18 GHz were investigated. To realize these phase shifters, combinations of microstrip transmission lines and short circuit stubs were used in multi-section mode to provide required bandwidth. At the first design step, a computer program based on optimizing an error function was written, using exact closed form equations for microstrip transmission lines. To avoid complexity in the program, parasitic effects of T-junctions were ignored. After this initial design, which is relatively fast and exact, to overcome the parasitic effects of T-junctions, final fine tuning was done on the lengths of transmission lines using full wave simulations. To illustrate the proposed design method, two different design examples were depicted. In the first design, input/output impedances were 50 ohms and desired phase shift difference was assumed to be -45 degrees. In the second design, a more general structure with unequal source and load impedances were considered in the case of -90 degrees phase shift difference. In both designs, acceptable results were obtained from the full wave simulation and measurements which satisfy design goals for transmission and reflection coefficients and phase shift differences in the design bandwidth

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