International Journal Of
Industrial Electronics Control and Optimization
Print ISSN: 3517-2645
Online ISSN: 3568-2645
Homepage: https://ieco.usb.ac.ir/

Quantum-Dot Cellular Automata-Based and High-Speed Design of New Structure for Fault-Tolerant 7-Input Majority Gate

Farzaneh Jahanshahi Javaran[1]| Somayyeh Jafarali Jassbi[1] | Hossein Khademolhosseini[1,2]| Razieh Farazkish[3]

Department of Computer Engineering, SR.C., Islamic Azad University, Tehran, Iran.[1]
Department of Computer Engineering, Bey.C., Islamic Azad University, Beyza, Iran.[2]
Department of Computer Engineering, BT.C., Islamic Azad University, Tehran, Iran.[3]
Corresponding author's email: khademolhosseini@iau.ac.ir

Article Info

Article type:
Research Article

Article history:
Received: 16-April-2025
Received in revised form: 10-August-2025
Accepted: 28-October-2025
Published online: 23-Sep-2026

Keywords:
Nano,
Basic gates,
7-input Majority Gate,
Fault-tolerant,
QCADesigner.

ABSTRACT

As the field of nanotechnology rapidly advances and the need for faster processing in smaller dimensions grows, so does the integration of Very Large-Scale Integration (VLSI) technology. These difficulties include things like large-scale area needs, high power consumption, and low operating speeds, which call for new approaches to lessen these constraints. Developed and implemented at the nano-based, Quantum-Dot Cellular Automata (QCA) technology presents itself as a viable way around these obstacles. The advent of QCA technology heralds our entry into the nano-scale realm, where the advantages of enhanced processing speeds, reduced dimensions, and minimal power consumption become manifest. This article focuses on the 7-input Majority Gate, a fundamental component in QCA technology, distinguished by its fault-tolerant characteristics. The primary objective is to present the design and simulation of this key gate within the context of QCA technology. Noteworthy among the merits of the 7-input Majority Gate is its capacity to implement logic gates with a greater number of inputs, consolidating multiple functionalities within a single gate. QCADesigner and QCAPro software have simulated the given gate, and the results demonstrate the exact and correct operation of the gate. This gate generates an output signal with a 0.25-clock-cycle delay and occupies an area of 0.03 μm² with 66 quantum cells. The simulation results demonstrate the precision of the circuit's operation. Additionally, basic fault-tolerant gates such as 4-input AND and 4-input OR using a 7-input fault-tolerant Majority Gate have been suggested to illustrate the proper operation of the new gate.

I. Introduction

Deep nanoscale technologies will bring current Complementary Metal-Oxide Semiconductor (CMOS) technology closer to its scaling limit [1]. The growing degrees of variance in each facet of a nanometer design provide certain challenges for CMOS technology at nanoscales [2]. Parallelism is a common technique used to improve the efficiency of logical systems. But new nanotechnologies need to be considered to improve the system's overall performance. One of the most exciting emerging technologies is Quantum-dot Cellular Automata (QCA), which provides a novel approach to computation and information transformation in addition to providing a solution at the nanoscale [3]. Since the Majority Gates are the fundamental building element of QCA circuits, there has been a lot of interest in the effective construction of QCA circuits using Majority Gates; nevertheless, some of these are not extensible or feasible [4]. According to several research studies, QCA can be used to construct memory and general-purpose computing circuits [5-8]. A key element in building QCA circuits is the majority, as each circuit can only be accomplished with the use of majority and inverter gates. Therefore, it is crucial to build a majority in QCA as effectively as possible [9].

On the other hand, by reducing the dimensions of the parts, the sensitivity of the circuit is increased, and quantum circuits are more vulnerable to the occurrence of defects and environmental radiation, and failures will be one of the important issues at the architectural level. It is a fact that

nano-architectures must be able to tolerate defects. So far, a large number of 3-input and 5-input fault-tolerant gates have been introduced, and of course, circuits have been designed with these 3-input and 5-input fault-tolerant gates [10, 11]. But the fault-tolerant 7-input Majority Gate is less designed; therefore, the research in this particular field seems appropriate. In this article, we are going to design and implement a 7-input Majority Gate that can tolerate faults, which is considered one of the basic gates in QCA technology [12]. The construction of fault-tolerant 7-input Majority Gates in QCA is a relatively unexplored field when considering the existing state of affairs. This paper highlights the need to focus research efforts on this particular area of QCA technology, where there is still room to improve fault tolerance in critical components [13, 14].

With the growing need for low-energy consumption and ultra-dense circuits, the fault-tolerant 7-input Majority Gate proposed here has large potential to be incorporated in QCA-based large-scale systems. It can be applied to memory arrays where multi-input logic functionality is essential, arithmetic processing units in nano-ALUs, error-resilient control systems, radiation-hardened computing systems like those used in aerospace technology, medical implants, or military-grade devices.

Therefore, acknowledging its critical significance as one of the foundational gates within the QCA framework, this article aims to contribute to this emerging subject by providing a thorough design and implementation of a fault-tolerant 7-input Majority Gate. Its purposeful focus on strengthening the fault tolerance of the 7-input Majority Gate (a crucial component of QCA technology) is what makes this research novel. The study aims to close a clear gap in the current state of research by addressing the shortcomings in existing designs and suggesting a fault-tolerant version. Given the growing applications of QCA technology and the critical need for reliable and fault-tolerant components in the rapidly changing field of nanoscale computing, this project is especially relevant and timely. In addition to trying to address current issues, the proposed 7-input Majority Gate also hopes to open the door for more dependable and robust QCA circuits. This research adds to the fundamental understanding of QCA technology by clarifying the fault-tolerant mechanisms and design complexities. It also provides useful information for the creation of fault-tolerant circuits within the larger framework of nanoscale computing. This paper's uniqueness is summarized as follows:

- Created the first fault-tolerant *7-input* Majority Gate
- Examining the suggested fault-tolerant gate for faults such as cell omission, cell displacement, cell misalignment, and extra-cell deposition.
- Using the QCAPro tool, compute and analyze the power consumption of the suggested structure.
- Using the proposed fault-tolerant *7-input* Majority Gate, propose fault-tolerant fundamental gates such as *4-input* AND and *4-input* OR.

This paper's structure will be as follows. Section 2 provides an overview of QCA technology, including QCA cells, QCA wires, fundamental QCA gates, clocking, different types of faults, and related operations. Section 3 proposes fault-tolerant 7-input Majority Gates. The proposed structure in Section 4 suggests fault-tolerant versions of fundamental gates such as *4-input AND, and 4-input OR* in QCA technology. Finally, the article is finished in Section 5.

II. Background

Introduction to QCA technology

The cell is the main component in QCA technology. The QCA cell consists of four cavities placed next to each other in a square shape. The QCA cell has two extra electrons, which can move freely between holes [15]. In general, *6* different states are available for *2* electrons to be placed in *4* holes. All these *6* states are not stable because, due to the Coulomb force between electrons, they are always in a state that has the greatest distance from each other, as shown in Figure 1. Therefore, the stable states are established when the holes are diagonally occupied, which creates two structures. These two structures display two poles, *+1 and -1*, which in calculations, we attribute logical values of *1 and 0* to them, respectively [13].

Fig. 1. QCA cell [16].

Another important issue in this technology is wiring. Not only is the Coulomb force established between the electrons inside a cell, but also each cell affects the adjacent cells. If two cells are located next to each other, they are always in a position where the Coulomb force is minimized. An array of contiguous cells can be used to transmit a logical value like a wire to transmit information [17, 18]. A linear array of standard cells can transmit binary data. In general, two wiring methods have been used in QCA, as shown in Figure 2. The first method, which is considered the wiring standard in QCA, is created by placing standard cells together; the input signal is applied from one side to the first cell, and due to electron repulsion, the polarization created in the first cell is transferred to the cells [19]. Adjacent ones are transmitted one after the other, and thus the signal is propagated in the first part of the wire. Finally, the incoming signal can be seen on the other side of the wire. The second method that is used in wiring is by using *45-degree* cells [20, 21]. In this way, the

cells are placed together with a polarity between *-1 and +1*, so a wire is created using these cells, and the signal can be transmitted. Another benefit of this technology is its capacity to cross wires. Since the cables are arranged in separate layers in this instance, they don't negatively impact one another. Additionally, there is no signal loss when using the same wire for multiple outputs [17, 18, 22].

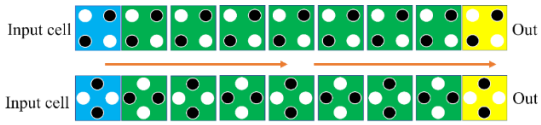


Fig. 2. Two types of QCA wire [23]

In addition to the above, clocking is very important in this technology. A QCA circuit cannot function properly without a clock schedule. In QCA, we must use a schedule that allows each cell to maintain its current state and not react to the change of state of the neighboring cells. The clock is an electronic factor that controls the movement of electrons inside the cell [24]. What the clock does is keep one set of cells in a certain polarization to allow other cells to make the appropriate changes [25]. The way it is controlled is that if information reaches a part of the circuit that must be combined with several other inputs and produce the desired output, if other inputs arrive later in that part of the circuit, it prevents information from spreading in that part until other inputs arrive. The existence of a clock creates synchronization in different parts of the circuit. Each clock signal is divided into four phases: switch, hold, release, and rest.

1. Switch Phase: During this phase, the opposing forces that hinder electron movement within each cell begin to intensify, making it increasingly difficult for electrons to move.
2. Maintenance Phase: In this stage, the forces that obstruct electron flow within the cell have reached their peak, resulting in a stable position for the electrons.
3. Release Phase: At this point, the blocking forces start to diminish, allowing electrons to be gradually released.
4. Resting Phase: In this phase, the cell exhibits no polarity, enabling electrons to move freely throughout the cell.

All cells in a clock domain have the same phase. This means that a clock phase occurs when the clock domain passes through four different phases, which is what the clock does [26]. The clocking in four phases in QCA is shown in Figure 3.

In addition to the above, the two basic gates in the QCA technology are the inverter gate and the Majority Gate, which can be used to design any circuit that is possible in this technology. In the Majority Gate, the output always shows the majority of the inputs; that is why we call it the majority function, the output is the inverse function of the majority of the inputs [27]. The types of Majority Gates in this technology are *3-input, 5-input, and 7-input*. Figure 4 shows *3, 5, and 7-input* Majority Gates and an inverter gate.

Defects in QCA

Also, one of the important things in this technology is the possibility of a fault. Defects in the placement stage can have a big impact on the system's functionality and dependability when it comes to QCA technology [28-30]. These flaws cover a wide range of anomalies or mistakes that could occur when arranging or placing quantum dots, which are the basic building blocks of QCA circuits. Potential flaws in the placement phase could include differences in the distance between quantum dots or misalignment of the dots themselves. These flaws could be the consequence of fabrication process restrictions, environmental variables, or manufacturing errors. It is imperative to address and mitigate these placement-related defects because they have the potential to affect both the accuracy of quantum computations and the overall performance of QCA-based devices. To increase the dependability and usefulness of QCA technology, scientists and engineers working in this area try to create strong methods for locating, stopping, and fixing these flaws [28-30]. The types of possible defects in the placement stage of this technology include:

- Cell deletion: It is a defect where a cell is left out of the circuit (Figure 5 (a))
- Cell displacement: defects that quantum cells move in their original direction (Figure 5 (b))
- Cell rotated: It is a defect in which the cell rotates in proportion to the adjacent cells in such a way that the direction of the cell changes (Figure 5 (c))
- Extra-cell: It is a defect in which one or a number of extra cells may be added to the circuit in the process of placing cells (Figure 5 (d)) [7].

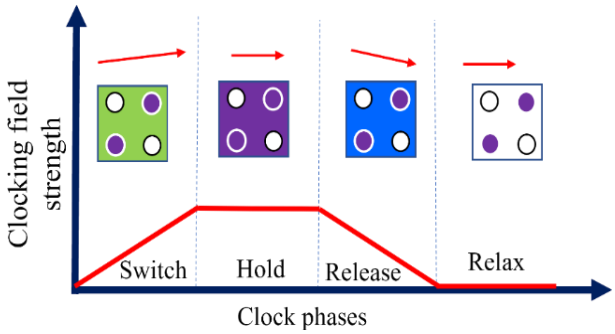


Fig. 3. Clocking in QCA technology [26]

Related works

In reference [31], a new 7-input Majority Gate is designed in QCA. The gate proposed in this article is designed in one layer and with a *0.25 clock cycle*. This gate is designed with *19* quantum cells, and is shown in Figure 7 (a). Also, the power dissipation map of this gate is shown in Figure 7 (a).

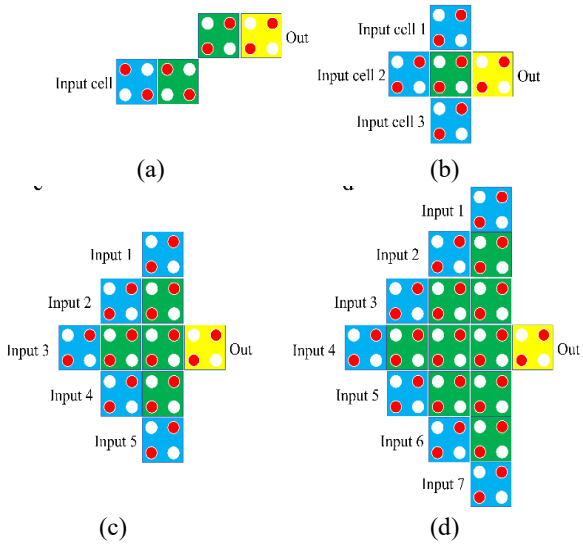


Fig. 4. QCA basic gates: (a) QCA inverter, (b) a three-input Majority Gate, (c) a five-input Majority Gate, and (d) a seven-input Majority Gate [3]

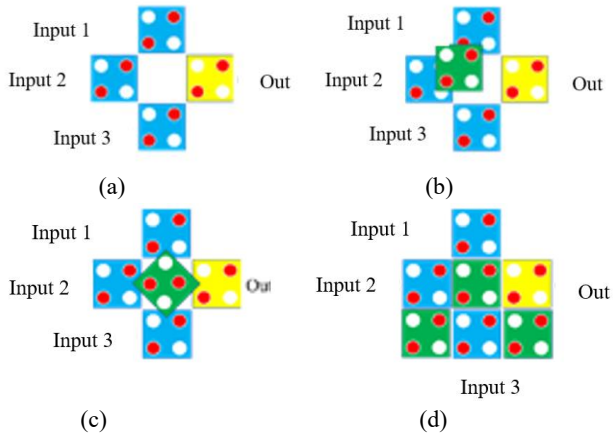


Fig.5. Types of defects in QCA technology: (a) cell omission, (b) cell displacement, (c) cell rotation, and (d) extra-cell deposition [7]

This gate's fault tolerance of less than *12%* indicates that it is quite prone to malfunctions. When the fault tolerance level is below a critical threshold in real-world terms, it can be said that the gate is not fault-tolerant. In this case, the gate's low fault tolerance points to a significant susceptibility to errors or disruptions, highlighting the need for additional advancements or substitute approaches to raise its dependability in practical uses.

In reference [32], a 7-input Majority Gate with a symmetrical structure is proposed. This research article presents a gate that is carefully constructed in a single layer and runs at *0.25 clock phase*. According to the reference, this gate's architectural layout consists of *24* cells in total. But a critical observation reveals that this specific gate, as shown in Figure 7 (b), is not intrinsically fault-tolerant. The power dissipation map of this gate is shown in Figure 7 (b). One important thing to note about this gate is that it doesn't have fault tolerance, which means that errors or disruptions could compromise its dependability in real-world scenarios. Its intricate design, in particular its reliance on a single clock phase and single-layer structure, makes it more prone to malfunctions.

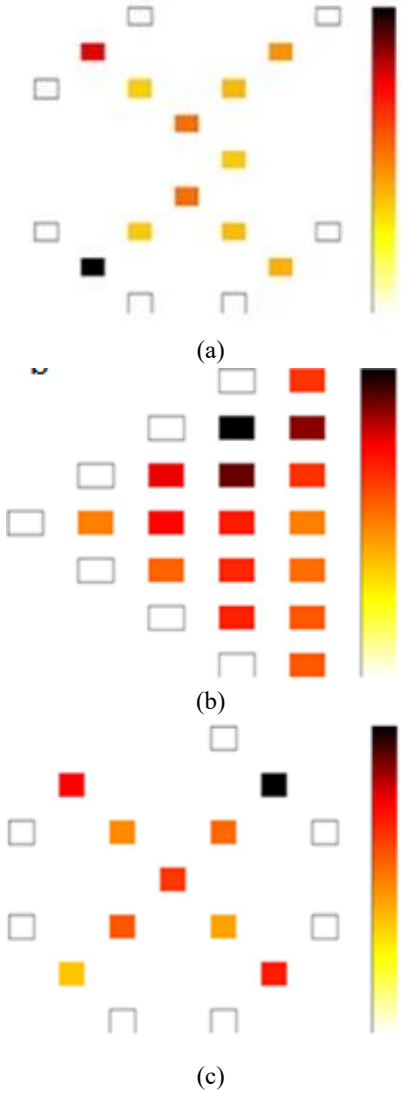


Fig.6. Power consumption analysis: (a) Power dissipation map of the in [31], (b) Power dissipation map of the in [32], and (c) Power dissipation map of the in [33]

In the minority gate, the output is the inverse function of the majority of the inputs. The proposed 7-input minority gate in reference [33] is shown in Figure 7 (c). This research article introduces a novel construction, the 7-input minority gate, which is made up of *16* cells that are synchronized within a small *0.25* clock cycle. Figure 6 (c) displays this gate's power dissipation map. The structural design consists of seven input cells, one output cell, and a middle configuration of eight cells. Note that this gate has a fault tolerance level of less than *13.75%,* even with its intricate design and effective clock cycle. The gate is considered to have no substantial error tolerance in practice when the fault tolerance figure falls below a critical threshold. Put differently, this means that the

gate is more prone to errors than is reasonable, which highlights the need to strengthen its fault tolerance.

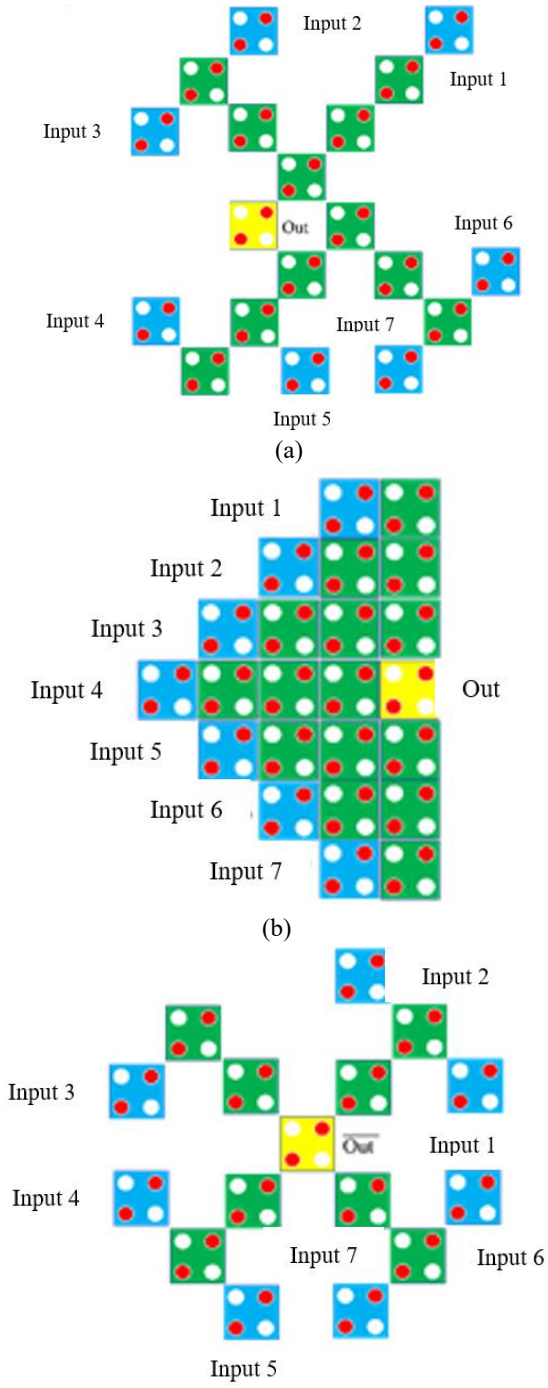


Fig.7.Three types of 7-input Majority Gate: (a) 7-input Majority Gate proposed in [31], (b) 7-input minority gate proposed in [32], and (c) 7-input Majority Gate in [33]

III. The proposed fault-tolerant 7-input Majority Gate

In QCA technology, a fault-tolerant 7-input Majority Gate is a state-of-the-art development in the realm of quantum computing. In comparison to classical computing systems, quantum computation at the quantum level (*QCA*) enables faster and more complex operations by applying the principles of quantum mechanics to computing. It is a revolutionary approach to computing. This particular part of a 7-input Majority Gate is made to process seven input signals and generate an output using the majority logic principle. In the field of QCA technology, this gate's fault-tolerant nature is essential because it shows how well it can tolerate and lessen the effects of any faults, mistakes, or disturbances that might occur while it is operating. Therefore, in this article, a fault-tolerant 7-input Majority Gate is presented. Figure 8 represents the proposed fault-tolerant 7-input Majority Gate with *66* quantum cells in an occupied space of *0.03* μm^2. All input and output cells are designed and implemented in one layer, and no other layers are needed to access them. Proper arrangement of the input cells and the length of the wires structurally have led to the coordinated effects, and accordingly, the fault-tolerant 7-input Majority Gate output. The correct output response is received after 0.25 clock cycles.

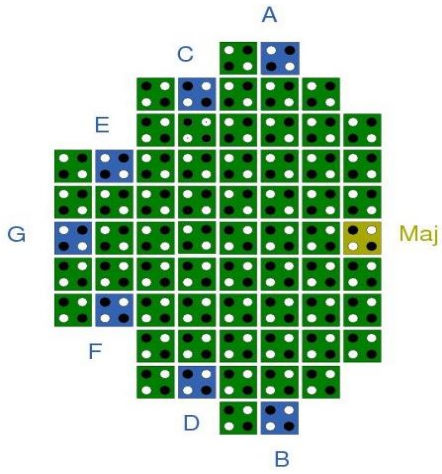


Fig.8.The QCA layout of the proposed fault-tolerant 7-input Majority Gate

Also, we have designed *4-input AND* and *4-input OR* gates with this gate as follows to show the efficiency of the presented gate. One of the main advantages of the 7-input Majority Gate is the ability to implement logic gates (*4-input AND, 4-input OR, 4-input NAND, and 4-input NOR* in QCA technology) with more inputs under the capability of one gate. The fault-tolerant *4-input AND, 4-input OR* can be designed within the fault-tolerant *7-input Majority Gate* by fixing three of the inputs to *0 and 1* as shown in Figure 9. When three inputs are set to *0*, the output of the function is *1* only when the other four inputs are *1*; otherwise, the output of the function is *0*. Therefore, the system will behave like an *"AND"* operator. A gate *"OR"* with four inputs can be designed by fixing three of the inputs to *+1* polarization. Functionality of these gates is presented in Eqs (1) and (2):

$$AND(A,B,C,D)=AB.CD=MV7(A,B,C,D,0,0,0) \quad (1)$$

$$OR(A,B,C,D)=A+B+C+D=MV7(A,B,C,D,1,1,1) \quad (2)$$

To ensure fault tolerance, structural redundancy was introduced in the design by adding the overlapping logical paths and the placement of cells with the potential to furnish logical compensation for local failures. In contrast to duplication or voting methods, this design emphasizes spatial distribution and logical symmetry that ensures functionality even when some cells are deleted or displaced. This system maintains gate functionality without unnecessary area or complexity overhead.

IV. Simulation software, results, energy dissipation analysis, and defect analysis

To thoroughly assess and validate the suggested circuit layouts and their associated functionality, we have utilized the sophisticated simulation tool QCADesigner version 2.0.3, which is designed especially for QCA circuits [8, 34]. With the aid of this simulation tool, we can evaluate the complex dynamics of QCA circuits and closely examine the proposed circuit's performance in a variety of scenarios. To guarantee the precision and dependability of the outcomes in the context of bistable approximation—a crucial component of QCA circuit simulations—a set of well-selected parameters has been provided. These specifications call for an 18 nm cell size and the use of *50,000* samples to provide a strong statistical analysis. Notably, the precise value of *0.0000100* is chosen for the convergence tolerance, highlighting the level of accuracy needed to achieve convergence during the iterative simulation process. In addition, several parameters that control the simulation environment have been carefully defined. The parameters used include the radius of effect (65 nm), relative permittivity (12.9), clock high (9.8e-22 J), clock low (3.8e-23 J), clock shift (0), clock amplitude factor (2.0), layer separation (11.5 nm), and maximum iterations per sample (100). Notably, most of these parameters are the QCADesigner defaults, guaranteeing uniformity and conforming to accepted practices in QCA simulations. Through the utilization of QCADesigner features and prudent parameter configuration, our goal is to perform a comprehensive analysis that examines the behavior of the suggested circuit in various scenarios [8, 34]. Ensuring the precision, dependability, and thorough comprehension of the suggested QCA circuit's performance attributes requires the careful selection and adjustment of these simulation parameters.

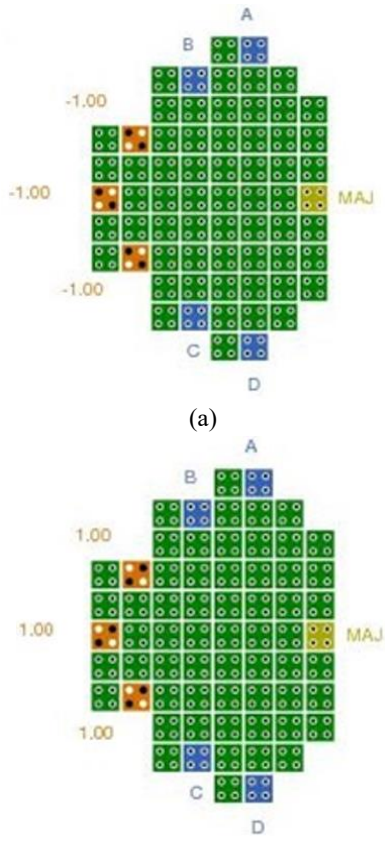


Fig.9. (a) The QCA layout of proposed fault-tolerant 4-input AND gate, and (b) The QCA layout of proposed fault-tolerant 4-input OR gate

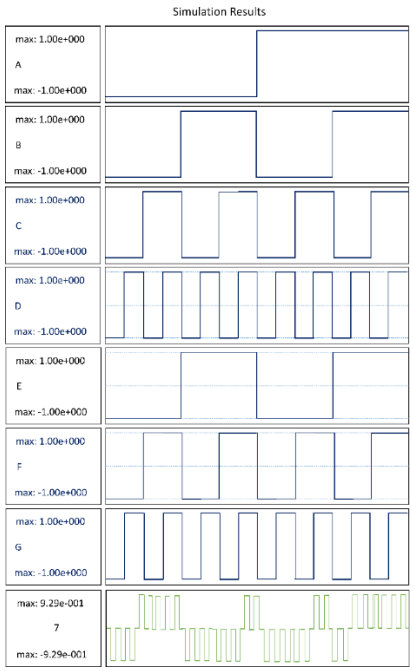
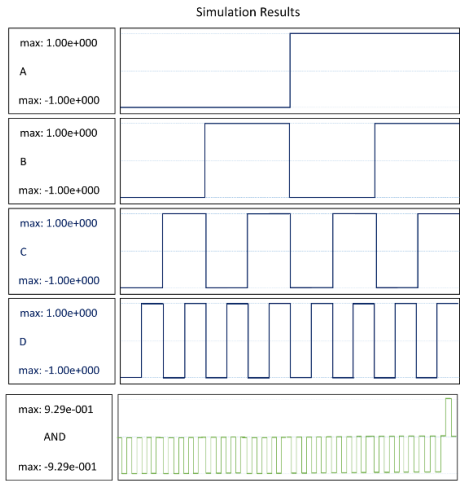


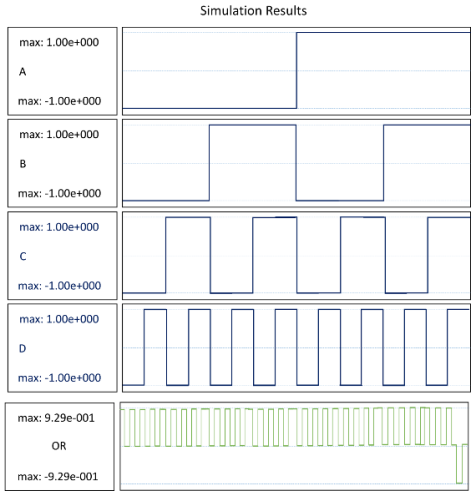
Fig.10.The simulation results of the proposed fault-tolerant 7-input Majority Gate

The simulation results from the QCADesigner simulation motors indicate the proper operation of the proposed Majority Gate for all possible inputs. The test vectors were applied sequentially to the inputs, and the results were examined by each motor separately. The matching of the waveforms revealed the correct operation of the design. Figure 10 represents the simulation result with the *Coherence Vector* simulation motor. Additionally, Figure 11 shows the simulation results for an *OR* and an *AND* gate with four inputs that are fault-tolerant. The figure makes it clear that all

potential inputs have been applied to the gates and that the gates have produced the expected and correct outputs, demonstrating the proper operation of the newly introduced gates.



(a)



(b)

Fig.11. (a) The simulation results of the proposed fault-tolerant 4-input AND gate, and (b) The simulation results of the proposed fault-tolerant 4-input OR gate

Considering that the *7-input gate* designed in this article is the first fault-tolerant *7-input Majority Gate*, therefore, no comparison has been made to this gate; however, Table 1 compares the 7-input minority and Majority Gates designed in previous articles with the gate proposed in this article. In this table, the proposed gate has been compared with the circuits designed in previous articles in terms of fault-tolerance percentage.

Also, to better confirm the accuracy of the presented fault-tolerant 7-input Majority Gate, this gate has been tested in QCAPro software. To calculate polarization error and non-adiabatic switching power loss in QCA circuits, a new modeling tool called QCAPro has been developed. When designing QCA circuits, the tool estimates highly erroneous cells using a quick approximation-based technique. In addition to providing an upper bound on power consumed, QCAPro estimates the power loss in a QCA circuit for clocks with sharp transitions, which lead to non-adiabatic operations. When an input switching operation is occurring in a QCA circuit, QCAPro can be used to estimate the maximum, minimum, and average power losses. The QCAPro software can measure the energy consumption of the fault-tolerant 7-input Majority Gate at three levels of *0.5 EK, 1 EK, and 1.5 EK* at *2.0 K*. The power dissipation map of the proposed Majority Gate with 0.5 EK is illustrated in Figure 12, and more energy dissipation details of the gate are listed in Table 2. Also, in this table, a comprehensive comparison has been made between the presented design and the best previous designs.

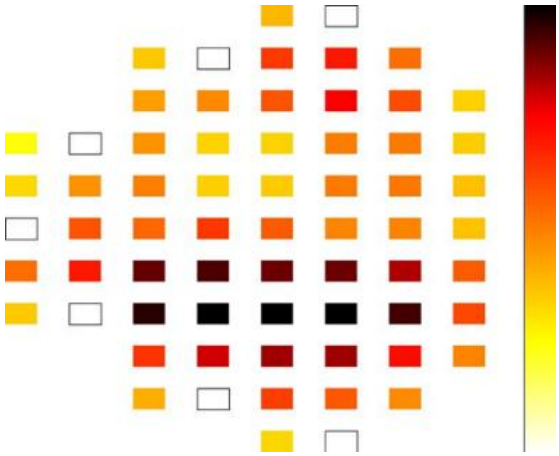


Fig.12.Power dissipation map of the proposed 7-input Majority Gate with $0.5\ E_k$

TABLE I. A comparison of the fault-tolerant 7-input Majority Gate and other similar gates

Design in	Area (μm^2)	Accessibility to the output	Accessibility to the input	Cell deletion	Cell [illegible]	Cell Rotation	Extra Cell	Average Fault [illegible]
propose	34444	Yes	Yes	38 %	89 %	38 %	93 %	64.5 %
Jahanshahi Javaran, Jafarali Jassbi [31]	24564	Yes	Yes	20 %	50 %	40 %	46.1%	11.525%
Navi, Chabi [32]	16284	Yes	Yes	15 %	48 %	52 %	61.1%	15.2 %
Mohammadi, Navi [33]	19044	Yes	No	12 %	39 %	37 %	55 %	13.75%

TABLE II. A comparison of the 7-input Majority Gate's energy dissipation

	Avg. leakage energy dissipation (eV)			Avg. switching energy dissipation (eV)			Total energy dissipation (eV)		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
Proposed	0.00918	0.03186	0.06350	0.17189	0.16451	0.15527	0.18107	0.19637	0.21877
Jahanshahi Javaran, Jafarali Jassbi [31]	0.00192	0.00365	0.00542	0.03468	0.05621	0.07932	0.12481	0.10355	0.10782
Navi, Chabi [32]	0.02996	0.03445	0.04138	0.04234	0.05483	0.08965	0.10258	0.08791	0.0389
Mohammadi, Navi [33]	0.00157	0.00294	0.00438	0.00345	0.00489	0.07814	0.10215	0.04258	0.00512

The comparison results show more energy consumption in the presented plan than in the previous plans. This is due to the high number of cells provided in the design, which has high tolerance, but the previous designs are not fault-tolerant.

Cell Deletion Analysis

Table 3 shows the results of evaluating the proposed gate's tolerance to cell deletion. By comparing the output waveforms of simulations with and without individual cell deletions (Figure 13), 22 of 58 cells could be deleted without affecting the output. This indicates a 38% tolerance to cell deletion ((22/58) × 100%).

Cell Displacement Analysis

Table 4 presents the results of the displacement fault analysis. Each of the 18 device cells was tested for displacement tolerance in four directions (North, South, East, West). Only cells 26 and 40 produced incorrect results. Therefore, the device cell fault tolerance is 89% ((16/18) × 100%).

Cell Rotation Analysis

Cell rotation evaluation was also performed in QCADesigner by changing the cell type from 90 degrees to 45. As shown in Table 5, all 58 cells were examined, and only 22 exhibited sufficient tolerance to this fault. Therefore, the proposed gate demonstrates poor tolerance to rotated cells, with a tolerance percentage of 38%.

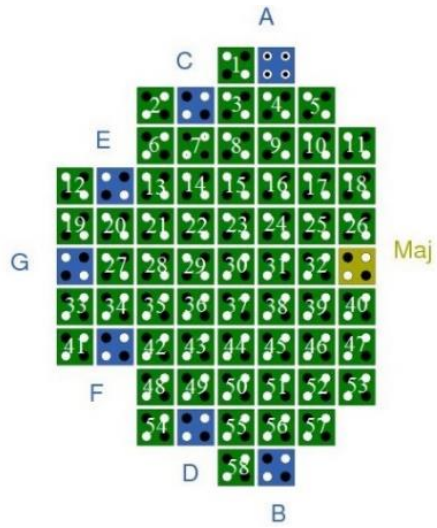


Fig.13.The proposed fault-tolerant 7-input Majority Gate (numbered cells)

TABLE III. The output of the proposed structure against the single-cell deletion defect.

Removed cell	Output	Removed cell	Output
1	MV7	29	Incorrect
2	MV7	31	Incorrect
3	Incorrect	32	Incorrect
4	Incorrect	33	MV7
5	MV7	34	MV7
6	MV7	35	Incorrect
7	Incorrect	36	Incorrect
8	Incorrect	37	Incorrect
9	Incorrect	38	Incorrect
10	MV7	39	Incorrect
11	MV7	40	Incorrect
12	MV7	41	MV7
13	Incorrect	42	Incorrect
14	Incorrect	43	Incorrect
15	Incorrect	44	Incorrect
16	Incorrect	45	Incorrect
17	MV7	47	MV7
18	MV7	48	MV7
19	MV7	49	Incorrect
20	MV7	50	Incorrect
21	Incorrect	51	Incorrect
22	Incorrect	52	MV7
23	Incorrect	53	MV7
24	Incorrect	54	MV7
25	Incorrect	55	Incorrect
26	Incorrect	56	Incorrect
27	Incorrect	57	MV7
28	Incorrect	58	MV7

TABLE IV. Outcomes of the permitted cell displacement in the proposed design

Cell	North	South	East	West
1	∞	-	-	∞
A	-	-	<=2	-
2	∞	-	-	∞
C	<=2	-	-	-
5	∞	-	∞	-
6	-	-	-	∞
11	∞	-	∞	-
12	∞	-	-	∞
E	<=4	-	-	-
18	-	-	<=10	-
19	-	-	-	∞
26	-	-	<=1	-
G	-	-	-	<=6
Maj	-	-	<=1	-
33	-	-	-	∞
40	-	-	<=1	-
41	-	∞	-	∞
F	-	<=4	-	-
47	-	-	<=10	-
48	-	-	-	∞
53	-	∞	∞	-
54	-	∞	-	∞
D	-	<=2	-	-
57	-	∞	∞	-
58	-	∞	-	∞
B	-	-	<=2	-

Extra-Cell Deposition Analysis

In order to analyze the extra-cell fault, the process starts by adding cells all around the proposed Majority Gate, as shown in Figure 14. The resulting waveforms are compared to the fault-free ones. Represents the possible places, and Table 6 lists the results of the process. Only in cells *5* and *28*, incorrect results produced. Consequently, the fault tolerance percentage for extra-cell can be calculated as (28/30) × 100, resulting in 93%.

Testing under Noisy and Thermal Environments

To assess the stability of the proposed 7-input Majority Gate under real-world operation conditions, additional simulations were run using QCAPro for both thermal fluctuation (between 0 K and 350 K) and injected environmental noise regimes. The simulations revealed that the gate operates correctly with extremely low output errors in all 128 input combinations. This confirms the fault-tolerant character of the gate under actual nanoscale operating variations.

Trade-off Analysis: Cell Count vs. Power vs. Fault Tolerance

Though the design is more power hungry due to a higher number of quantum cells, the improvement in fault tolerance is considerable. In comparison with previous designs with smaller-sized power footprints, our design achieves a fault tolerance of up to 93% under circumstances of additional-cell faults and performs within tolerable margins under deletion and displacement faults. Such a compromise is justified in applications where fault resiliency is worth more than the lowest power, i.e., mission-critical or high-radiation environments. Table II has been accordingly adjusted to offer complete and comparative values.

TABLE V. The results of the proposed structure against single-cell rotation defect.

Rotated cell	**Output**	**Rotated cell**	**Output**
1	MV7	30	Incorrect
2	MV7	31	Incorrect
3	Incorrect	32	Incorrect
4	Incorrect	33	MV7
5	MV7	34	MV7
6	MV7	35	Incorrect
7	Incorrect	36	Incorrect
8	Incorrect	37	Incorrect
9	Incorrect	38	Incorrect
10	MV7	39	Incorrect
11	MV7	40	Incorrect
12	MV7	41	MV7
16	Incorrect	42	Incorrect
17	MV7	46	MV7
18	MV7	47	MV7
19	MV7	48	MV7
20	MV7	49	Incorrect
21	Incorrect	50	Incorrect
22	Incorrect	51	Incorrect
23	Incorrect	52	MV7
24	Incorrect	53	MV7
25	Incorrect	54	MV7
26	Incorrect	55	Incorrect
27	Incorrect	56	Incorrect
28	Incorrect	57	MV7
29	Incorrect	58	MV7

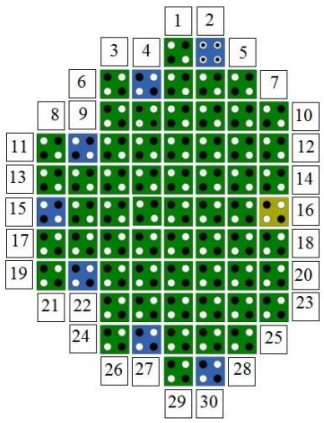


Fig.14.All instances of extra-cell deposition around the proposed gate

TABLE VI. Analysis of additional cell defects.

Additional cell	Output	Additional cell	Output	Additional cell	Output
1	MV7	11	MV7	21	MV7
2	MV7	12	MV7	22	MV7
3	MV7	13	MV7	23	MV7
4	MV7	14	MV7	24	MV7
5	Incorrect	15	MV7	25	MV7
6	MV7	16	MV7	26	MV7
7	MV7	17	MV7	27	MV7
8	MV7	18	MV7	28	Incorrect
9	MV7	19	MV7	29	MV7
10	MV7	20	MV7	30	MV7

V. Conclusion and future works

Scientists have been actively searching for new approaches to address persistent issues in Very Large-Scale Integration (VLSI) systems as the field of nanotechnology develops quickly and the demand for faster processing in smaller dimensions rises. These challenges include things like high power consumption, low operating speeds, and large-scale area requirements, which necessitate new strategies to reduce these limitations. Quantum-Dot Cellular Automata (*QCA*) technology, developed and applied at the nanoscale, offers itself as a potential solution to these challenges. Its growing popularity can be attributed to its special features, which include eliminating electric current and the need for capacitive components, both of which make the design much simpler. With the introduction of QCA technology, we are moving closer to the nanoscale, where the benefits of faster processing, smaller size, and lower power consumption become apparent. According to the above scenarios and the relevance of Majority Gates, a novel fault-resistant *7-input Majority Gate* has been assembled for the first time in QCA technology employing hardware redundancy. In addition to structural analysis, the study of gate tolerance was done using the four fault types: cell omission, cell displacement, cell rotation, and extra-cell deposition, and the accuracy of gate operation was assessed using the *QCADesigner* simulation tool. The proposed Majority Gate is composed of *66* cells, which occupy *0.03* μm^2 with *0.25 clock cycle* propagation delay. Instead of providing a single averaged fault tolerance measure, individual fault tolerance rates are provided for each fault type: cell deletion (38%), displacement (89%), rotation (38%), and extra-cell insertion (93%). This initial analysis provides a more accurate indication of fault behavior and avoids misleading statistical summaries. A fault is "tolerated" when the output is functionally correct for at least 90% of input combinations under that fault. Also, for the first time, various types of fault-tolerant basic gates, such as *4-input AND, 4-input OR*, in QCA technology are implemented. Future research will expand on the current study's contributions by optimizing and expanding fault-tolerant basic gates in QCA technology. To increase the versatility and dependability of these gates in nanoscale circuit design, researchers will investigate a variety of types, including QCA basic gates. By addressing both theoretical and practical aspects of fault tolerance in QCA-based systems, the goal is to advance the field and lay the groundwork for future VLSI technologies that will be more reliable and efficient.

In summary, the novel fault-tolerant 7-input majority gate is highly resilient to various types of faults without compromising sound logic functionality. Although it requires more quantum cells and thus marginally more power, the trade-off is worthwhile for high-reliability applications. Future work will focus on layout optimization to continue reducing power and area, including adding the fault-tolerant design to 9-input and hybrid majority gates and exploring fabrication-aware designs. This gate's performance and robustness make it especially well-suited for QCA-based systems in space, military, or biomedical applications where reliability is the top priority.

REFERENCES

[1] Ahmadpour, S.S., M. Mosleh, and S. Rasouli Heikalabad, Robust QCA full adders using an efficient fault tolerant five input majority gate. International Journal of Circuit Theory and Applications, 2019. 47(7): p. 1037-1056.

[2] Raj, M., L. Gopalakrishnan, and S.B. Ko, Reliable SRAM using NAND-NOR gate in beyond CMOS QCA technology. IET Computers & Digital Techniques, 2021. 15(3): p. 202-213.

[3] Safaiezadeh, B., et al., Design and simulation of efficient combinational circuits based on a new XOR structure in QCA technology. Optical and Quantum Electronics, 2021. 53: p. 1-16.

[4] Li, Z., S. Zhang, and B.O. Mohammed, An efficient three-level nano-design for reversible gate using quantum dot-cellular automata with cost analysis. Materials Science and Engineering: B, 2023. 294: p. 116526.

[5] Chen, X., et al., Accurate reliability evaluation using quantum dot cellular automata probabilistic transfer matrix. Micro & Nano Letters, 2014. 9(2): p. 77-82.

[6] Norouzi, M., S.R. Heikalabad, and F. Salimzadeh, A reversible ALU using HNG and Ferdkin gates in QCA nanotechnology. International Journal of Circuit Theory and Applications, 2020. 48(8): p. 1291-1303.

[7] Seyedi, S. and N.J. Navimipour, Design and evaluation of a new structure for fault-tolerance full-adder based on quantum-dot cellular automata. Nano communication networks, 2018. 16: p. 1-9.

[8] Walus, K., et al., QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE transactions on nanotechnology, 2004. 3(1): p. 26-31.

[9] Jain, V., et al., Comprehensive and Comparative Analysis of QCA based Circuit Designs for Next Generation Computation. ACM Computing Surveys, 2023.

[10] Ahmadpour, S.-S., et al., An ultra-efficient design of fault-tolerant 3-input majority gate (FTMG) with an error probability model based on quantum-dots. Computers and Electrical Engineering, 2023. 110: p. 108865.

[11] Roohi, A., et al., A symmetric quantum-dot cellular automata design for 5-input majority gate. Journal of Computational Electronics, 2014. 13: p. 701-708.
[12] Farazkish, R. and K. Navi, New efficient five-input majority gate for quantum-dot cellular automata. Journal of Nanoparticle Research, 2012. 14: p. 1-6.
[13] Jafarali Jassbi, S., et al., Design and analysis of a fault tolerant 3-input majority gate in quantum-dot cellular automata. Journal of Advances in Computer Research, 2019. 10(4): p. 27-36.
[14] Majeed, A.H., et al., A new 5-input majority gate without adjacent inputs crosstalk effect in QCA technology. Indonesian Journal of Electrical Engineering and Computer Science, 2019. 14(3): p. 1159-1164.
[15] Majeed, A.H., et al., Optimal design of RAM cell using novel 2: 1 multiplexer in QCA technology. Circuit world, 2020. 46(2): p. 147-158.
[16] Reis, D.A., et al. A methodology for standard cell design for QCA. in 2016 IEEE International Symposium on Circuits and Systems (ISCAS). 2016. IEEE.
[17] Graziano, M., et al., Characterisation of a bis ferrocene molecular QCA wire on a non ideal gold surface. Micro & Nano Letters, 2019. 14(1): p. 22-27.
[18] Roohi, A., H. Thapliyal, and R. DeMara, Wire crossing constrained QCA circuit design using bilayer logic decomposition. Electronics Letters, 2015. 51(21): p. 1677-1679.
[19] Ahmadpour, S. and N. Jafari Navimipour, A New Nano-Design of 16-bit Carry Look-Ahead Adder Based on Quantum Technology. Physica Scripta, 2023.
[20] Jahanshahi Javaran, F., et al., Robust QCA Full Adders Using a Novel Fault Tolerant Five-Input Majority Gate. International Journal of Industrial Electronics Control and Optimization, 2024. 7(2): p. 99-108.
[21] Motalebi, F. and S. Sayedsalehi, Design of Low Power Full-Adder Circuit Using Quantum-dot Cellular Automata. International Journal of Industrial Electronics Control and Optimization, 2022. 5(1): p. 99-108.
[22] Rasmi, H., et al., Novel Efficient Scalable Design of Full-Adder in Atomic Silicon Dangling Bonds (ASDB) Technology. Physica Scripta, 2023.
[23] Seyedi, S. and N.J. Navimipour, An optimized design of full adder based on nanoscale quantum-dot cellular automata. Optik, 2018. 158: p. 243-256.
[24] Vankamamidi, V., M. Ottavi, and F. Lombardi. Clocking and cell placement for QCA. in 2006 sixth IEEE conference on nanotechnology. 2006. IEEE.
[25] Seyedi, S. and N.J. Navimipour, Designing a three-level full-adder based on nano-scale quantum dot cellular automata. Photonic Network Communications, 2021. 42: p. 184-193.
[26] Seyedi, S. and N.J. Navimipour, An efficient structure for designing a nano-scale fault-tolerant 2: 1 multiplexer based on quantum-dot cellular automata. Optik, 2022. 251: p. 168409.
[27] Khan, A., et al., Behaviors of QCA inverter due to cell displacement and temperature variation. arXiv preprint arXiv:2310.09734, 2023.
[28] Bahadori, G., M. Houshmand, and M. Zomorodi-Moghadam, Design of a fault-tolerant reversible control unit in molecular quantum-dot cellular automata. International Journal of Quantum Information, 2018. 16(01): p. 1850010.
[29] Poorhosseini, M. and A.R. Hejazi, A fault-tolerant and efficient XOR structure for modular design of complex QCA circuits. journal of Circuits, Systems and Computers, 2018. 27(07): p. 1850115.
[30] Seyedi, S. and N.J. Navimipour, A fault-tolerance nanoscale design for binary-to-gray converter based on QCA. IETE Journal of Research, 2023. 69(5): p. 2991-2998.
[31] Jahanshahi Javaran, F., et al., Computational Circuit Design Using a New Seven-Input Majority Gate in Quantum-dot Cellular Automata. Journal of Intelligent Procedures in Electrical Technology, 2022: p. 21-34.
[32] Navi, K., A.M. Chabi, and S. Sayedsalehi, A novel seven input majority gate in quantum-dot cellular automata. International Journal of Computer Science Issues (IJCSI), 2012. 9(1): p. 84.
[33] Mohammadi, H., K. Navi, and M. Hosseinzadeh, An efficient quantum-dot cellular automata full adder based on a new convertible 7-input majority-not gate. IETE Journal of Research, 2023. 69(1): p. 558-566.
[34] Aralikatti, S. QCA Designer: A simulation and Design Layout Tool for QCA based Nano Domain Computing Architectures. in 2020 Second International Conference on Inventive Research in Computing Applications (ICIRCA). 2020. IEEE.

Farzaneh Jahanshahi Javaran was born in Kerman, Iran She a PhD student in Computer Systems Architecture from Islamic Azad University, Science and Research Department. University of Science and Research is a prestigious university in the field of computer systems architecture in Iran. Currently, her researching the design of fault-tolerant majority gates in quantum cellular automata. Her current research interests include quantum dot cellular automata, fault tolerance.

Sommayeh Jafarali Jassbi was born in Tehran, Iran, in 1982. She received the MSc degree in computer architecture engineering in 2007, and the Ph.D. degree in computer architecture engineering in 2010 from the Islamic Azad University, Science and Research Branch. In 2010, she joined the Department of computer engineering, Islamic Azad University Science and Research Branch. She became an associate professor in 2011. Her interests are cloud computing, internet of things, wireless sensor network and computer architecture and cryptography. She was head of computer department in 2012. Now she is selected as a head of computer department again. She was also an active member of young researcher club from 2004. She has written, translate and published several professional books and paper in her fields.

Hossein Khademolhosseini received B.Sc. degree in computer engineering in 2008 from Shiraz University, Shiraz, Iran. He also received his M.Sc. and Ph.D. degree in computer architecture at Department of Computer Engineering, Science and Research Branch of Islamic Azad University, Tehran, Iran, in 2011 and 2016, respectively. He is currently an assistant professor with the Department of Computer Engineering, Islamic Azad University, Beyza Branch. His research interests are computer arithmetic, photonic NoC and electronics with emphasis on QCA and VLSI.

Razieh Farazkish received the B.S. degree in computer engineering from the IAU, Central Tehran Branch (2007) and the M.S. (2009) and Ph.D. (2012) degrees in computer engineering from the IAU, Science and Research Branch. In 2012, she joined the Department of Computer Engineering, IAU, South Tehran Branch, as a Professor. Her current research interests include quantum-dot cellular automata, fault tolerance, nanoelectronic circuits, nano computing, testing and design of digital systems.