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A New Soft Switching Dual-input High Step-up Converter for Renewable Energy Systems

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ABSTRACT

Objective: This paper presents a new converter featuring an auxiliary circuit configuration, designed to facilitate soft switching conditions while minimizing the number of components used. This auxiliary circuit is innovatively developed to achieve zero voltage switching (ZVS) and effectively recover snubber energy on the input side, thereby enhancing the converter efficiency. Furthermore, the deliberate integration of coupled inductors into the converter's design significantly boosts its gain while reducing voltage stress on the switching components. The modular architecture of the auxiliary circuit allows for adding circuit branches and increasing power capacity without requiring extra components for its auxiliary circuit. To evaluate the performance of the proposed converter, extensive simulations were performed using PSPICE software, along with the construction of a laboratory prototype capable of operating at 170 W. The alignment between the experimental results and simulation data strongly supports the theoretical analysis, illustrating the converter's potential for efficient power conversion in renewable energy systems.

Nomenclature

f	Switching frequency	DIC	Dual Input Converter
n	Turn ratio of coupled-inductor	L_M	Magnetizing inductor
I_{sw}	Final current of the switch before turning it off	I_{LM}	Magnetizing inductor current
V_{sw}	Final voltage across switch before turning on	C_S	Snubber capacitor
t_r	Switch current rise time	L_K	Leakage inductance
t_f	Switch current fall time	D	Duty cycle
V_D	Diode voltage	Po	Output power
T	Switching cycle period	PWM	Pulse width modulation
V_o	Output voltage	ZVS	Zero voltage switching
Vin	Input voltage	ZCS	Zero current switching
Vs	Switch voltage		

I. Introduction

Recently, rising environmental issues and the depletion of fossil fuels have significantly boosted the demand for renewable energy sources like wind turbines, photovoltaic (PV) panels, and fuel cells (FCs). PV sources generate low-amplitude DC voltage, requiring high step-up DC-DC converters in DC-AC systems to boost this voltage to the desired level. The classical DC-DC boost converter is an essential solution for voltage boosting [1]-[4]. However, the

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efficiency of PV systems is generally decreased by the use of converters, highlighting the need for high-efficiency converters [5-7]. Such converters are preferred over PV systems due to their high efficiency, low cost, and ability to achieve high voltage gains with fewer circuit elements. Achieving high efficiency and voltage gain in these converters typically requires several passive components, which increases the circuit's volume. To optimize converter size and efficiency and reduce input current ripple, new step-up converters are designed that employ techniques involving coupled inductors, transformers, and multiplier units [3]. Recent proposals include a new high step-up DC-DC converter topology that allows for high voltage conversion ratios with low voltage stress on power switches. This topology, combined with alternative designs that integrate SEPIC and boost converters, aims to address challenges such as high-power losses in passive components and semiconductors, as well as reverse recovery issues that decrease efficiency. Novel approaches include multi-input structures integrating energy from different sources, enhancing reliability and power generation [8]-[10].

Dual Input Converters (DICs) are categorized into isolated, non-isolated, and semi-isolated types based on their design and operational characteristics. Isolated DICs feature magnetic coupling between input and output ports through transformers or coupled inductors, incorporating multiple switches but offering favorable soft-switching conditions. In contrast, non-isolated DICs lack galvanic isolation between the inputs and outputs, often resulting in the loss of soft-switching capabilities and generally lower voltage gains [11]-[13]. These converters, however, offer advantages like a reduced number of semiconductor components and enhanced power density. Semi-isolated DICs uniquely isolate only one port (typically the output) via a transformer, enhancing voltage gain and providing soft switching due to the transformer's leakage inductance. Similar to non-isolated converters in that the input ports are not isolated from each other, semi-isolated DICs manage to use fewer semiconductors while providing satisfactory power sharing.

The converter presented in [14] features two interleaved boost converters combined with a Cockcroft–Walton (CW) multiplier cell. By incorporating additional stages of the CW multiplier, the voltage gain of the converter is increased. However, a substantial rise in the number of stages increases conduction losses, thereby reducing the overall efficiency. To address this, a multi-input converter with a novel voltage multiplier was proposed in [16]. A technique for cascading boost converters was presented in [17] and [18], allowing each input source to independently transfer power to the output. Additionally, an active clamping circuit was employed to achieve soft-switching conditions, though it resulted in significant circulating current.

In [20], the introduction of series diodes and unidirectional current flow in the auxiliary circuit helped to reduce the current stress on the switches. Nevertheless, the primary challenges of this converter include limited voltage gain and high voltage stress on the main switches.

This paper introduces a new dual-input converter, characterized by its high efficiency and the capability to redirect snubber energy back to the input. This innovative design reduces voltage stress on switches and solves the diode reverse recovery issue by implementing ZCS conditions for them.

II. Description of the Proposed Converter

The proposed dual-input converter has an innovative auxiliary circuit with a switch Sa, an auxiliary inductor La, two auxiliary diodes D_{a1} and D_{a2}, and two snubber capacitors C_{s1} and C_{s2}. This converter uses two coupled inductors L_1-L_2 and L_3-L_4 to increase the gain. In addition, two capacitors C_1 and C_2 are connected in series to the coupled inductors. This converter also has diodes D_1 and D_2 and D_{o1} and D_{o2}. Capacitor C_o and two main switches S_1 and S_2 are the main components of the converter. Switches S_1 and S_2 are turned on simultaneously, but due to the difference in their input voltages, they have different duty cycles. The auxiliary switch is turned on shortly before switches S_1 and S_2 and is turned off once they are turned on. Figure 1 demonstrates a schematic view of the proposed converter.

A. Operation of Proposed Dual-input Converter

The proposed dual-input converter has eight operation modes, which are explained. For the simplicity of the analysis of circuit operation, it is assumed that the output voltage and capacitors C_1 and C_2 are constant. Magnetizing inductors' current is also supposed to be constant in one cycle. Fig. 2 demonstrates the switching waveforms theoretically and Fig. 3

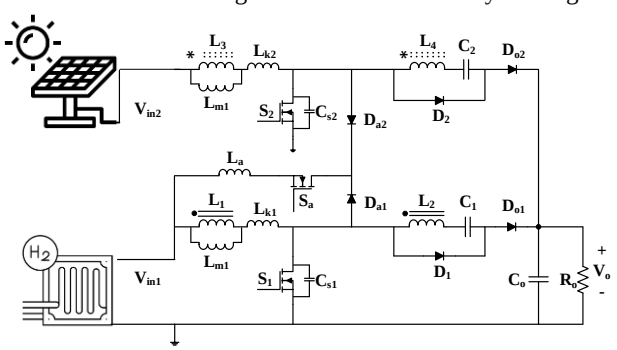


Fig. 1. A schematic view of the proposed converter

illustrates the equivalent circuits of different modes of converter.

Before the first status, it is assumed that both switches S_1 and S_2 are off and diodes D_{o1} and D_{o2} conduct, so the energy of magnetizing inductors L_{m1} and L_{m2} is transmitted to output through these diodes.

The first mode: This condition starts when the auxiliary switch S_a is turned on. Due to the existence of the auxiliary inductor L_a in series with this switch, its current is increased linearly because the constant voltage V_o-V_c-V_{in} across it drops. In this mode, diodes D_{a1} and D_{a2} are on, and as the current L_a is increased, the current of diodes D_{o1} and D_{o2} decreases. When current L_a reaches the value of I_{in1}+I_{in2}, diodes D_{o1} and D_{o2} are turned off under ZC conditions.

The second mode: When D_{o1} and D_{o2} are turned off, inductor L_a resonates with capacitors C_{S1} and C_{S2} and fully discharges the energy of the capacitors. In this mode, capacitors C_1 and C_2 also start to be charged from the path of diodes D_1 and D_2.

The third mode: At the beginning of this mode, capacitors C_{S1} and C_{S2} are fully discharged and body diodes S_1 and S_2 are turned on. Since then, these switches will be turned on under zero voltage switching (ZVS) conditions. Also, the inverse voltage – V_{c1}/n drops across L_a and its current decreases linearly so that it reaches zero at the end of this mode. In the first to third modes, when the auxiliary switch is turned on, both snubber capacitors start to discharge at the input through the auxiliary inductor (L_a), so the energy of the snubber circuit is not dissipated and is transferred to the input.

The fourth mode: This mode starts when D_{a1} and D_{a2} are turned off under ZC conditions. When switch Sa is turned off, the auxiliary circuit is fully disconnected from the converter.

The fourth mode: This mode starts when D_{a1} and D_{a2} are turned off under ZC conditions. When switch Sa is turned off,

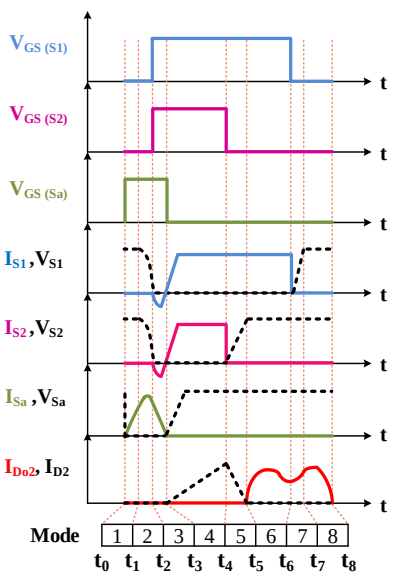


Fig.2 Theoretical main waveforms of the proposed converter

the auxiliary circuit is fully disconnected from the converter. Both switches are active, causing the magnetizing inductances L_{m1} and L_{m2} to charge linearly, while the load current is provided by the output capacitor Co.

The fifth mode: In this mode, switch S_2 is turned off under ZV conditions due to the presence of snubber capacitor C_{S2}, and capacitor C_{S2} is charged by current I_{Lm1} up to voltage $V_o/(n+1)$.

The sixth mode: When C_{S1} voltage reaches Vo/(n+1), diode D_2 is turned off and diode D_{o2} is turned on. This mode continues until S_1 is turned off.

The seventh mode: When S_1 is turned off, capacitor C_{S1} is charged linearly by I_{Lm2} current to reach Vo/(n+1). This mode ends when D_{o1} is turned on and D_1 is turned off.

The eighth mode: When D_1 is turned off, this mode starts and the energy of inductors L_{m1} and L_{m2} starts to be discharged at the output. This mode concludes when the auxiliary switch is turned back on.

III. Analysis of the Proposed Dual-input Converter

This section analyzes the dual-input converter. Firstly, the converter gain and voltage stress on semi-conductor elements are calculated parametrically, and then the passive elements of the design equations of the proposed dual-input converter are explained.

B. The Converter Voltage Gain:

By deriving the volt-second balance equation and applying Kirchhoff's Voltage Law (KVL) in the output loop, we have:

$$-V_{in} + V_{L1} + nV_{L1} - V_C + V_o = 0 \quad (1)$$

$$V_{L1} = \frac{V_{in} + V_{C1} - V_o}{n+1} \quad (2)$$

$$DTV_{in} + (1-D)T(V_{in} - \frac{V_o}{n+1}) = 0 \quad (3)$$

$$V_{C1} = nV_{in} \quad (4)$$

$$\frac{V_o}{V_{in}} = \frac{n+1}{1-D} \quad (5)$$

Fig. 4 demonstrates the gain diagram for different values of the turn ratio.

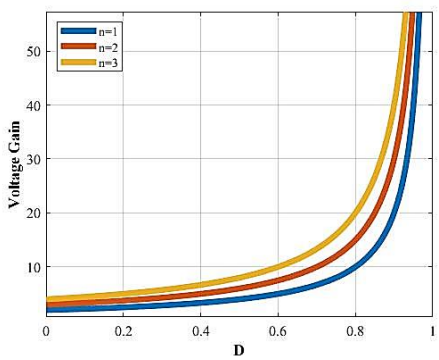


Fig. 4 The gain diagram of the proposed converter for different values of turn ratio.

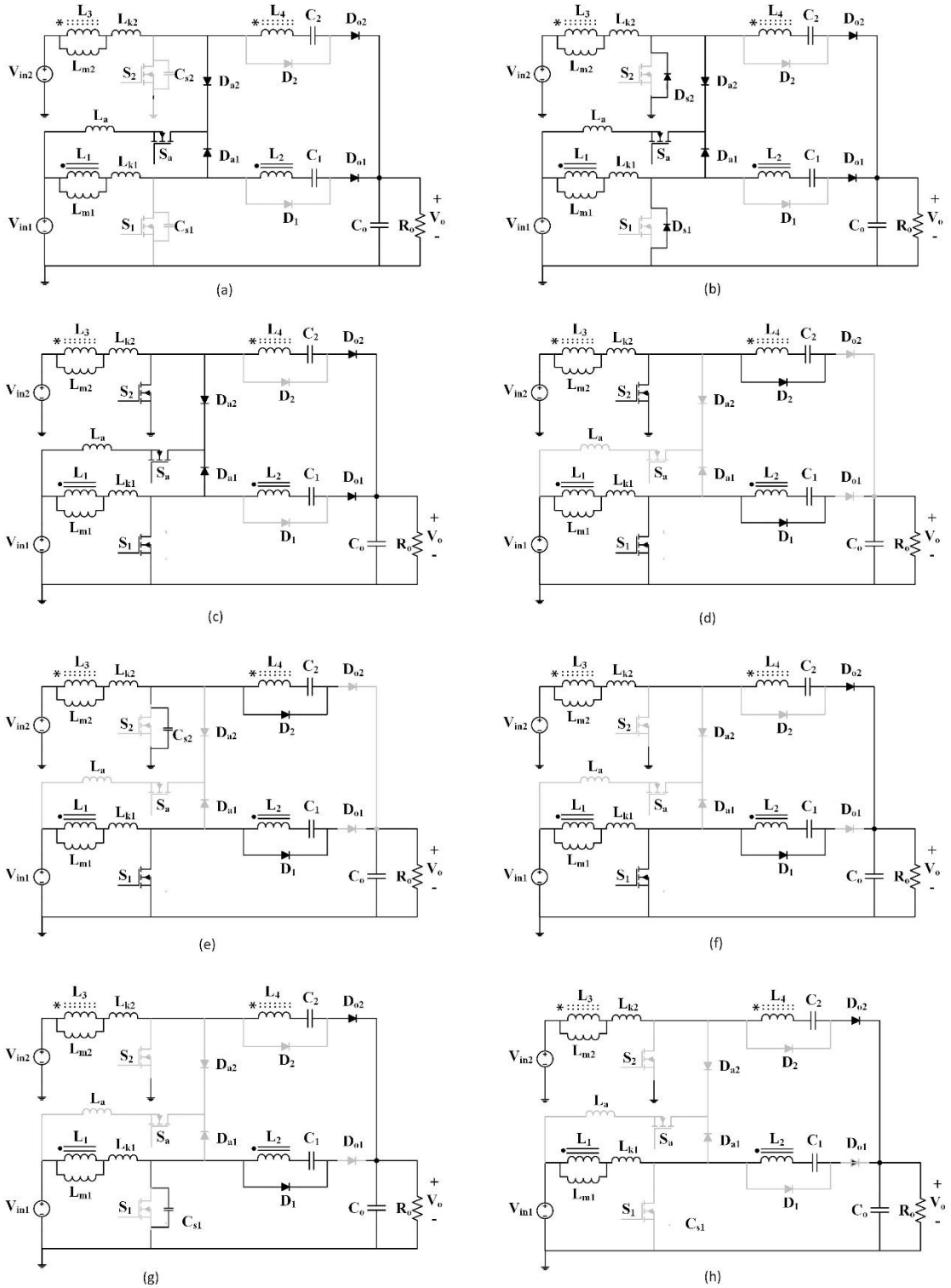


Fig. 3. Equivalent circuit of the proposed converter at the a) first, b) second, c) third, d) fourth, e) fifth, f) sixth, g) seventh, and h) eighth modes

C. Voltage Stress of Semiconductor Elements

By writing KVL in the ring in which switches and diodes are located (in the off mode), the element's voltage stress can be obtained. Fig. 5 illustrates the normalized stress diagram of the components for different values of turn ratio.

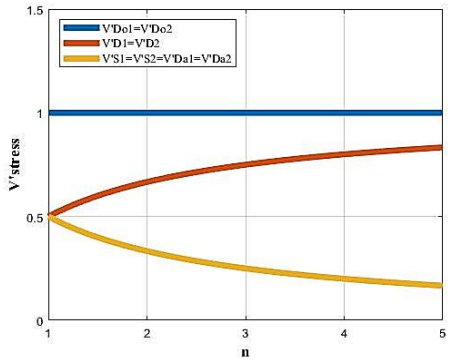


Fig. 5. Diagram of normalized stress across the components for varying turn ratio values.

$$V_{S1} = V_{S2} = \frac{V_o}{n+1} \quad (6)$$

$$V_{D1} = V_{D2} = nV_{L1} - V_{C1} = \frac{nV_o}{n+1} \quad (7)$$

$$V_{Do1} = V_{D02} = V_o \quad (8)$$

TABLE 1. SPECIFICATIONS OF THE PROPOSED CONVERTER AND THE VALUES OF ITS COMPONENTS

Elements/specifications	Value/part name
Switches	IRF740
All diodes	MUR860
C_{s1},C_{s2}	1nF
C_1,C_2	1µF
C_o	47µF
n	2
P_o	170W
First input voltage	30V
Second input voltage	60V
Output voltage (V_o)	410V
Switching frequency	100kHz

D. The Design of Auxiliary Elements

We use the snubber equation to design the auxiliary inductor L_a.

$$L_a > \frac{V_{sw}.t_r}{I_{sw}} > 2.2\mu H \quad (9)$$

in which t_r is the switch current ascending time, voltage V_{sw} is the final voltage across the switch before turning on, and I_{sw} is the final current of the switch before turning off. In addition, snubber capacitors can be obtained from Equation 10.

$$C_s > \frac{T_{res}^2}{2\pi L_a} > 11.5nF \quad (10)$$

E. The design of the Main Elements

The following equations are derived to calculate the values of the main circuit components based on the nominal output power, switching frequency, and voltage ripple across capacitors C_1, C_2, and the output capacitor, as well as the current ripple in the magnetizing inductance. It should be noted that all passive components have been designed with larger values to ensure compliance with the required conditions.

$$C_o > \frac{D_{max}V_O}{\Delta V_o f R_o} > 41\mu F \quad (11)$$

$$C_1, C_2 > \frac{I_o D}{4f\Delta V_C} > 0.64\mu F \quad (12)$$

$$L_m > \frac{D(1-D)^2 R_o}{4(1+n)^2 f} > 160\mu H \quad (13)$$

IV. Simulation Results of the Proposed Dual-input High Step-up Converter

Based on the design steps outlined in the previous section, the converter is simulated for an output power of 170 W and an output voltage of 410 V. Table 1 lists the values and specifications of all components. To verify the accuracy of the conducted analyses, the proposed converter was simulated using PSPICE software.

The layout of the simulated converter is depicted in Fig. 6, with simulation results illustrated in Figs. 7 to 12. Fig. 7 shows the gate-source pulse waveforms for both the main and auxiliary switches. Figs. 8 and 9 present the simulated current and voltage waveforms for the main switches S1 and S2. These figures indicate that when the switches are turned on, the switch current is negative, causing the body diode to conduct and enabling ZVS conditions. Additionally, the voltage across the switches gradually increases at turn-off moments, establishing Zero Voltage (ZV) conditions for the main switches during turn-off.

Fig. 10 demonstrates the auxiliary switch current waveform. According to the current slope, the auxiliary switch is on and is turned off under zero current switching (ZCS) conditions. Figs. 11 and 12 show diodes D_1-D_{o1} and D_2-D_{o2} current waveforms of the proposed converter, respectively. In all the figures, it is evident that the diode current exhibits a sloped increase and decrease, indicating that the diodes turn on and off under ZCS conditions.

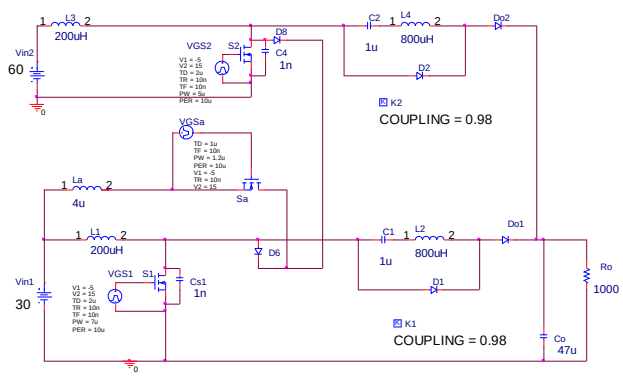


Fig.6 A schematic view of the proposed dual-input high step-up converter simulated in PSPICE software

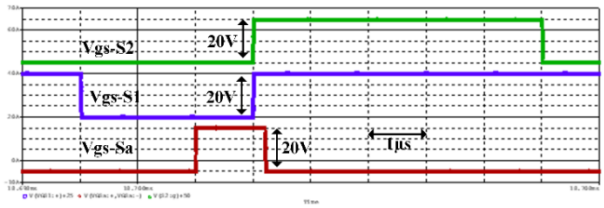


Fig.7. The gate-source pulse waveform of switches S_1 (blue), S_2 (green), and Sa (red) of the simulated converter

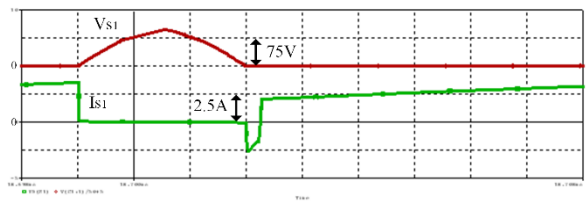


Fig.8. The simulated converter switch S_1 voltage (top) and current (bottom) waveform

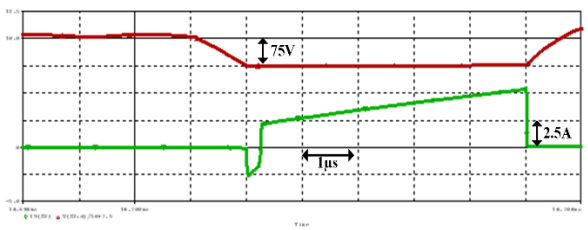


Fig.9 The simulated converter switch S_2 voltage (top) and current (bottom) waveform

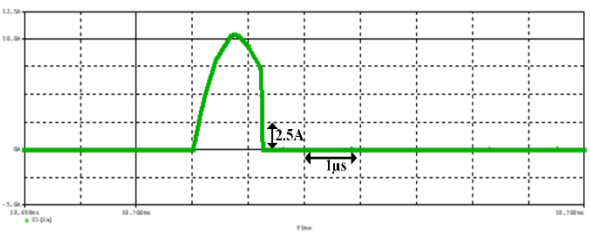


Fig.10. The simulated converter switch S_a current waveform

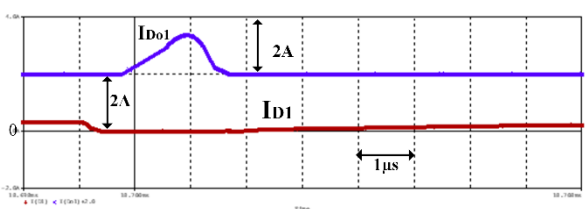


Fig.11. The simulated converter diode D_1 current (bottom) waveform and diode D_{o1} current (top) waveform

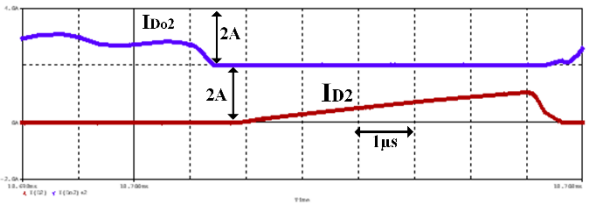


Fig.12. The simulated converter diode D_2 current (bottom) waveform and diode D_{o2} current (top) waveform

V. Practical Results

To verify the accuracy of the theoretical analysis, a 170-W experimental prototype of the proposed converter was implemented and tested according to Table 1. Fig. 13 displays the laboratory setup of the proposed converter. In the experimental setup, a MEGATEK M0-3003 power supply was employed to provide a stable DC voltage. To capture and analyze the waveforms accurately, a GW Instek GDS-2104 oscilloscope was used, allowing precise observation of voltage and current waveforms across various components of the converter. Also, to control and drive the switches, an FPGA Spartan 6 is utilized, along with an HCPL3120 as the driver.

Fig. 14 depicts the practical waveforms for the voltage and current of the switches and diodes in the proposed converter. According to this figure, all switches and diodes of the proposed converter operate under soft-switching conditions. In Figs. 14a and 14b, the switch current is negative when the switches are turned on, causing the body diode to conduct and create ZVS conditions for the switches. At turn-off, the voltage increases gradually, achieving ZV conditions for the main switches. The maximum voltage across the main switches is 160 V, significantly lower than the 410 V output, which helps reduce conduction losses. In Fig. 14c, the steep rise in current through switch S_a establishes ZCS conditions for the auxiliary switch during both turn-on and turn-off. Fig. 14d shows soft switching for diodes D_1 and D_{O1}, where their current rises and falls gradually, ensuring ZCS conditions and eliminating reverse recovery issues.

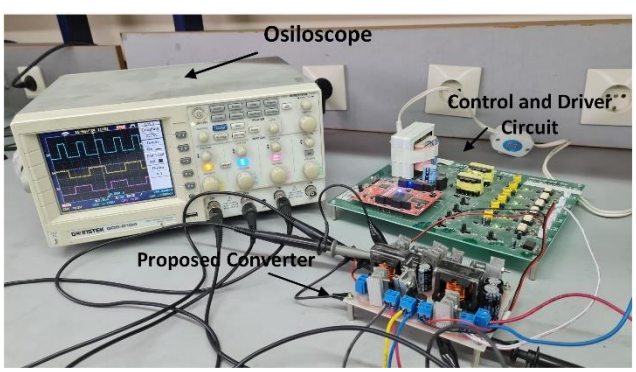


Fig. 13. The experimental setup of the proposed converter

VI. Analysis of the Proposed Converter Efficiency

Fig. 8 compares the efficiency between the proposed dual-input, high step-up converter, and its dual-input. The inclusion of a coupled inductor necessitates the use of a clamp circuit for the switches in the hard-switching version, leading to increased circuit losses due to resistance, thereby reducing efficiency. However, as illustrated in Fig. 8, the efficiency of the converter under soft-switching conditions is markedly improved over that of the hard-switching setup. This improvement is attributed to the auxiliary circuit's brief connection time within the proposed converter, which limits the circulating current and minimizes its impact on losses. Nonetheless, at low output power, the auxiliary circuit may slightly reduce the converter's efficiency. According to Fig. 8, the efficiency of the proposed converter at a rated power of 170 W reaches 95%, achieving a 5% increase over the hard-switching counterpart.

VII. Comparison of the Proposed Converter with Previous Converters

Table 2 provides a comparative analysis of the proposed converter against previously developed similar converters, focusing on criteria such as component count, voltage gain, and voltage stress on the switches. Table 2 reveals that the component count for both the proposed converter and converters [13], [14] is the same and lower than that of [11], [12]. However, converters [14] and [15] operate under hard switching conditions and exhibit significantly lower efficiency. The proposed converter achieves equivalent gain and stress

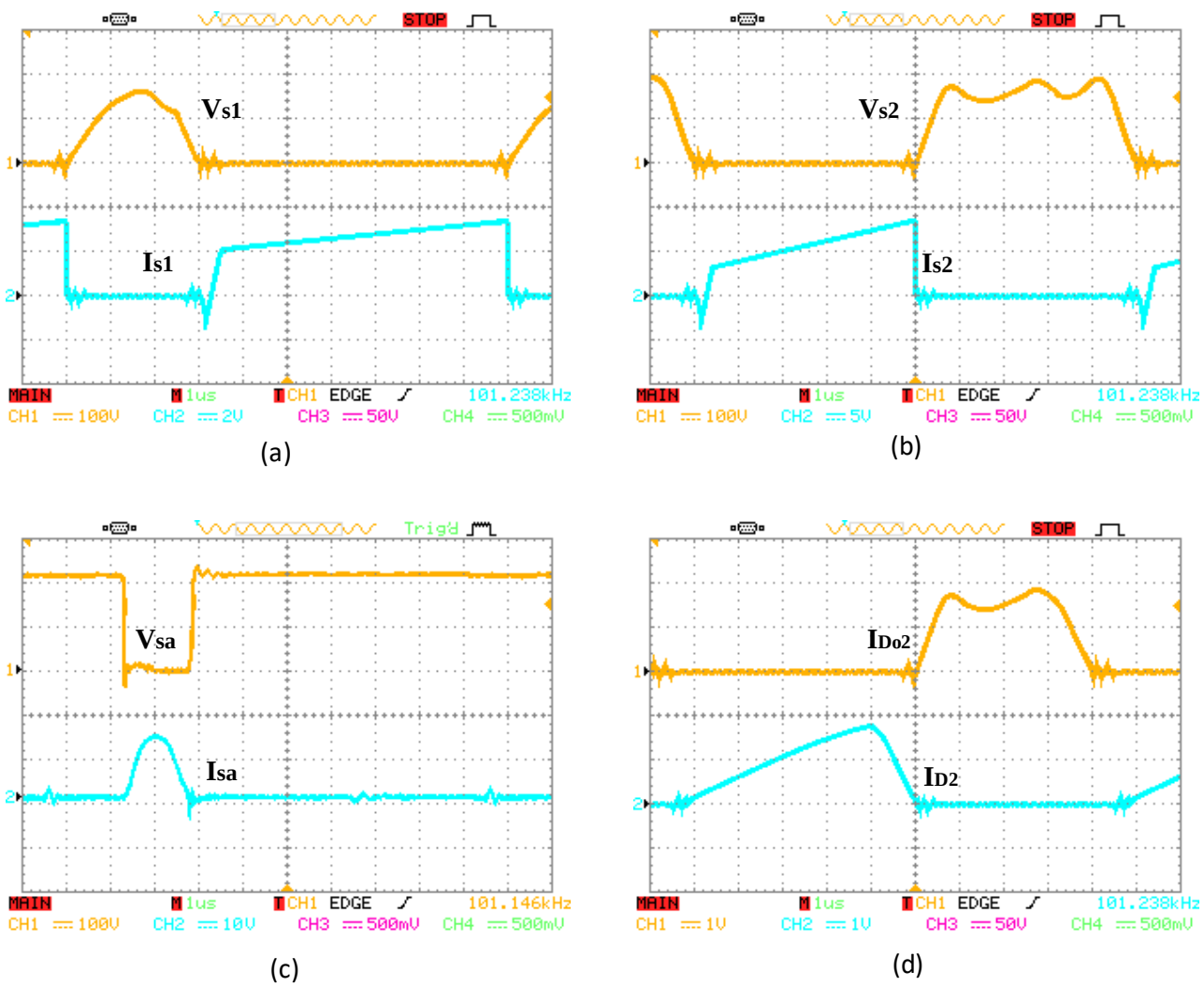


Fig.14. The practical results of (a) the measured voltage (up) and current (bottom) waveform of S_1 (100V/div, 2A/div, 1µs/div) (b) the measured voltage (up) and current (bottom) waveform of S_2 (100V/div, 5A/div, 1µs/div), (c) the measured voltage (up) and current (bottom) waveform of S_a (100V/div, 10A/div, 1µs/div), (d) the measured current waveform of D_2 (bottom) and D_{o2} (up) (1A/div, 1µs/div).

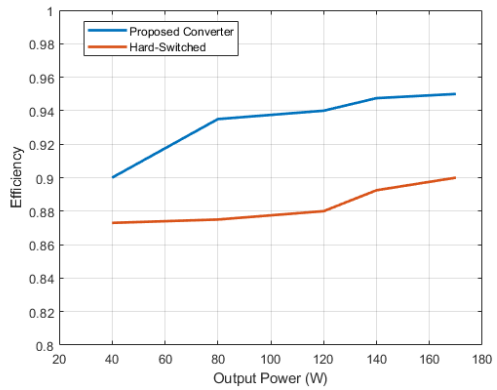


Fig. 15. The efficiency curve of the proposed converter in comparison to its hard-switching counterpart.

levels as observed in converters [12], [13], [15], and [20], yet it utilizes fewer components than [12]. Converters [19]-[21] achieve high voltage gain without using a coupled inductor and require fewer components than the proposed converter. However, converter [19] operates with hard switching and has a floating source on the switch, necessitating driver circuit isolation. Converter [20], while efficient, suffers from switching losses and high voltage stress on the switches, leading to increased costs. Converter [21] has a low component count and continuous input current but also experiences high voltage stress and requires an isolated driver.

VIII. Conclusions

This paper introduced a new dual-input converter with a modular auxiliary circuit designed to reduce conduction and switching losses. The modularity of the auxiliary circuit enables it to remain unchanged while universally adapting to an increasing number of converter inputs. Additionally, the proposed converter achieves soft switching across all semiconductor devices, delivers high voltage gain, and reduces voltage stress on the switches. All diodes turn off under zero current (ZC) conditions, effectively eliminating reverse recovery issues, while the main switch operates under ZV conditions, thereby avoiding capacitive turn-on losses and switching losses. Since the number of auxiliary circuit elements is low and the auxiliary switch is on for a short duration, the auxiliary circuit does not impose significant losses on the converter. Furthermore, the proposed converter efficiently recovers the energy stored in the snubber capacitors by redirecting it to the input, thereby enhancing overall efficiency. As a result, the converter's efficiency improves by 5% at full load compared to its hard-switched counterpart.

TABLE 2. A COMPARISON OF THE PROPOSED DUAL-INPUT CONVERTER PARAMETERS WITH SIMILAR PREVIOUS CONVERTERS

Reference / Parameter	[11]	[12]	[13]	[14]	[15]	[19]	[20]	[21]	Proposed converter
Number of elements	18	17	14	14	12	12	11	10	14
Switching Condition	ZV	ZV	ZC	Hard	Hard	Hard	Hard	Hard	ZV
Voltage Gain	4/(1-D)	(n+1)/(1-D)	(n+1)/(1-D)	(n+1+D)/(1-D)	(n+1)/(1-D)	$(3-D)/(1-D)^2$	(n+1)/(1-D)	(1-D)/(1-2D)	(n+1)/(1-D)
Voltage Stress on Switch	Vo/4	Vo/(n+1)	Vo/(n+1)	Vo/(n+1+D)	Vo/(n+1)	Vo(3-2D)/(6-2D)	Vo	Vo/(1-D)	Vo/(n+1)
Common Ground	No	No	Yes	Yes	Yes	Yes	Yes	No	Yes

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