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A Minimum Phase DC-DC Converter with High Voltage Gain and Continuous Input Current

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ABSTRACT

This paper presents a new design of a minimum phase high step-up DC-DC converter with a fast dynamic response for renewable energy systems. In addition to the common ground sharing between the input and output ports, the proposed converter draws a low ripple current from the input source, prolonging the input source's life cycle. Moreover, eliminating the right half plane zero from the control to output transfer function enables the converter to provide fast dynamic responses. Moreover, low voltage stress across the circuit components, simple structure, and low EMI are other merits of the suggested topology. Theoretical analysis, including the principle of operation, the mathematical calculation for steady-state operation, and small-signal modeling derivation, are clarified in detail. At last, to verify these analyses and the mentioned features of the proposed converter, a 25V input voltage, 100V output voltage and 100 W output power with 50 kHz switching frequency laboratory prototype has been implemented, and the main experimental results have also been outlined.

NOMENCLATURE

T	TIME DURATION OF A SWITCHING CYCLE
f_s	SWITCHING FREQUENCY
D	DUTY CYCLE OF THE POWER SWITCH
r_{Lk}	TOTAL PARASITIC RESISTANCE OF COUPLED INDUCTORS
$r_{Do(i)}, V_{FDo(i)}$	THE ITH DIODE PARASITIC RESISTANCE AND VOLTAGE DROP
t_{on}, t_{off}	THE SWITCH TURN-ON AND TURN-OFF TIMES
r_L	PARASITIC RESISTANCE OF THE INPUT INDUCTOR L
$r_{C(i)}$	THE ITH CAPACITOR PARASITIC RESISTANCE

I. Introduction

Global warming has been seen as an accelerating issue over the past decades that only gets worse. Needless to say, burning fossil fuels and the released greenhouse gases are the primary causes of this trend [1]. As a result of this worrying trend, researchers have paid ever-increasing attention to promising renewable energy sources such as wind and solar power and their penetration into the power grid [2-4]. Although solar power is the most convenient renewable power source across the planet, photovoltaic (PV) panels cannot be directly connected to the utility grid since their output voltage is much

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lower than the utility grid's demanded voltage. Hence, PV panels need an interface to inject their power into the power grid [5-7]. Conventional Boost Converter (CBC) is the most prevalent choice for step-up applications due to its simple structure and easy control. However, CBC suffers from multiple drawbacks, such as high voltage stress on its semiconductors, limited voltage gain, and low efficiency. To overcome these problems, extensive research has been done to report numerous DC-DC converters capable of realizing high efficiency and high voltage gain without extreme voltage stress across their semiconductors [8-12].

On the other hand, fast dynamic response is vital for many applications, namely portable electronic devices, DC microgrids, energy storage systems, and especially transformation electrification [13, 14]. In view of the fact that CBC's control to output transfer function has a Right-Half Plane Zero (RHPZ), it is a non-minimum phase system. Subsequently, many efforts have been put into improving the dynamic response of step-up DC-DC converters.

A damping network has been employed in several structures to eliminate RHPZ. These converters add a series Resistance-Capacitance (RC) to their structure to move the RHPZ to the left-hand side, hence improving the dynamic response of the converter. A damping network was added to the diode-capacitor-based boost and buck-boost converters to avoid the RHPZ in their structures [15]. Apart from the lack of common ground sharing between the input and output ports and the discontinuous input current of the buck-boost converter, both suffer from low voltage gain and low efficiency. In [16], a bidirectional switched capacitor DC-DC converter was reported, which uses a damping network to exclude right-half plane zero from its control to output transfer function. Also, a dual output AC/DC hybrid converter with a damping network was introduced in [17] to obtain minimum phase characteristic. All the same, the voltage gain is equal to the conventional buck-boost converter. On the other hand, using the RC networks leads to power losses in these converters, and the lack of high efficiency is a significant setback.

Complex control approaches have been used to realize minimum phase behavior for DC-DC converters. Time-based control technique was applied to CBC in [18] to remove the RHPZ and modify the dynamic response of the converter. The sampling position approach in a dual-loop digital average current mode controller was implemented to cancel the RHPZ in CBC [19]. Another method named Passivity-Based Control (PBC) was proposed and applied to CBC in [20] for better dynamic response. Yet, the non-minimum phase characteristic of CBC and Z-source converter was tackled with Active Disturbance Rejection Control (ADRC) and cascaded sliding mode controller in [21] and [22], respectively. Despite improving the dynamic response using advanced controllers, the power circuit of CBC and Z-source converter still faces several challenges, including limited voltage gain, high voltage stress across semiconductors, inefficient energy conversion, etc. The performance of the general predictive and linear controllers in overcoming the non-minimum phase feature of a multi-input boost converter [23]. This investigation confirms that General Predictive Control (GPC) accomplishes faster dynamic response and more robustness than linear controller.

Researchers have addressed removing the RHPZ by changing CBC's structure and turning it into Tri-state converters [24, 25]. These converters add a power switch and a diode to CBC to cancel the right-half plane zero from their control to the output transfer function. However, these structural modifications cause the ripple in the input current to rise. Hence, [26] offered an interleaved-based tri-state boost converter to tackle this issue. Nevertheless, with these enhancements, the voltage gain of these converters is still constrained, rendering them improper for high voltage gain demands. Similar to tri-state converters, a third-order boost converter was also introduced to increase voltage gain conversion [27]. But, the input and output ports do not share a common ground. Besides, due to the high ripple input current, the converter falls short of the imperative specifications for practical applications. Employing coupled inductors is another approach to cancel out the RHPZ in DC-DC converters. This technique was implemented in [28] for eliminating the RHPZ since it can establish a path from the input source to the output load when the main switch is in its ON state. Despite possessing a fast dynamic response, the converter has a voltage gain equal to CBC and employs a damping network, resulting in efficiency degradation. Three inductors were coupled in [29] and [30] to limit the input current ripple while transferring the RHPZ to the left-hand side. Like the converter in [28], the restricted voltage gain deteriorates the overall performance of the converters. Furthermore, the low coupling coefficient is another drawback that leads to energy loss of magnetic elements and construction complexity. To attain the requirements for high step-up voltage gain, coupled inductors have also been utilized to acquire simultaneous minimum phase feature and high voltage conversion ratios in several DC-DC converters [31-34]. By making a forward path from the input source to the output load during the ON time of the power switch, the boost-forward converter in [31] can offer minimum phase characteristic and higher voltage gain compared to all the previously mentioned converters. However, the input current ripple is large, reducing the input source's life span. The voltage gain was improved by utilizing switched capacitors and coupled inductors in the reported converters in [32, 33]. Despite improving voltage gain, the high input current ripple drawback still persists. To resolve the high input current ripple problem, an interleaved-based converter was proposed in [33]. Whilst the converter offered a lower input current ripple compared to [31], the ripple is still high due to

using an asymmetrical structure of the coupled inductors [35, 36].

Juxtaposing all the pros and cons of the above-mentioned minimum phase converters, none can provide high voltage gain while drawing a low ripple current from the input source. Hence, the primary novelty of this paper is the proposal for a minimum phase DC-DC converter by combining boost forward [31] and conventional boost converter. In addition to the fast dynamic response, high voltage gain, low ripple input current, and common ground sharing between input and output ports are other merits of the presented converter. Thanks to these characteristics, the new converter is compatible with many applications.

The remainder of this paper is organized as follows: Section II describes the operation principles of the proposed converter. Voltage and current stresses have been derived in Section III. Section IV represents the small-signal modeling process. Performance comparison is introduced in Section V. Experimental results are discussed in Section VI. Lastly, Section VII concludes the paper.

II. Principles of Operation

The proposed converter is comprised of one power switch S, one inductor L, two diodes D_{o1}, and D_{o2}, three capacitors C_1, C_{o1} , and C_{o2} and two coupled inductors N_1 and N_2. The proposed converter equivalent circuit is shown in Fig. 1. The voltage and current associated with each element are shown separately.

With the object of simplifying calculation for steady-state analysis, the below assumptions are taken into account;

1) The capacitors' voltage is considered constant during one switching cycle.
2) All the circuit elements are ideal. Hence, the power switch's turn-on resistance, diodes' voltage drop during on state, and parasitic resistances of the capacitors and inductors are ignored.
3) A transformer with a leakage inductance L_k and a large magnetizing inductance L_M is used to model the coupled inductors.

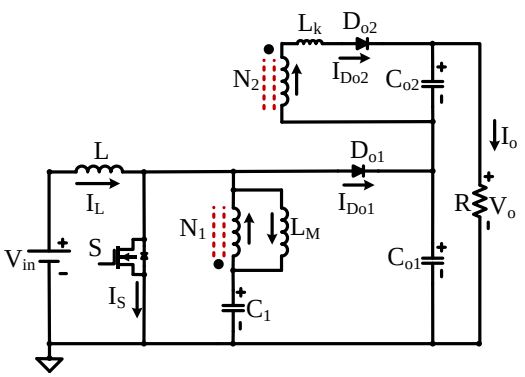


Fig. 1. The proposed converter.

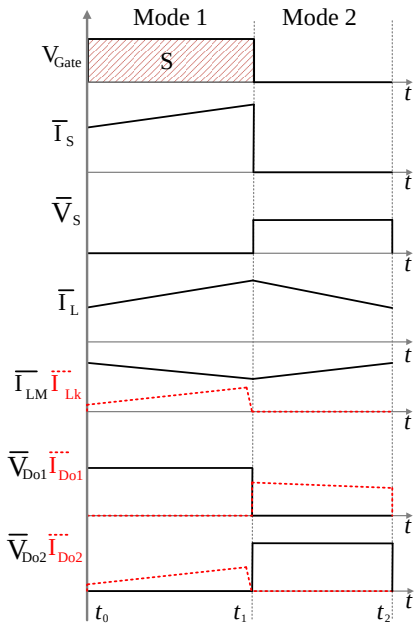


Fig. 2. Key waveforms of the proposed converter in a switching cycle.

4) The proposed converter operates in Continuous Conduction Mode (CCM).

Fundamental waveforms of the proposed converter are drawn in Fig. 2. The proposed converter has two operational stages. They are described in detail below.

Mode 1 $[t_0 - t_1]$: At $t = t_0$ switch S is turned ON by the driving circuit, and the diode D_{o1} is turned OFF. The input voltage source V_{in} gives energy to the inductor L. At the same time, the capacitor C_1 together with magnetizing inductance L_M charge capacitor C_{o2} and the output load through the coupled inductors and diode D_{o2}. Moreover, the output capacitors C_{o1} and C_{o2} supply the load at this time interval. The following equations are derived for this operational stage.

$$V_L = V_{in} \quad (1)$$

$$V_{Lk} = -V_{Co2} + nV_{C1} \quad (2)$$

$$V_{LM} = V_{C1} \quad (3)$$

$$V_o = V_{Co1} + V_{Co2} \quad (4)$$

$$I_{Lk} = I_{Co2} + I_o \quad (5)$$

Mode 2 $[t_1 - t_2]$: At $t = t_1$ switch S is turned OFF by the driving circuit, and the diode D_{o2} is turned OFF. Besides, diode D_{o1} is turned ON. Accordingly, the stored energy in the inductor L is released to magnetizing inductance L_M, capacitor C_1 and capacitor C_{o1}. Like the previous mode, output capacitors C_{o1} and C_{o2} supply the load. The following equations are derived in this operational stage.

$$V_L = V_{in} - V_{Co1} \quad (6)$$

$$V_o = V_{Co1} + V_{Co2} \quad (7)$$

$$V_{LM} = V_{C1} - V_{Co1} \quad (8)$$

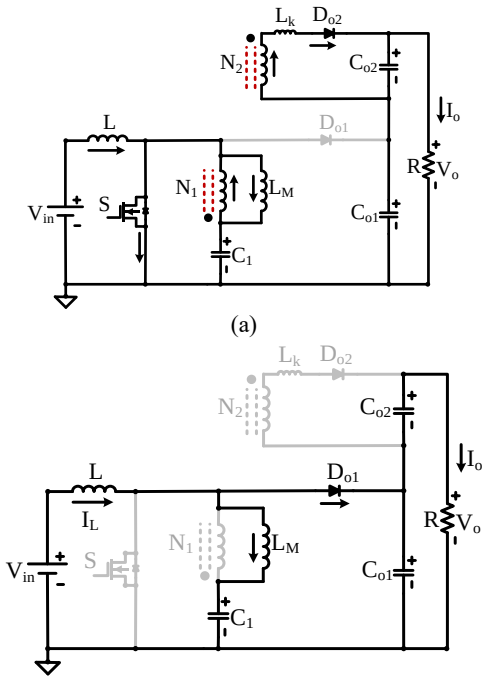


Fig. 3. Equivalent circuit of the proposed converter in a switching cycle (a) Mode 1 and (b) Mode 2.

$$I_{Do1} = I_o + I_{Co1} \tag{9}$$

The equivalent circuits for both operational stages are depicted in Fig. 3.

III. Steady-State Analysis of the Proposed Converter

A. Voltage stress across circuit elements

This section calculates all the elements' voltage stresses. Then, the voltage gain of the converter is derived. Since the input voltage source, input inductor L, magnetizing inductor L_M, and capacitor C_1 make a loop, the average voltage across the capacitor C_1 is equal to the input voltage;

$$V_{C1(avg)} = V_{in} \tag{10}$$

Hence, the voltage across the capacitor C_{o2} is derived as

$$V_{Co2} = nV_{in} \tag{11}$$

in which $n = \frac{N_2}{N_1}$ is the turns ratio of the coupled inductors. Moreover, by applying the volt-second balance law to the input inductor L, the below equations can be written.

$$\int_0^{DT} V_{in}dt + \int_{DT}^{T}(V_{in} - V_{Co1})dt = 0 \tag{12}$$

$$V_{Co1} = \frac{V_{in}}{1-D} \tag{13}$$

Now, from (11) and (13), the voltage gain of the proposed converter equals (14).

$$M = \frac{V_o}{V_{in}} = \frac{1}{1-D} + n \tag{14}$$

One can see that the voltage gain of the converter can be controlled by both the duty cycle of the power switch and the turn ratio of the coupled inductors.

B. Semiconductor's voltage stresses

From operational principals, the power switch S and diode D_{o1} should tolerate a voltage equal to V_{C1} during their OFF state. As a result, their voltage stresses are calculated as

$$V_{Do1} = V_S = \frac{V_{in}}{1-D} \tag{15}$$

And the voltage stress of the diode D_{o2} can be written as (16).

$$V_{Do2} = V_{Co2} - V_{N2} = \frac{nV_{in}}{1-D} \tag{16}$$

C. Current stress analysis of circuit elements

Notably, the proposed converter's power losses and the inductors' current ripple are ignored to facilitate current stress analysis. Now, the average current of the input inductor L can be expressed as

$$I_{L1(avg)} = MI_o = \left(\frac{1}{1-D} + n\right)I_o \tag{17}$$

Additionally, by applying the charge-balance law to the capacitor C_{o1}, the following equations are obtained.

$$\int_0^{DT} -I_o\,dt + \int_{DT}^{T}(I_L - I_{LM} - I_o)dt = 0 \tag{18}$$

$$I_{LM(avg)} = nI_o \tag{19}$$

Given the above equations and doing some mathematical calculations, the average, maximum, and Root Mean Square (RMS) currents of the power switch and diodes are acquired as

$$I_{S(avg)} = DI_o\left(\frac{1}{1-D} + \frac{n}{D}\right) \tag{20}$$

$$I_{Do1(avg)} = I_{Do2(avg)} = I_o \tag{21}$$

$$I_{S(max)} = I_o\left(\frac{1}{1-D} + \frac{2n}{D}\right) \tag{22}$$

$$I_{Do1(max)} = \frac{2I_o}{1-D} \tag{23}$$

$$I_{Do2(max)} = \frac{2I_o}{D} \tag{24}$$

$$I_{S(RMS)} = I_o\sqrt{\frac{D}{(1-D)^2} + \frac{2n}{1-D} + \frac{4n^2}{3D}} \tag{25}$$

$$I_{Do1(RMS)} = I_o\sqrt{\frac{7}{3(1-D)}} \tag{26}$$

$$I_{Do2(RMS)} = \frac{2I_o}{\sqrt{3D}} \tag{27}$$

Finally, the RMS currents of the leakage inductance and the capacitors are given by

$$I_{Lk} = I_{C1(RMS)} = nI_o\sqrt{\frac{4-3D}{3D}} \tag{28}$$

$$I_{Co1(RMS)} = I_o\sqrt{\frac{D}{1-D}} \quad (29)$$

$$I_{Co2(RMS)} = I_o\sqrt{\frac{4-3D}{3D}} \quad (30)$$

The voltage gain of the proposed converter as a function of the duty cycle at multiple turns ratio is illustrated in Fig. 4.

Likewise, the power switch's normalized RMS current by considering various turn ratios is shown in Fig. 4. As evidenced, the voltage gain has a straightforward relation with both the duty cycle and turns ratio of the coupled inductors. On the contrary, the normalized RMS current of the power switch decreases as the duty cycle increases. Meanwhile, the coupled inductors' turn ratio limits the falling rate.

IV. Small Signal Modelling

This section explains the small-signal modeling process and its mathematical derivation. Since DC-DC converters contain nonlinear elements, such as switches and diodes, they are inherently nonlinear systems. Hence, the proposed converter's Nonlinear Time-Variant (NLTV) model is transformed into a linear time-invariant (LTI) model by employing the State Space Average (SSA) method.

Moreover, it is essential to note that the voltages across the capacitors and the currents through the inductors are considered state variables. In the interest of using the SSA method, differential equations associated with each mode, with the help of Kirchhoff's Voltage and Current Laws (KVL and KCL), are written as

Mode 1:

$$\frac{di_L}{dt} = \frac{-r_L i_L}{L} + \frac{V_{in}}{L} \quad (31)$$

$$\frac{di_{LM}}{dt} = \frac{v_{C1}}{L_M} \quad (32)$$

$$\frac{dv_{C1}}{dt} = \frac{-i_{LM}}{C_1} - \frac{n^2 DT_s}{L_k C_1} v_{C1} + \frac{nDT_s}{L_k C_1} v_{Co2} \quad (33)$$

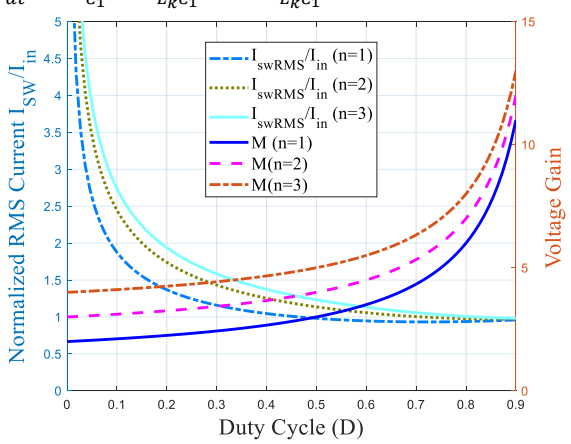


Fig. 4. Voltage gain and switch's normalized RMS currents for various coupled inductors turn ratio.

$$\frac{dv_{Co1}}{dt} = -\frac{(v_{Co1}+v_{Co2})}{RC_{o1}} \quad (34)$$

$$\frac{dv_{Co2}}{dt} = \frac{nDT_s}{L_k C_{o2}} v_{C1} - \frac{v_{Co1}}{RC_{o2}} - \left(\frac{1}{RC_{o2}} + \frac{DT_s}{L_k C_{o2}}\right) v_{Co2} \quad (35)$$

Mode2:

$$\frac{di_L}{dt} = \frac{-r_L i_L}{L} - \frac{v_{Co1}}{L} + \frac{V_{in}}{L} \quad (36)$$

$$\frac{di_{LM}}{dt} = \frac{v_{C1}}{L_M} - \frac{v_{Co1}}{L_M} \quad (37)$$

$$\frac{dv_{C1}}{dt} = -\frac{i_{LM}}{C_1} \quad (38)$$

$$\frac{dv_{Co1}}{dt} = \frac{i_L}{C_{o1}} + \frac{i_{LM}}{C_{o1}} - \frac{(v_{Co1}+v_{Co2})}{RC_{o1}} \quad (39)$$

$$\frac{dv_{Co2}}{dt} = -\frac{(v_{Co1}+v_{Co2})}{RC_{o2}} \quad (40)$$

The closed-form of the state equations can now be written by applying the time weight coefficients of every operational stage to equations (31)-(40) as follows.

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Eu \end{cases} \quad (41)$$

in which $x, y,$ and u are the state variables, the output voltage, and the input matrix, respectively. Additionally, the final form of A, B, C, and E are expressed as

$$A = \begin{bmatrix} \frac{-r_L}{L} & 0 & 0 & \frac{D-1}{L} & 0 \\ 0 & 0 & \frac{1}{L_M} & \frac{D-1}{L_M} & 0 \\ 0 & \frac{-1}{C_1} & \frac{-T_s D^2 n^2}{C_1 L_k} & 0 & \frac{T_s D^2 n}{C_1 L_k} \\ \frac{1-D}{C_{o1}} & \frac{1-D}{C_{o1}} & 0 & \frac{-1}{RC_{o1}} & \frac{-1}{RC_{o1}} \\ 0 & 0 & \frac{T_s D^2 n}{C_{o2} L_k} & \frac{-1}{RC_{o2}} & -\frac{(RT_s D^2 + L_k)}{RC_{o2} L_k} \end{bmatrix} \quad (42)$$

$$B^T = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 \end{bmatrix} \quad (43)$$

$$C = [0 \quad 0 \quad 0 \quad 1 \quad 1] \quad (44)$$

$$E = 0 \quad (45)$$

with the help of the following equations, the steady state value of all the variables can be determined as follows.

$$I_L = (n + \frac{1}{1-D})I_o \quad (46)$$

$$V_{Co1} = \frac{V_{in} - r_L I_L}{1-D} \quad (47)$$

$$V_{C1} = (1-D)V_{Co1} \quad (48)$$

$$V_{Co2} = \frac{L_k V_{Co1} - RT_s D^2 n V_{C1}}{RT_s D^2 + L_k} \quad (49)$$

$$I_{LM} = \frac{T_s D^2 n (V_{Co2} - nV_{C1})}{L_k} \quad (50)$$

Moreover, a comparison has been made to validate the modeling accuracy between the circuit's and model's responses. The result is depicted in Fig. 5. As shown, there is a step change in the input voltage value, from 50V to 60V at $t = 0.05s$, in which both responses have a wise agreement. Accordingly, the converter's model is valid for further analysis.

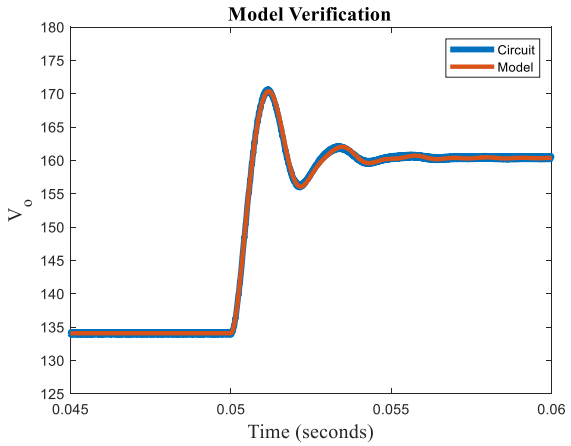


Fig. 5. Circuit's response and model's response comparison.

A small signal model is required to extract the conditions that make the proposed converter behave like a minimum-phase system. As a result, small ac perturbations (negligible compared to steady-state values) are added to the DC values of the state variables, the input voltage, and the duty cycle. These added ac perturbations with the "^" sign and the DC values in capital form are summarized in (51).

$$\begin{cases} x = X + \hat{x} \\ d = D + \hat{d} \\ v_{in} = V_{in} + \hat{v}_{in} \end{cases} \quad with \quad \begin{cases} |\hat{x}| \text{"} |X| \\ |\hat{d}| \text{"} |D| \\ |\hat{v}_{in}| \text{"} |V_{in}| \end{cases} \tag{51}$$

After applying (51) to (31)-(40), doing some calculations, and linearizing the model at the operation point via using (46)-(50), the small signal model of the proposed converter is determined as follows;

$$\begin{cases} \dot{\hat{x}} = A_s\hat{x} + B_s\hat{u} \\ \hat{y} = C_s\hat{x} + E_s\hat{u} \end{cases} \tag{52}$$

Where As is:

$$\begin{bmatrix} \frac{-r_L}{L} & 0 & 0 & \frac{D-1}{L} & 0 \\ 0 & 0 & \frac{1}{L_M} & \frac{D-1}{L_M} & 0 \\ 0 & \frac{-1}{C_1} & \frac{-T_sD^2n^2}{C_1L_k} & 0 & \frac{T_sD^2n}{C_1L_k} \\ \frac{1-D}{C_{o1}} & \frac{1-D}{C_{o1}} & 0 & \frac{-1}{RC_{o1}} & \frac{-1}{RC_{o1}} \\ 0 & 0 & \frac{T_sD^2n}{C_{o2}L_k} & \frac{-1}{RC_{o2}} & -\frac{(RT_sD^2+L_k)}{RC_{o2}L_k} \end{bmatrix} \tag{53}$$

$$B_s{}^T = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ \frac{V_{Co1}}{L} & \frac{V_{Co1}}{L_M} & \frac{2T_snD[V_{Co2}-nV_{C1}]}{C_1L_k} & -\frac{I_L+I_{LM}}{C_{o1}} \end{bmatrix} \tag{54}$$

$$C_s = [0 \quad 0 \quad 0 \quad 1 \quad 1] \tag{55}$$

$$E_s = 0 \tag{56}$$

$$\hat{u} = \begin{bmatrix} \widehat{v_{in}} \\ \hat{d} \end{bmatrix} \tag{57}$$

$$\hat{x}^T = [\widehat{i_L} \quad \widehat{i_{LM}} \quad \widehat{v_{C1}} \quad \widehat{v_{Co1}} \quad \widehat{v_{Co2}}] \tag{58}$$

Hence, by employing the Laplace transformation, the control-to-output transfer function G_{vod} is obtained as

$$G_{vod}(s) = \frac{\widehat{v_o}}{\hat{d}} = C_s(SI - A_s)^{-1}B_s + E_s \tag{59}$$

Using (59), the control to output transfer function G_{vod} can be rewritten as (60).

$$G_{vod} = \frac{\widehat{v_o}}{\hat{d}} = \frac{a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0}{b_5s^5 + b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \tag{60}$$

From (60), the control to output transfer function has four zeros and five poles. To force the converter to function like a minimum phase system, all the zeros should be placed on the left-hand side of the s-plane. As a result, the Routh-Hurwitz condition must be met by coefficients $a_1 - a_4$. The following conditions are produced when the coefficients $a_1 - a_4$ are subjected to this criterion.

$$a_4 > 0, a_3 > 0, a_0 > 0, a_2a_3 - a_4a_1 > 0, a_1\left[\frac{a_2a_3 - a_4a_1}{a_3}\right] - a_0a_3 > 0 \tag{61}$$

Fig. 6 (a) sketches the pole-zero map of G_{vod}, by employing the parameters in TABLE 1 at various output loads. Obviously, the system does not have any right-hand side zeros after considering the conditions summarized in (61). Hence, the converter benefits from the minimum phase characteristic. This figure also demonstrates that zeros with relatively higher frequency move considerably farther as the output load rises. Conversely, high-frequency poles move toward the imaginary axis as the output load increases.

Moreover, the area near the imaginary axis has been enlarged for better understanding in Fig. 6(b). As seen, with the output load increment, zeros and poles with relatively lower frequencies are shifted toward $j\omega$ axis. Finally, the Bode diagram of G_{vod} is illustrated in Fig. 7 for different output loads.

TABLE 1. OPERATING POINT'S SPECIFICATIONS OF THE PROPOSED CONVERTER

Parameters	Value
V_{in}	25V
L , r_L	300µH, 22mΩ
$L_M(turnsratio = n_1{:}n_2)$	460µH (1:2)
L_k	5µH
C_1, C_{o1}, C_{o2}	50µF, 68 µF, 50µF
R	50-150 Ω
f_s	50kHz

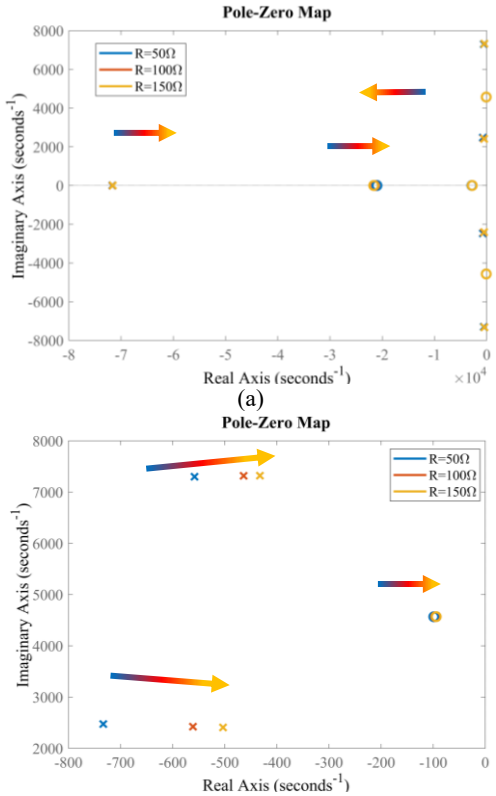


Fig. 6. Pole-Zero Map of G_{vod} at various output loads (a) Original Map, (b) Enlarged Map.

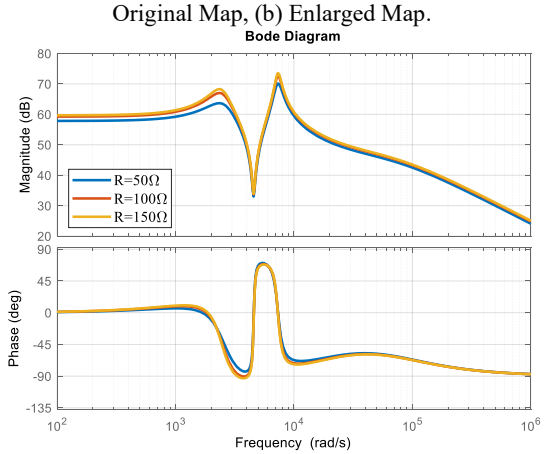


Fig. 7. Bode plot of G_{vod} at various output loads.

V. Comparison with Similar Converters

Since several studies about DC-DC converters with minimum and non-minimum phase features have been published, this section compares the proposed converter and its counterparts comprehensively.

Firstly, the normalized voltage stress of the power switch is compared for the proposed converter and DC-DC converters summarized in Fig. 8. Based on Fig.8 (a), the normalized power switch's voltage stress of [15]-boost, [32] and [33] are lower than the proposed converter. However, these converters suffer from high ripple input currents. Secondly, from Fig. 8 (b), the voltage gain of the proposed converter is higher than all the suggested converters except [12], [32] and [33]. It should be noted that the reported converter in [12] is a non-minimum phase converter and struggles with slow dynamic response. In the case of normalized input current ripple, Fig. 8 (c) confirms that only the converter in [26] can offer a lower input current ripple only for the duty cycle around 0.5.

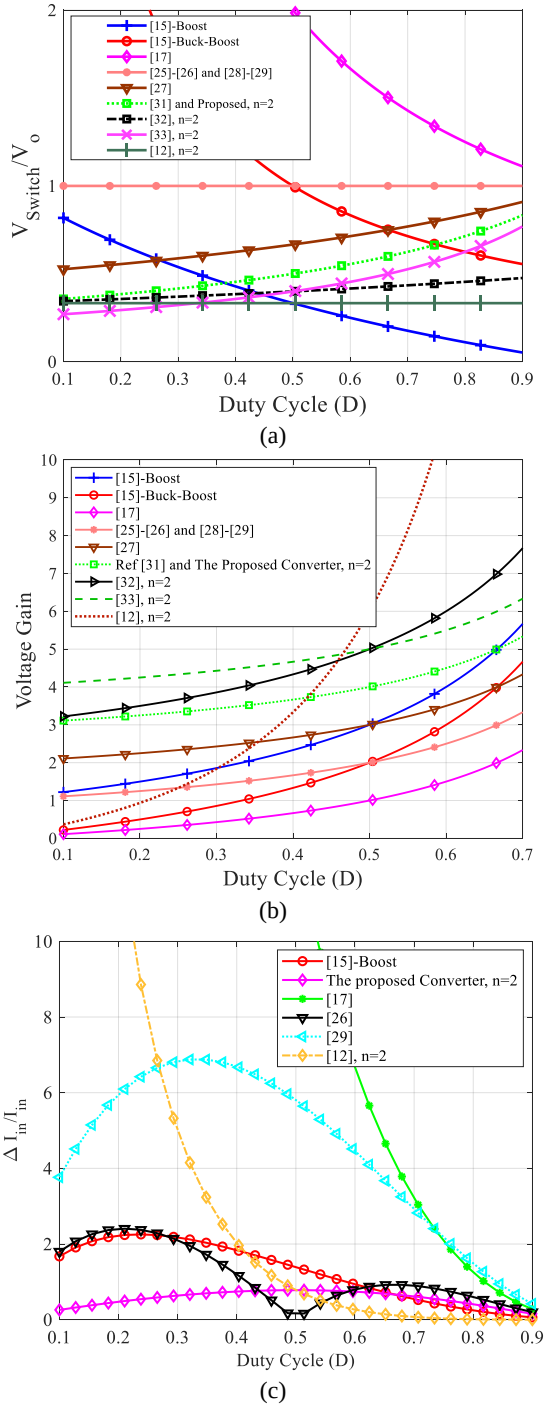


Fig. 8. Comparison with other minimum phase converters (a) Normalized voltage stress of the power switch, (b) Voltage gain comparison, and (c) Normalized input current ripple comparison.

TABLE 2 COMPARISON WITH OTHER SIMILAR CONVERTERS

Item / Converter	Voltage gain	Number of elements* MC	C	D	S	R_d	T	Voltage stress on switch(es)	Highest voltage stress on diodes	ICR**	C. G***
Ref [15] Boost	$\frac{1+D}{1-D}$	2	5	2	1	2	12	$\frac{(1-D)V_o}{1+D}$	$\frac{(1-D)V_o}{1+D}$	Low	×
Ref [15] Buck-Boost	$\frac{2D}{1-D}$	2	5	2	1	2	12	$\frac{V_o}{2D}$	$\frac{V_o}{2D}$	High	×
Ref [17] DC Part	$\frac{D}{1-D}$	2	3	1	4	-	10	$\frac{V_o}{D}$	$\frac{V_o}{D}$	Low	✓
Ref [25]	$\frac{1}{1-D}$	1	1	2	2	-	6	V_o	V_o	High	✓
Ref [26]	$\frac{1}{1-D}$	2	1	4	4	-	11	V_o	V_o	Low	✓
Ref [27]	$\frac{2-D}{1-D}$	1	2	2	1	-	6	$\frac{V_o}{2-D}$	$\frac{V_o}{2-D}$	High	×
Ref [28]	$\frac{1}{1-D}$	1	2	1	1	1	7	V_o	V_o	High	✓
Ref [29]	$\frac{1}{1-D}$	1	3	1	1	-	6	V_o	V_o	Low	✓
Ref [31]	$n+\frac{1}{1-D}$	1	2	2	1	-	6	$\frac{V_o}{n(1-D)+1}$	$\frac{nV_o}{n(1-D)+1}$	High	✓
Ref [32]	$1+\frac{n}{1-D}$	1	3	3	1	-	8	$\frac{V_o}{1-D+n}$	$\frac{nV_o}{2+n-D}$	High	✓
Ref [33]	$n+\frac{2-D}{1-D}$	2	3	3	1	-	9	$\frac{V_o}{n(1-D)+2-D}$	$\frac{nV_o}{n(1-D)+2-D}$	High	✓
Ref [12]	$\frac{(1+n)D}{(1-D)^2}$	2	3	3	2	-	10	$\frac{V_o}{n+1}$	$\frac{nV_o}{(1+n)D}$	Low	✓
Proposed converter	$n+\frac{1}{1-D}$	2	3	2	1	-	8	$\frac{V_o}{n(1-D)+1}$	$\frac{nV_o}{n(1-D)+1}$	Low	✓

* MC= Magnetic core, C= Capacitor, D=Diode, S= Switch, R_d=Damping Resistor and T= Total **ICR=Input Current Ripple, *** C.G= Common Ground

Otherwise, the proposed converter and the converter in [12] have the lowest input current ripple among all the converters.

Moreover, the input and output ports of the converters in [15] and [27] do not share a common ground, which limits their applications. From an efficiency point of view, the converters in [15] and [27] are not proper due to using damping resistances in their structure. Although the reported converters in [25], [27], [29], and [31] have the minimum number of elements, the lack of high voltage gain or continuous input current is their main drawback.

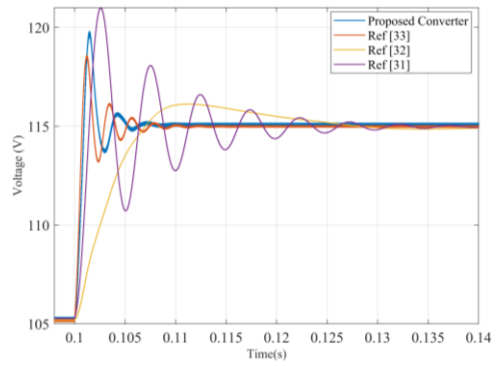
Juxtaposing all these comparisons, while converters with higher voltage gain exist, the proposed converter is the only one capable of simultaneously offering high voltage gain, low ripple input current, and common ground features. Additionally, the proposed converter provides these features without using a high number of elements or compromising a vital characteristic.

Moreover, Fig. 9 illustrates and contrasts the dynamic response to an abrupt change in the duty cycle of the proposed converter and converters in [31-33]. It is noteworthy that all the converters deliver 100W power to the output load in this comparison and employ coupled inductors in their structure. Regarding Fig. 9, a sudden change in the duty cycle is applied at $t = 0.1s$ and the output voltage of the converters rises from 105V to 115V. While all the converters present relatively fast responses, the responses of the proposed converter and the converter in [33] are the fastest ones with lower oscillation, unlike the converters in [31] and [32].

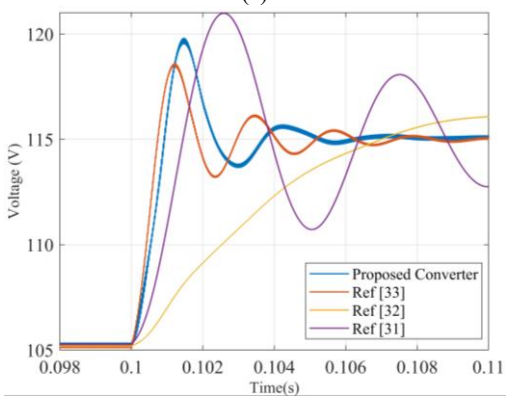
At the end of this section, the frequency response of the control to output transfer function for the proposed converter, the converter in [31], and CBC are drawn and compared in Fig. 10 using the parameters in TABLE 1. As can be seen, CBC has a negative phase margin and a gain margin. Hence, it is unstable. To make this comparison more straightforward, the main parameters of the bode plot, such as phase margin, gain margin, stability, and bandwidth of the studied converters, are summarized in TABLE 3. Although the proposed converter

TABLE 3 DETAILED FREQUENCY RESPONSE COMPARISON

Item	CBC	Ref [31]	The proposed converter
PM (degree)	-47.9	90.2	90.3
GM (dB)	-46.7	∞	∞
Stable	×	✓	✓
Band Width (kHz)	2.24	5.1	3.54



(a)



(b)

Fig. 9. (a) Response of the proposed converter and its peers against a sudden change in duty cycle, (b) Enlarged sketch of the responses.

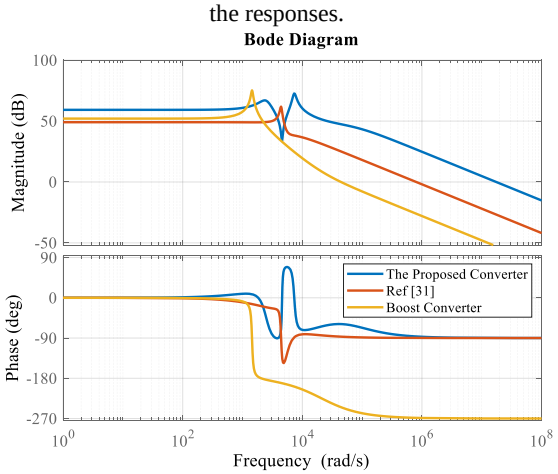


Fig. 10. Frequency response comparison.

and the converter in [31] have similar phase and gain margins, the proposed converter's bandwidth is less than [31].

VI. Experimental Results

Steady-state analyses are validated in this section using hardware-based experimental results. TABLE 4 also presents the laboratory prototype's elements and their values.

A 300 µH inductor is designed and implemented as the input inductor L. The implemented magnetizing inductance in the laboratory is 460µH. Fig. 13(a) sketches the applied pulse to the power switch's gate and the input current waveforms. This figure also confirms the proposed converter's low input current ripple characteristic. It should be noted that for the converter to behave like a minimum phase system, the size of elements should pass the criteria introduced in. The output voltage and leakage inductance's current waveforms are indicated in Fig. 13(b).

Time domain waveforms of the power switch's voltage and current are depicted in Fig. 13(c). Since the power switch's voltage stress is about 50V, half of the output voltage, a power switch with low $R_{DS(on)}$ can be chosen, resulting in lower power loss and higher power conversion efficiency.

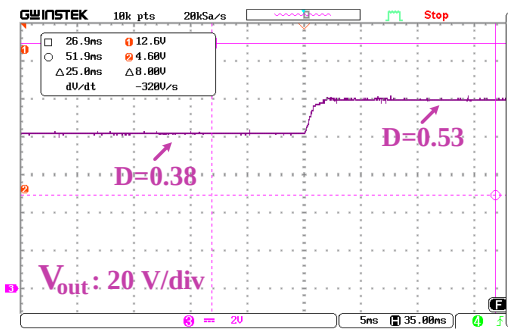


Fig. 11. Dynamic response of the proposed converter.

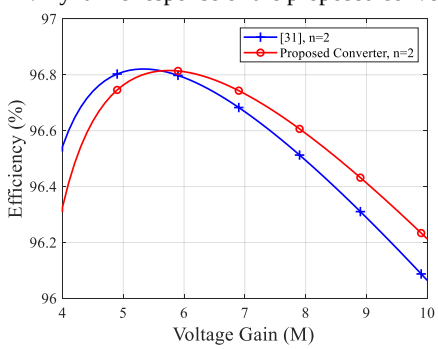


Fig. 12. Efficiency comparison of the proposed converter and [31].

Corresponding voltage and current waveforms of the diode D_{o1} are demonstrated in Fig. 13(d). Like the power switch, the voltage stress across D_{o1} is far lower than the output voltage. Besides, the measured voltage and current waveforms of the diode D_{o2} have been presented in Fig. 13(e). Even though the voltage stress of the diode D_{o2} is larger as compared to the power switch and the diode D_{o1}, it is not higher than the output voltage. Finally, Fig. 13(f) displays the implemented prototype of the converter.

Now, to corroborate the minimum phase performance of the proposed converter, the converter's dynamic response for a 40% step change in the duty cycle is shown in Fig. 11. As can be seen, the converter's output voltage does not have an undershoot as the duty cycle changes from 0.38 to 0.53. The efficiency of the proposed converter and the converter in [31] for a vast range of voltage gains is illustrated in Fig. 12 with the parameters outlined in TABLE 4. This figure reveals that although the proposed converter has more elements, it can

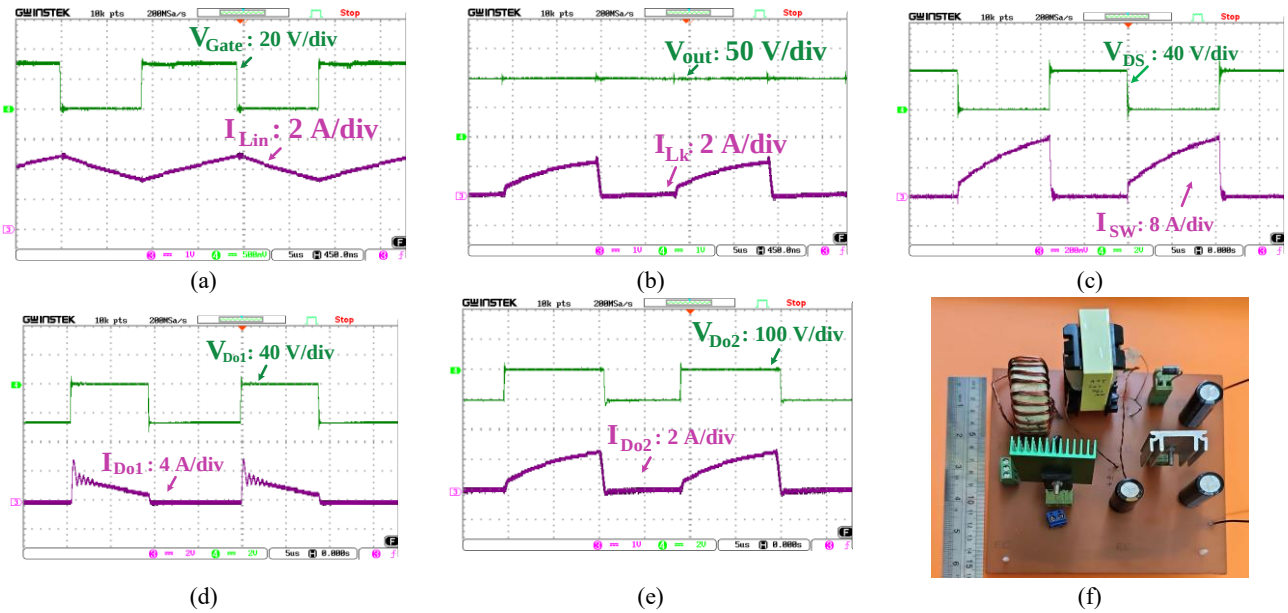


Fig. 13. Experimental results of the proposed minimum phase converter (a) Applied driving signal to the power switch and input current waveforms, (b) Output voltage and leakage inductance current waveforms, (c) Voltage and current waveforms of the power switch, (d) Voltage and current waveforms of the Diode D_{o1}, (e) Voltage and current waveforms of the Diode D_{o2}, and (f) Prototype of the converter.

offer better power conversion efficiency over a vast range of voltage gains compared to [31]. This sketch also approves that drawing a high ripple current from the input source leads to higher power loss. As a consequence of these results, the proposed converter can be utilized in various renewable energy applications and those requiring fast dynamic responses.

TABLE 4. HARDWARE SPECIFICATIONS.

Item		Specification
Output Power		100W
Output Voltage		100V
Input Voltage		25V
Switching Frequency		50kHz
Coupled Inductors (EE 42/21/15)	Turns Ratio	2
	Leakage Inductance	5 µH
	Magnetizing Inductance	460 µH
	Total Resistance	27mΩ
L_1		(T 184-52)/300 µH/ $r_L = 22m\Omega$
Capacitors (C_1, C_{o1}, C_{o2})		50 µF/65mΩ, 68 µF/47mΩ, 50 µF/65mΩ
Power Switch (S)		IRFB 4227 ($R_{DS} = 19.7m\Omega$)
Diodes	D_{o1}	MBR10100, ($V_f = 0.65V$)
	D_{o2}	MUR 440, ($V_f = 1.05V$)

VI. Conclusion

This paper proposes a minimum-phase DC-DC converter by making a path between the input source and output load. Accordingly, the converter can eliminate the right half plane zero inherently. Providing minimum phase feature and the following advantages altogether is the main contribution of this paper;

a) High voltage gain,

b) Low voltage stress across its semiconductors,

c) High power conversion efficiency,

d) Common ground sharing between its input and output ports,

and e) low input current ripple altogether. Despite the existence of converters with larger voltage gains, the proposed converter provides a respectable gain while maintaining the previously mentioned benefits. In addition, comprehensive theoretical and mathematical analysis, including steady-state analysis, small signal modeling, efficiency calculation, and so forth, have been done to lighten the novelty of the proposed converter. Aside from verifying the mentioned characteristics of the proposed converter through the experimental results, the presented comparison reveals its competitive features. Combining all the advantages of the proposed converter, one can inspect it as a proper choice for a vast range of applications.

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