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A New Quadratic CUK-Based Step-Up DC/DC Converter Without Right Hand Plane Zero

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ABSTRACT

In this paper, a new transformerless high step-up DC/DC converter with low input current ripple for renewable energy generation systems. This introduced circuit is based on a conventional quadratic boost converter with a CUK circuit. Therefore, the advantages of Cuk and quadratic boost converters such as continuity of the input and output currents have been maintained. In this suggested topology, switched capacitor and switched inductor techniques are also considered to obtain high voltage gains. The series connection of an inductor with the load causes the converter to have no right half plane zeros (RHPZ) in the transfer function; Thus, the proposed structure is able to provide fast dynamic behavior under the load variation than the other typical counterparts. The other advanced features of the introduced topology are its ultra-high voltage gain, continuous input current with low ripple, low voltage stress, and common ground between the input source and output load. The voltage conversion ratio of the suggested topology for both ideal and non-ideal modes has been provided. The operating principle, steady-state analysis along with comparison study of the proposed converter are discussed in detail. Finally, to confirm the theoretical analysis, a 80 W (20 V/ 160 V) hardware prototype is established.

I. Introduction

In recent decades, due to the importance of energy management, the use of renewable energy sources (RES) and batteries have been paid more attention. RESs are used in many applications such as renewable energy, energy harvesting, uninterruptible power supply (UPS), data centers, medical implantable devices, industrial, lighting technology, medical and military, automotive and railway technology, portable devices, gadgets, space and avionics, telecommunications, and physics research. Because of the low output voltage level of resources (< 48 V), the use of high voltage gain DC/DC converters as an interface circuit to create a desired output voltage is necessary [1-2]. For step-up dc-dc structures, high step-up capability and low input current ripple requirements are necessary for that are applied in RES applications [2]. Moreover, due to simple structure, and compact design, non-isolated structures of step-up converters are preferred for low-power applications.

In past years, conventional step-up power topologies such as Boost, SEPIC and Buck-Boost circuits with simple structures and low component counts have been introduced for high-voltage gain applications. However, in these converters, strong limitation on voltage conversion ratio limits their applications. Moreover, due to the use of a diode in the output side of the circuit, which leads to the discontinuity of the output current, a right half plane zero (RHPZ) is created, which leads to non-minimum phase (NMP) behavior in their transfer function and slow dynamic response [3, 4].

So far, many modified high voltage gain DC-DC topologies have been introduced. In these topologies, to raise the voltage conversion ratio, some effective boosting methods including voltage-lift, switched inductors (SI), switched capacitors (SC), cascading technique, voltage multipliers (VM) and coupled-inductor (CI) have been used [1, 2, 5]. It should be noted that

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in CI-based converters, the leakage inductance of the CI often causes high voltage spikes across the power switch which should be limited by adding auxiliary clamp circuits to the converter [6,7].

In recent years, many non-isolated transformerless converters with high voltage gain have been introduced. In [8, 9], two new types of quadratic boost step-up DC-DC converters are introduced. However, low voltage gain along with high input current ripple are demerits of the mentioned circuits, which limits their applications for RES systems. Using two power switches, high voltage gain DC-DC converter with low input current ripple and low voltage stress are suggested in [16-21]. In addition, in [22-23], some quadratic high-gain DC-DC converters based on extended capacitor-diode networks are presented. However, the lack of common ground between the input and output sides is the main disadvantage of these circuits. To solve the mentioned problem, ultrahigh step-up quadratic single-switch converters with continuous input current ripple are suggested in [24-28]. In addition, new non-isolated single-switch high gain converters with low input current ripple and common ground are proposed in [25-28]. Nevertheless, due to RHPZ, these converters are not able to provide a fast transient response.

One of the methods to eliminate the RHPZ is the continuity of the current on the output side of the circuit. For this purpose, in [29-32], step-up DC/DC converters with fast dynamic response and low input current ripple for low-power applications are presented. However, the mentioned circuits suffer from a low voltage gain ratio along with using two power switches. In [33] and [34], two new types of high-voltage gain DC-DC converters are suggested. However, because of the NMP feature, these structures are not able to provide a fast transient response.

Keeping in mind the merits and demerits of the discussed high step-up converters, this paper suggests a new topology of a non-isolated single-switch quadratic high voltage gain DC-DC converter without RHPZ for renewable energy source applications. The advantages of the proposed converter are as follows:

1- High voltage gain.
2- Common ground connection.
3- Low input current ripple.
4- A single power switch structure.
5- Minimum phase behavior.

II. Operational principles of the converter

The circuit diagram of the proposed circuit is shown in Fig. 1. In this introduced converter, there are seven didoes (D_1-D_7), one power switch (S), six capacitors (C_1-C_5, and C_o), along with four inductors (L_1-L_4). Regarding this figure, the proposed topology is a modified structure of a conventional quadratic boost topology, and a CUK converter. Thus, the proposed structure maintains the benefits of the quadratic boost and Cuk circuits such as continuity of the input and output current waveforms, and high voltage gain ratio. Moreover, in order to achieve high voltage gains under low voltage stress, voltage boosting techniques SC and SI are also considered in the converter. Therefore, high output DC voltages can be created at low duty cycles, which leads to efficiency improvement. Also, to restrict the voltage stress rate across the power switch (S), a simple passive clamp circuit including the diode D_7 and the capacitor C_5 is used. To simplify the analysis of the presented circuit, all switching devices are considered ideal. Fig. 2 shows the theoretical key waveforms of the proposed converter in one switching period. Furthermore, the circuit has two operating modes continuous conduction mode (CCM), which are depicted in Fig. 3.

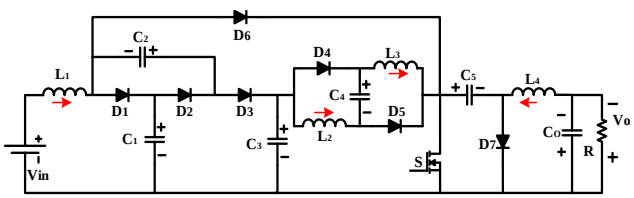


Fig. 1. The circuit configuration of the proposed converter.

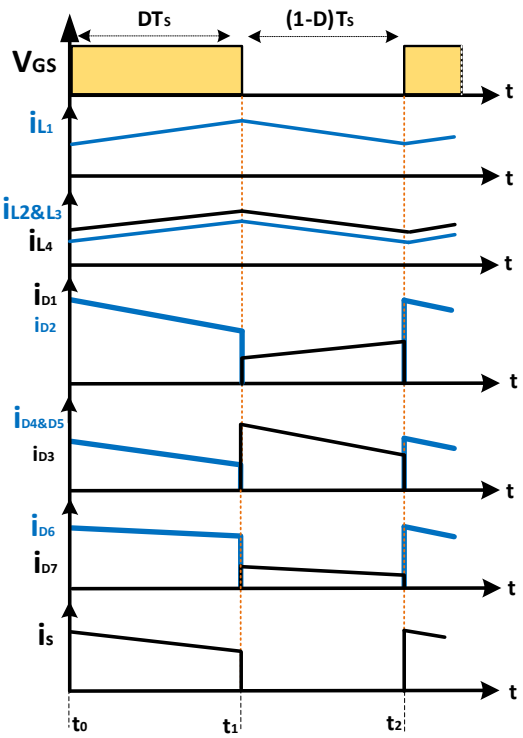
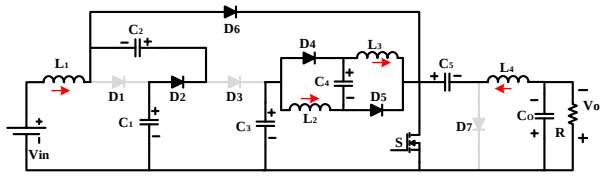
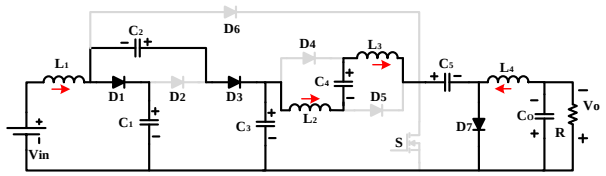


Fig. 2. The time-domain key waveforms of the converter.



(a)



(b)

Fig. 3. Equivalent circuits of the introduced converter; (a) Mode-1, (b) Mode-2.

Mode-1 [t_0 - t_1]: At t = t_0, the single power switch S is turned ON by applying PWM pulses. From Fig. 3-(a), during operating mode, the diodes D_2, D_4, D_5, and D_6 are also conducting, while other diodes of the circuit are off. In this time interval, the input inductor (L_1) is charging from the input DC voltage source; thus, its current is increased linearly. Furthermore, the middle inductors L_1, L_2 and also the capacitor C4 are charged from the voltages across the capacitor C_3 through the diodes D_4, D_5 and the power switch. Besides, the output inductance (L_4) gets charged due to the positive voltage induced from the capacitor C_5. Moreover, the capacitor C_2 receives energy from the capacitor C_1 through the power switch and diodes D_2 and D_6.

Mode-2 [t_1 - t_2]: As shown in Fig 3 (b), in the second operating mode, as soon as the active switch (S) at time $t = t_1$ is turned OFF, the diodes D_1, D_3 and D_7 begin to conduct. In this mode, the capacitors C_1 and C_3 start to charge from the input inductor current. moreover, the energies stored in the inductors L_2 and L_3 along with the capacitor C_4 are released to the capacitor C_5. During this interval, the output inductor (L_4) charges the output capacitor C_o.

III. Steady-State Analysis

A. Steady-State Equations

The voltage of the inductors and also the current of the converter capacitors during both operation modes can be stated as follows:

$$L_1 \frac{di_{L1}}{dt} = D(V_{in}) + (1-D)(V_{in} - V_{C1}) \quad (1)$$

$$L_2 \frac{di_{L2}}{dt} = D(V_{C3}) + (1-D)(V_{C3} + V_{C4} - \acute{V}) \quad (2)$$

$$L_3 \frac{di_{L3}}{dt} = D(V_{C3}) + (1-D)(\acute{V} - V_{C5}) \quad (3)$$

$$L_4 \frac{di_{L4}}{dt} = D(V_{C5} - V_o) + (1-D)(-V_o) \quad (4)$$

$$C_1 \frac{dV_{C1}}{dt} = D(-i_{D2}) + (1-D)(i_{L1} - i_{D3}) \quad (5)$$

$$C_2 \frac{dV_{C2}}{dt} = D(i_{D2}) + (1-D)(-i_{D3}) \quad (6)$$

$$C_3 \frac{dV_{C3}}{dt} = D(-i_{L2} - i_{D4}) + (1-D)(i_{D3} - i_{L3}) \quad (7)$$

$$C_4 \frac{dV_{C4}}{dt} = D(i_{D4} - i_{L3}) + (1-D)(-i_{L3}) \quad (8)$$

$$C_5 \frac{dV_{C5}}{dt} = D(-i_{L4}) + (1-D)i_{L3} \quad (9)$$

$$C_o \frac{dV_{Co}}{dt} = D(i_{L4} - I_o) + (1-D)(i_{L4} - I_o) \quad (10)$$

Which, D denotes duty cycle of the power switch (S).

A. Average Voltage and Current of the Energy Storage Components

By applying the volt-second balance principle across the circuit inductors of the converter and using (1)-(4), the average voltage across the capacitors of the converter can be achieved as follows:

$$\boldsymbol{V_{C1} = V_{C2} = \frac{V_{in}}{1-D}} \quad (11)$$

$$\boldsymbol{V_{C3} = V_{C4} = \frac{2V_{in}}{1-D}} \quad (12)$$

$$\boldsymbol{V_{C5} = \frac{4V_{in}}{(1-D)^2}} \quad (13)$$

$$\boldsymbol{V_{Co} = \frac{4DV_{in}}{(1-D)^2}} \quad (14)$$

Moreover, using the current second balance of the circuit capacitors, the average current value of the inductors of the converter can be obtained as follows:

$$\boldsymbol{I_{L1} = \frac{4DI_o}{(1-D)^2}} \quad (15)$$

$$\boldsymbol{I_{L2} = I_{L3} = \frac{DI_o}{1-D}} \quad (16)$$

$$\boldsymbol{I_{L4} = I_o} \quad (17)$$

According to equation (14), the voltage gain ratio of the suggested topology is increased exponentially versus the duty cycle in quadratic form, which leads to create an ultra-high voltage gain ratio.

B. Considering Parasitic Elements

Equation (14) shows the ideal voltage gain ratio of the proposed topology. However, the parasitic resistances of the components including inductors (r_L), switches (r_S), and diodes (r_D) are affected to the performance of each topology. The presence of parasitic resistors causes a drop in the voltage gain ratio of the converter, especially in high duty cycles. In the proposed topology, after the inclusion of these parasitic components, the non-ideal voltage gain is obtained as follow:

$$\frac{V_o}{V_{in}} = \frac{4D}{(1-D)^2}\left(1 - \frac{r_L}{R}\frac{4D}{(1-D)^4} - \frac{r_s}{R}\frac{4D^2}{(1-D)^4} - \frac{r_D}{R}\frac{4D}{(1-D)^3}\right) \quad (18)$$

Regarding (14) and (18), the ideal and non-ideal voltage gains of the presented topology have been compared in Fig. 4. From this figure, in the duty cycle range 0<D<0.5, the value of the ideal voltage gain is almost close to the non-ideal gain; thus,

their difference can be ignored.

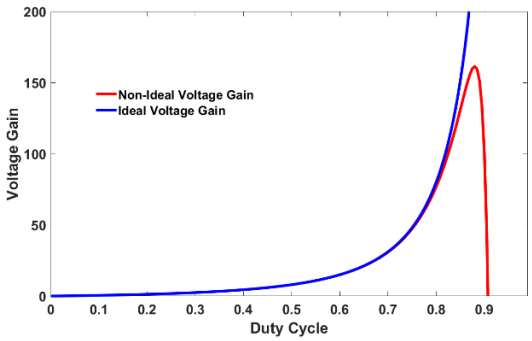


Fig. 4. Ideal voltage and non-ideal voltage gains of the proposed converter.

C. DCM Performance Analysis

D.1. Boundary Between CCM and DCM

In the proposed circuit, the boundary condition between CCM and DCM performances occurs when the input current reaches zero at the end of the switch period, in which case the currents of the diodes D_1 and D_3 fall to zero at $t=t_2$. Fig. 5 shows the current waveforms of the input inductor and the diodes D_1 and D3 at the boundary operation. With the help of converter operation modes, the slope of m_1 and m_2 of the input inductor current can be obtained as follows:

$$m_1 = \frac{V_{in}}{L_{1B}} \quad (19)$$

$$m_2 = \frac{-DV_{in}}{L_{1B}(1-D)} \quad (20)$$

Given the average value of input inductor current, and using (19) - (20), the boundary condition of the input inductance is derived as:

$$L_{1(min)} = \frac{DR}{2.f.M_{CCM}{}^2} \quad (21)$$

Regarding (21), the voltage gain, output load, and switching frequency affect the boundary condition value of the L_1.

D.2. Discontinuous Conduction Mode (DCM)

Fig. 6 illustrates the current waveforms of the input inductor and the diodes D_1 and D_3 under DCM mode. In DCM operation, according to the structure of the proposed topology and also by applying the volt-second balance principle on L_1, the average voltages of C_1 and C_2 are derived as follows:

$$V_{C1} = V_{C2} = \frac{1-\Delta}{1-D-\Delta} V_{in} \quad (22)$$

Which Δ is the time duration $t_2<t<t_3$, which the diodes D_1 and D_3 turn-off. In addition, the voltages of the other capacitors are achieved as:

$$V_{C3} = V_{C4} = \frac{2(1-\Delta)}{1-D-\Delta} V_{in} \quad (23)$$

Eventually, the voltage gain of the converter in DCM operation is obtained as follows:

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{(1-\Delta)4D}{(1-D)(1-D-\Delta)} \quad (24)$$

From (24), the time duration $1-\Delta$ as a function of the proposed converter parameters can be determined as:

$$1-\Delta = \frac{Q(M_{DCM})^2}{D} \quad (25)$$

Which, Q is defined as:

$$Q = \frac{2L_1 f_s}{R} \quad (26)$$

With substituting (59) into (56) and after rearranging, the voltage gain of the suggested circuit at DCM condition is calculated as:

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{4QD+2D\sqrt{Q(4Q+(1-D)^2)}}{2Q(1-D)} \quad (27)$$

D. Efficiency Interpretation

The power loss mechanism of the suggested circuit is provided in this part. The key parasitic parameters of the proposed circuit are listed in Table 1. The power loss of the power switch can be taken by

$$P_S = \frac{1}{2T_s}.V_{DS}(i_S^{t=on}.t_{on}) + \frac{1}{2T_s}.V_{DS}(i_S^{t=off}.t_{off}) + r_{DS(on)}.I^2_{S(RMS)} \quad (28)$$

$$P_s = \frac{16D}{(1-D)^4}\frac{r_S}{R}P_o \quad (29)$$

Here, $i_S^{t=on}$, $i_S^{t=off}$ are the switch current values at turn-on, turn-off instants. Also, the power loss of the diodes can be achieved as given below:

$$P_{Di} = r_{Di}.I^2_{D(RMS)} + V_{FDi}.I_{D(AVG)} \quad (30)$$

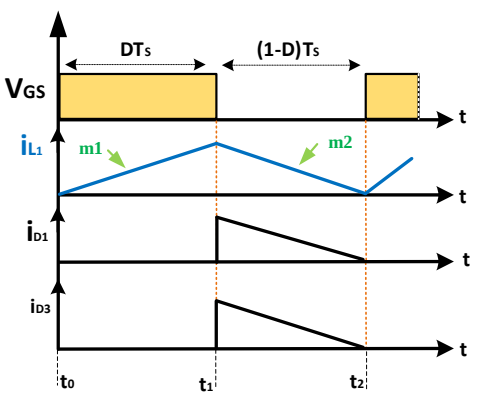


Fig. 5. The current waveforms of L_1 and Diodes D_1 and D_3 at the boundary condition between CCM and DCM mode.

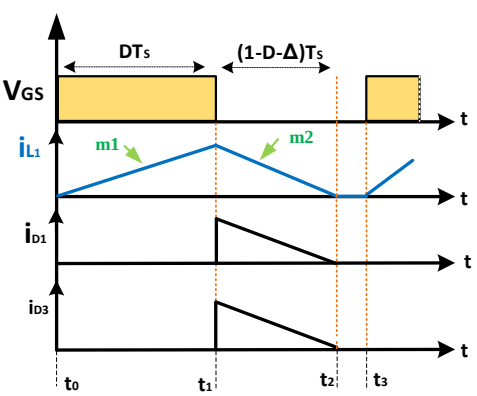
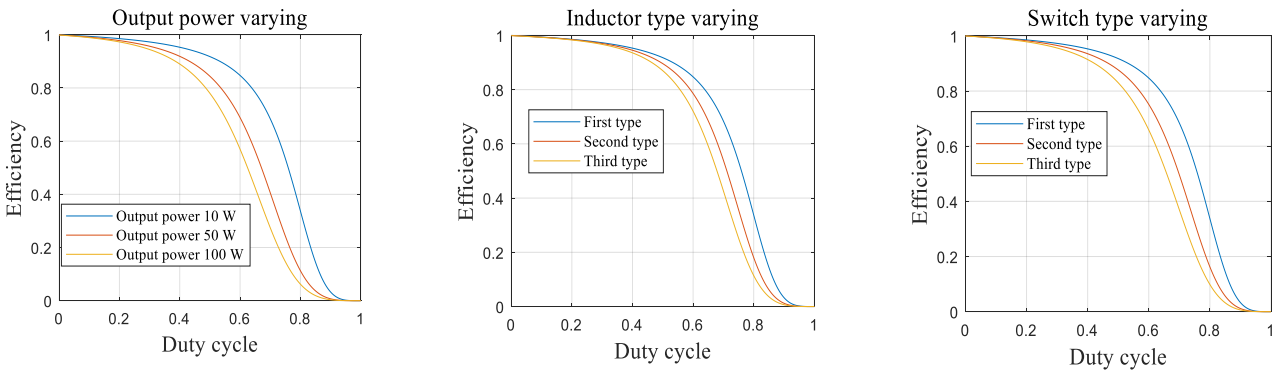


Fig. 6. The current waveforms of L_1, D_1 and D_3 at DCM.

$$x(t) =$$



(a) (b) (c)

Fig. 7. Theoretical efficiency of the presented converter versus duty cycle and parasitic parameters.

$$P_D = \frac{10D-6D^2}{(1-D)^2} V_{FD.} I_o \quad (31)$$

Besides, the power dissipation of the circuit capacitor is:

$$P_{Cap.i} = r_{Ci}.I_{Ci(RMS)}^2 \quad (32)$$

$$P_C = \frac{11D+D^3}{(1-D)^3}\frac{r_D}{R}P_o \quad (33)$$

Finally, the power loss of the magnetic components can be estimated as:

$$P_{Li} = r_{L_i}.I_{L_i}^2 + P_{Core} \quad (34)$$

$$P_L = \frac{3D^4-8D^3+24D^2-4D+1}{(1-D)^4}\frac{r_L}{R}P_o \quad (35)$$

Fig. 7 (a)-(c) shows the effect of the parasitic parameters of the proposed circuit versus the duty cycle per the theoretical efficiency. From these figures, the proposed converter can provide high power-handling capacities at high voltage gains.

TABLE 1 THE PARASITIC PARAMETERS OF THE CONVERTER.

Parameter	Description
$r_{DS(ON)}$	ON-state resistance of the active switch (MOSFET)
t_{on} , t_{off}	Turn-on and turn-off times of the switch
T_s	The switching cycle time of the single switch
ESR_i	Equivalent Series Resistance of the converter capacitors
V_{FDi}	Threshold voltage of the converter diodes
r_D	Diodes' Resistance in Forwarding State
r_{Lin}, r_{Ni}	Parasitic resistances of the magnetic components (L_{in},and CI)

IV. Derivation of the Small-Signal Model

In this part, the small signal derivation along with analyzes of the low-frequency behavior of the presented topology are provided. For this purpose, the state-space averaging technique is used [35]. In order to simple modeling of the circuit, the state-space averaging method is used. The state variables of the system include the inductor currents and capacitor voltages. Thus, the state vector of the proposed converter is defined as:

$$[i_{L1} \quad i_{L2} \quad i_{L3} \; i_{L4} \quad V_{C1} \quad V_{C2} \quad V_{C3} \quad V_{C4} \quad V_{C5} \quad V_{Co}] \quad (36)$$

To obtain the state equations of the converter, it is necessary to consider the parasitic resistances of the middle capacitors r_{C1}, r_{C2}, r_{C3}, and r_{C4} in series with the capacitors. According to the converter structure, the state equations of operating mode *I* ($t_0<t<t_1$) are expressed as:

$$L_1\frac{di_{L_1}}{dt} = V_{in} \quad (37)$$

$$L_2\frac{di_{L_2}}{dt} = L_3\frac{di_{L_3}}{dt} = -X_1 r_{C4} i_{L_2} - X_1 r_{C4} i_{L_3} + X_0 r_{C4} V_{C3} + (1 - X_0 r_{C4}) V_{C4} \quad (38)$$

$$L_4\frac{di_{L_4}}{dt} = V_{C5-}V_{Co} \quad (39)$$

$$C_1\frac{dV_{C1}}{dt} = X_3(V_{C2} - V_{C1}) \quad (40)$$

$$C_2\frac{dV_{C2}}{dt} = X_3(V_{C1} - V_{C2}) \quad (41)$$

$$C_3\frac{dV_{C3}}{dt} = (X_1 - 1)i_{L_2} + (X_1 - 1)i_{L_3} - X_0 V_{C3} + X_0 V_{C4} \quad (42)$$

$$C_4\frac{dV_{C4}}{dt} = -X_1 i_{L_2} - X_1 i_{L_3} + X_0 V_{C3} - X_0 V_{C4} \quad (43)$$

$$C_5\frac{dV_{C5}}{dt} = -i_{L_4} \quad (44)$$

$$C_o\frac{dV_{Co}}{dt} = i_{L_4} - \frac{V_{Co}}{R} \quad (45)$$

The state equations of mode *II* ($t_2<t<t_3$), are given as:

$$L_1\frac{di_{L_1}}{dt} = V_{in} - X_3 X_4 i_{L_1} + X_3 r_{C3} i_{L_2} + (-1 + X_3)V_{C1} + X_3 V_{C2} - X_3 V_{C3} \quad (46)$$

$$L_2\frac{di_{L_2}}{dt} = L_3\frac{di_{L_3}}{dt} = 0.5[X_2 r_{C3} V_{C1} - X_6 i_{L_1} + (r_{C4} + X_2 r_{C3}{}^2) i_{L_2} - X_1 r_{C4} i_{L_3} + (1 - X_2 r_{C3})V_{C3} + V_{C4} - V_{C5}] \quad (47)$$

$$L_4\frac{di_{L_4}}{dt} = -V_{Co} \quad (48)$$

$$C_1\frac{dV_{C1}}{dt} = X_2(r_{C2} + r_{C3})i_{L_1} - X_2 r_{C3} i_{L_2} + X_2(-V_{C1} - V_{C2} + V_{C3}) \quad (33)$$

$$C_2\frac{dV_{C2}}{dt} = [X_2(r_{C2} + r_{C3}) - 1]i_{L_1} - X_2 r_{C3} i_{L_2} + X_2(-V_{C1} -$$

$V_{C2} + V_{C3})$ (49)

$$C_3 \frac{dV_{C3}}{dt} = -[X_2(r_{C2} + r_{C3}) - 1]i_{L_1} + (X_2 r_{C3} - 1)i_{L_2} + X_2(V_{C1} + V_{C2} - V_{C3}) \quad (50)$$

$$C_4 \frac{dV_{C4}}{dt} = -i_{L_2} \quad (51)$$

$$C_5 \frac{dV_{C5}}{dt} = i_{L_2} \quad (52)$$

$$C_o \frac{dV_{Co}}{dt} = i_{L_4} - \frac{V_{Co}}{R} \quad (53)$$

Where, X_0-X_6 are defined as follows:

$$X_0 = \frac{1}{r_{c3}+r_{c4}} \quad ,X_1 = \frac{r_{c3}}{r_{c3}+r_{c4}} \ , \ X_2 = \frac{1}{r_{c1}+r_{c2}+r_{c3}} \ ,$$
$$X_3 = \frac{r_{c1}}{r_{c1}+r_{c2}+r_{c3}} \quad (54)$$

$$X_4 = r_{c2} + r_{c3} \quad ,X_5 = \frac{1}{r_{c1}+r_{c2}} \ , \ X_6 = 0.5(r_{c4} - X_2 {r_{c3}}^2 - r_{c3}) \quad (55)$$

The simulation results of the frequency response (Bode plot) control-to-output voltage (V_o/d) transfer function of the presented circuit is provided in Fig. 8. Also, the dominant pole and zero map of the transfer function is depicted in Fig. 9. The values of simulation parameters are selected as V_{in}=20V, D=0.5, R=200 Ω, L_1= 0.2mH, L_2= L_3= 8mH, L_4= 5mH, C_1= C_4= C_5=200uF, C_2=220uF, C_3=C_o=100uF and r_{C1}=0.1 Ω r_{C2}=0.2 Ω, r_{C3}=0.1 Ω, r_{C4}=0.1Ω. Regarding these figures, the suggested converter is stable without right half-plane (RHP) zero (minimum phase behavior (MP). This behavior is due to the use of an inductor in the output of the circuit (L_4), which leads to the continuity of the circuit current on the output side and therefore the MP behavior. It is noteworthy that one of the prominent features of most current-fed high step-up converters is NMP behavior which led to an inverse response, narrow bandwidth, low transient response and destabilization in higher voltage gain.

V. Comparison with Other Topologies

In this part, a comparative study between the presented quadratic high voltage gain converter and other similar converters is provided. For this purpose, some typical key indicators including the number of components, voltage conversion ratio, input current ripple, minimum phase

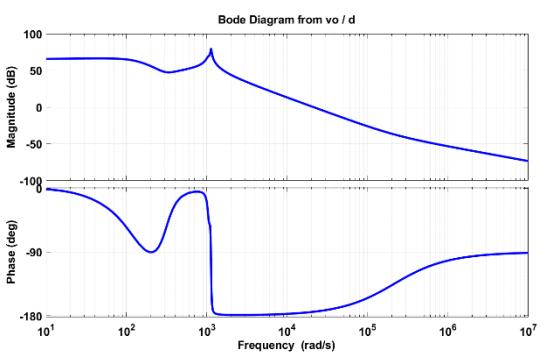


Fig. 8. Bode diagram Control-to-output transfer function $G_{vo\text{-}d}$

of the proposed converter.

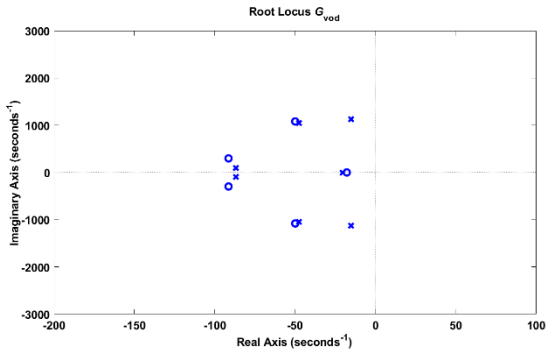


Fig. 9. Root locus graph for control-to-output voltage transfer function G_{vod}.

behavior, and voltage stress are considered, which are summarized in Table 2. From the table, the converters in [3], [29]-[32] have minimum phase (MP) behavior which leads to a fast transient response. Also, low input current ripple is the main demerit of the converters in [17], [19], [32] and [3] that limits their applications for RES. Moreover, converters [28] and [12] suffer from the lack of common ground between input DC source and output load.

Fig. 10 represents the voltage gain comparison of the converters given in the comparison table. Regarding this figure, the proposed converter along with the converters in [11], [12], [17] and [25] can provide higher output DC voltage gains than the other counterparts. However, these converters suffer from a high input current ripple (in [17]), the lack of common ground (in [12]), NMP behavior (in [11], [12], [19], and [25]) and use two active switches (in [17]). Also, among MP structures, the proposed converter has a higher voltage gain. Moreover, the experimental efficiency along with the characteristics of the circuit implemented in different converters was prepared in the comparison table. According to the table, compared to other converters, the proposed converter is able to provide proper efficiency.

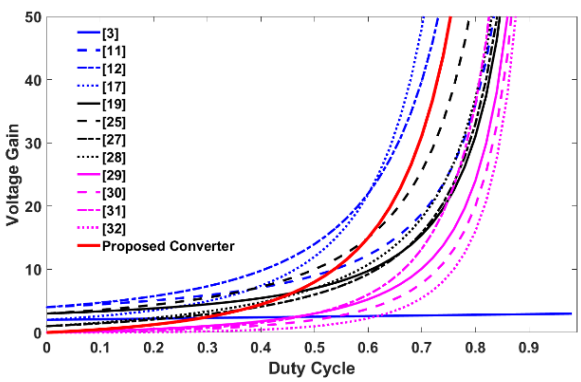


Fig. 10. Total voltage gain comparison.

TABLE 2 PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH OTHER COUNTERPARTS.

Converter	No. of Components S/D/C/L	Voltage Gain	Low Input Current Ripple	Minimum Phase Behavior	Maximum Voltage Stress on Switch	Maximum Voltage Stress on Diodes	Common Ground	Sample prototype specifications Vin/Vo/f/ Po/Eff.
[3]	2/4/5/1	2+D	No	Yes	$\frac{V_o}{2+\mathrm{D}}$	$\frac{V_o}{2+\mathrm{D}}$	Yes	26V/44V/50 KHz/100W/92.8%
[11]	1/5/4/2	$\frac{(2-D)^2}{(1-D)^2}$	Yes	No	$\frac{V_o}{2-\mathrm{D}}$	$\frac{V_o}{2-\mathrm{D}}$	Yes	10V/70V/50 KHz/ 200W/88%
[12]	1/9/5/3	$\frac{4-2\mathrm{D}+2D^2}{(1-D)^2}$	Yes	No	$\frac{(1+D)V_o}{4-2\mathrm{D}+2D^2}$	$\frac{(1+D)V_o}{4-2\mathrm{D}+2D^2}$	No	-
[17]	2/5/4/3	$\frac{2-\mathrm{D}}{(1-D)^3}$	No	No	$\frac{1-\mathrm{D}}{2-D}V_o$	$\frac{1}{(1-D)^2}V_o$	Yes	24V/340V/20KHz/ 500W/93%
[19]	2/3/3/2	$\frac{3-3\mathrm{D}+D^2}{(1-D)^2}$	No	No	$\frac{V_o}{3-3\mathrm{D}+D^2}$	$\frac{(2-D)V_o}{3-3\mathrm{D}+D^2}$	Yes	20V/190V/25 KHz/ 123W/94%
[25]	1/6/4/3	$\frac{3-\mathrm{D}}{(1-D)^2}$	Yes	No	$\frac{2V_o}{3-\mathrm{D}}$	$\frac{(1+D)V_o}{3-\mathrm{D}}$	Yes	20V/200V/50 KHz/ 100W/89%
[27]	1/5/6/4	$\frac{1+2\mathrm{D}-2D^2}{(1-D)^2}$	Yes	No	$\frac{V_o}{1+2\mathrm{D}-2D^2}$	$\frac{V_o}{1+2\mathrm{D}-2D^2}$	Yes	24V/222V/50 KHz/ 200W/90%
[28]	1/6/8/5	$\frac{1+3\mathrm{D}-3D^2}{(1-D)^2}$	Yes	No	$\frac{V_o}{1+3\mathrm{D}-3D^2}$	$\frac{V_o}{1+3\mathrm{D}-3D^2}$	No	20V/200V/50 KHz/ 180W/90%
[29]	2/2/3/3	$\frac{\mathrm{D}(2-\mathrm{D})}{(1-D)^2}$	Yes	Yes	$\frac{V_o}{\mathrm{D}(2-\mathrm{D})}$	V_o	Yes	-
[30]	2/2/3/3	$\frac{\mathrm{D}}{(1-D)^2}$	Yes	Yes	$\frac{V_o}{\mathrm{D}}$	$\frac{V_o}{\mathrm{D}}$	Yes	18V/48V/40 KHz/ 48W/89%
[31]	2/3/4/3	$\frac{\mathrm{D}(1+\mathrm{D})}{(1-D)^2}$	Yes	Yes	$\frac{V_o}{\mathrm{D}}$	$\frac{V_o}{\mathrm{D}}$	Yes	-
[32]	2/2/3/3	$\frac{D^2}{(1-D)^2}$	No	Yes	$\frac{V_o}{\mathrm{D}}$	$\frac{V_o}{\mathrm{D}}$	Yes	20V/100V/50 KHz/ 100W/92%
Proposed Converter	1/7/6/4	$\frac{4D}{(1-D)^2}$	Yes	Yes	$\frac{V_o}{\mathrm{D}}$	$\frac{V_o}{\mathrm{D}}$	Yes	20V/160V/50 KHz/ 80W/93%

V. Design Considerations

In this part, the design considerations of the presented topology are discussed. Duty cycle of the power switch is achieved from the desired voltage gain ratio (14) as:

$$D = \frac{2G+4-4\sqrt{1+G}}{2G} \quad (56)$$

In (40), G is the voltage conversion ratio of the circuit. Due to the degrading effects of high current ripple from RES such as short lifetime, circuit design in CCM with low input current ripple is preferred. Considering allowable input current ripple ($\Delta I_{in} \approx 20\%.I_{in}$), the minimum value of the input inductance L_1 of the converter can be determined as:

$$L_1 > \frac{V_{L1}.D}{\Delta I_{in}.f_s} = \frac{V_{in}.D}{\Delta I_{in}.f_s} \quad (57)$$

Where, f_s is the switching frequency of the single power switche. Moreover, the proper values of the other inductors of the proposed circuit (L_2, L_3 and L_4) are calculated as:

$$L_2 > \frac{2D.V_{in}}{\Delta I_{L2}.(1-D)f_s} \quad (58)$$

$$L_3 > \frac{2D.V_{in}}{\Delta I_{L3}.(1-D)f_s} \quad (59)$$

$$L_4 > \frac{(1-D).V_o}{\Delta I_{L4}.f_s} \quad (60)$$

Based on the allowable output voltage ripple (ΔV_{Co}), the value of the output capacitance C_o can be given as:

$$\boldsymbol{C_o > \frac{(1-D).V_o}{8.L_4\Delta V_{co}.f_s^2}} \quad (61)$$

Furthermore, the proper values of the other used capacitors in the presented circuit can be designed as:

$$C_1 > \frac{2D.I_o}{\Delta V_{C1}(1-D)f_s} \quad (62)$$

$$C_2 > \frac{2D.I_o}{\Delta V_{C2}(1-D)f_s} \quad (63)$$

$$C_3 > \frac{D(1+D).I_o}{\Delta V_{C3}(1-D)f_s} \quad (64)$$

$$C_4 > \frac{D.I_o}{\Delta V_{C4}f_s} \quad (65)$$

$$C_5 > \frac{D.I_o}{\Delta V_{C5}f_s} \quad (66)$$

With the help of this non-ideal voltage gain, the real maximum voltage rates across the semiconductor elements can be determined as follows:

$$V_S = V_{D7} = \frac{4V_{in}}{(1-D)^2} = \frac{V_o}{D}.\alpha \quad (67)$$

$$V_{D1} = V_{D2} = V_{D3} = \frac{V_{in}}{1-D} = \frac{(1-D)V_o}{4D}.\alpha \quad (68)$$

$$V_{D4} = V_{D5} = \frac{2V_{in}}{1-D} = \frac{(1-D)V_o}{2D}.\alpha \quad (69)$$

Which, α is defined as:

$$\alpha = \frac{1}{\left(1-\frac{r_L}{R}\frac{4D}{(1-D)^4}-\frac{r_S}{R}\frac{4D^2}{(1-D)^4}-\frac{r_D}{R}\frac{4D}{(1-D)^3}\right)} \quad (70)$$

VI. Experimental Validation

In order to verify the performance of the introduced circuit, an 80W sample prototype with an input voltage of V_{in}=20 V and V_o=160V was built in the laboratory. The specifications of the components used to implement this sample prototype are summarized in Table *3*.

Fig.11 (a) shows the DC voltage of the output load of the converter in the sample prototype of the introduced circuit. Also, the measured voltage stresses of the switching components (MOSFET and diodes) components are presented in Fig. 11 (b)-(e). The current waveforms of the switching components of the proposed converter are illustrated in Fig. 11 (f)-(l). Also, Fig. 11 (m) presents the experimental results of the dynamic responses of the output voltage and the output

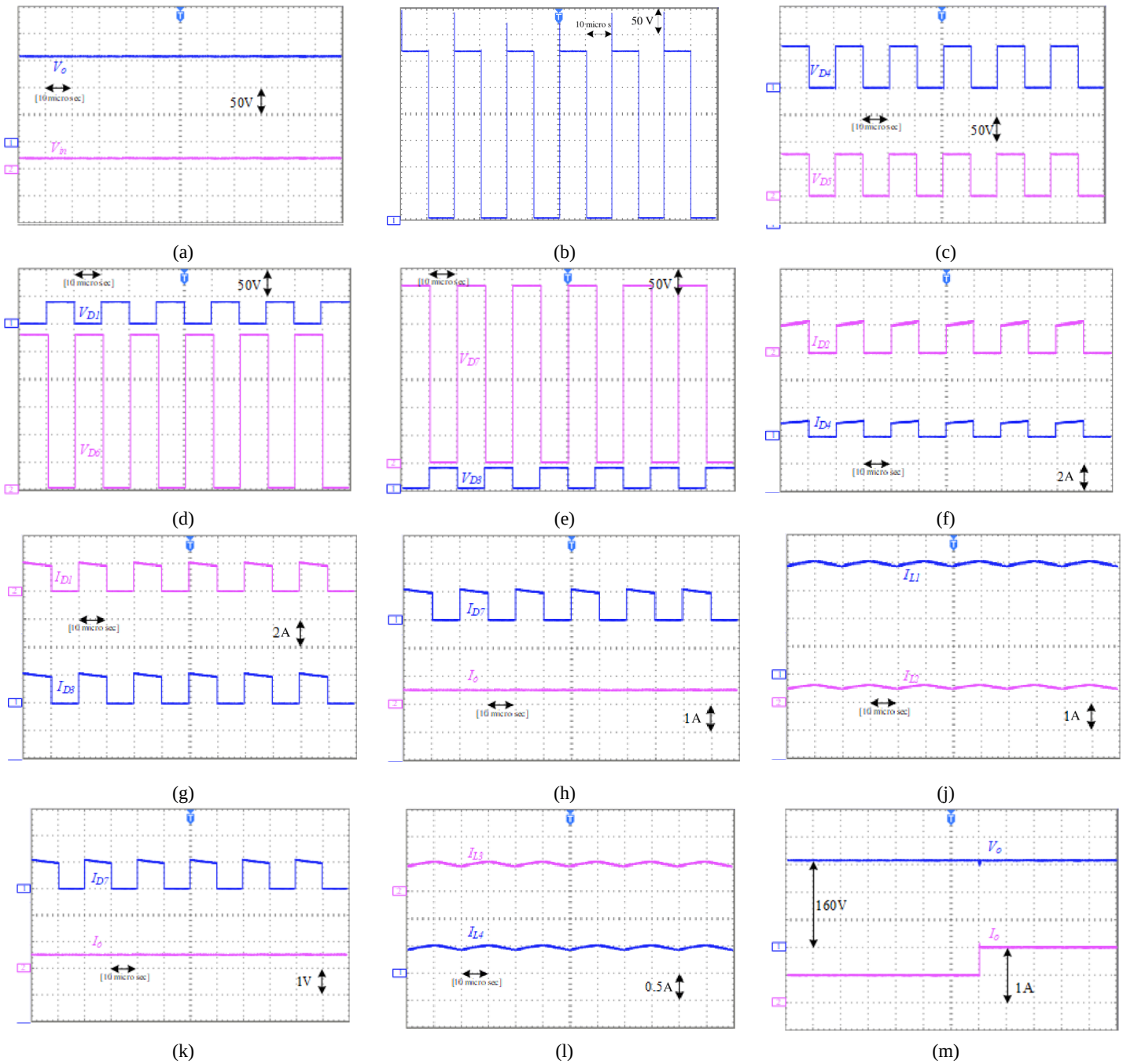
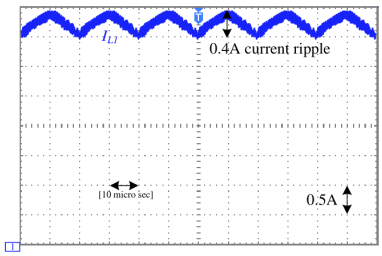
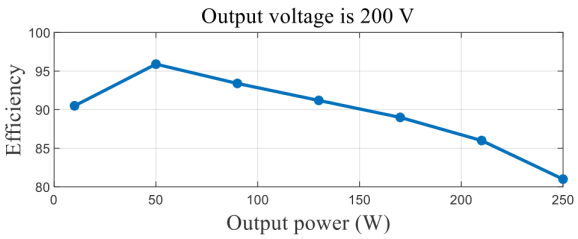


Fig. 11. Experimental results. (a)V_o and V_{in} (b) V_s (c) V_{D4}, V_{D5}, (d) V_{D1}, V_{D6}, (e) V_{D7}, V_{D3}, (f) I_{D2}, I_{D4}, (g) I_{D1}, I_{D3}, (h) I_{D7}, I_o, (j) I_{L1}, I_{L2}, (k) I_{D7}, I_o, (l) I_{L3}, I_{L4}, (m) Dynamic response of the output voltage along with the output load current of the proposed circuit under the output load changing from R_L=320Ω to R_L=160Ω.

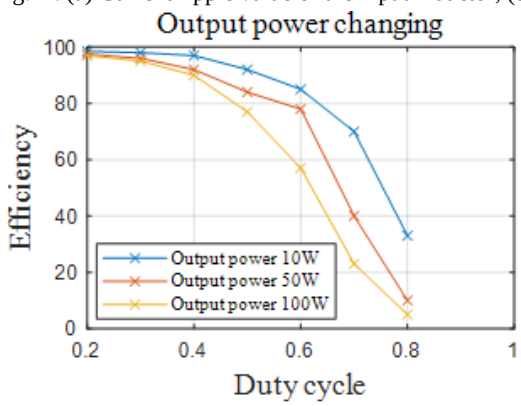


(a)

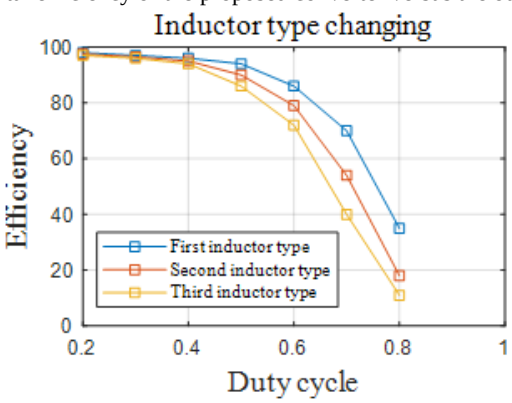


(b)

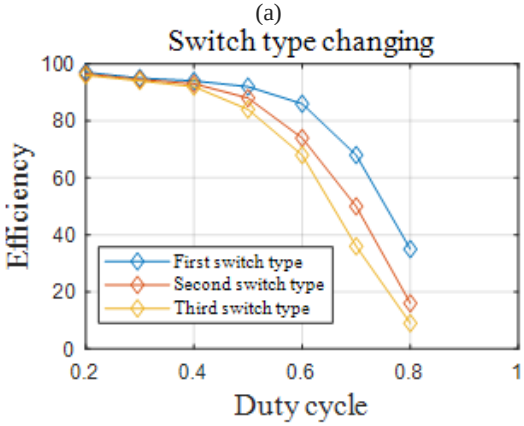
Fig.12. (a) Current ripple value of the input inductor, (b) Experimental efficiency of the proposed converter versus the output power.



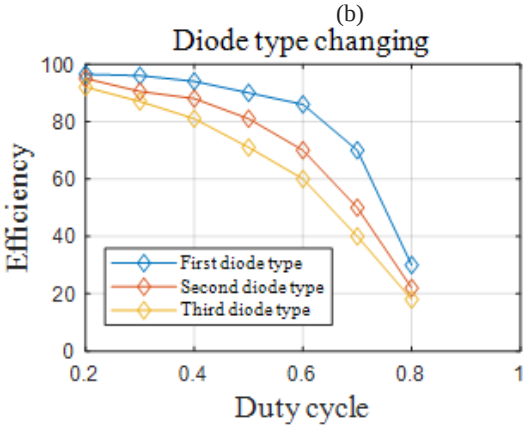
(a)



(b)



(c)



(d)

Fig.13 . Experimental results of the efficiency versus, (a) output power, (b) inductor types, (c) power switch type.

TABLE *3* KEY PARAMETERS OF PROTOTYPE SETUP.

Parameter	Values
Output Power (P_{out})	80 W
Input Voltage (V_{in})	20 V
Output Voltage (V_o)	160 V
Switching Frequency (f_s)	50 kHz
Capacitors C_1 –C_o	190 µF
Power Switch S	IRFP250
Input Inductor L_{in}	210 µH / EE42/21/20
Inductors L_2, L_3, L_4	2 mH
Diodes D_1 – D_7	SFF100-04CT

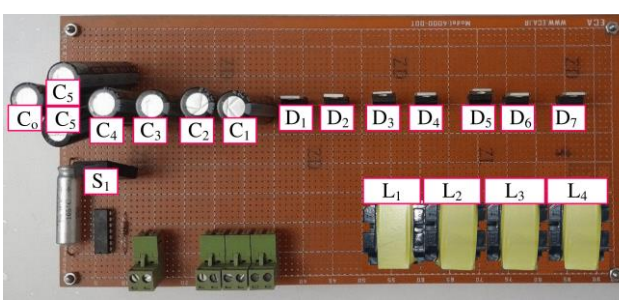


Fig. 14. Picture of the proposed converter prototype.

load current of the introduced circuit at a step change in the output load from R_L=320Ω to R_L=160Ω.

In addition, according to Fig. 12 (a), the input current is continuous with low ripple. From this figure, the value of input current ripple in the proposed converter is about 0.4A.

Moreover, the experimental efficiency of the proposed converter under the output power is provided in Fig. 12 (b). regarding this figure, the maximum efficiency of the suggested topology is about 0.93%.

I. Conclusion

A new transformerloss high voltage gain of quadratic CUK-based DC-DC converter with low input current ripple has been suggested in this paper. The introduced circuit provides unique features, including minimum phase behavior, high voltage gain ratio, enough high efficiency, and common ground between the source and load sides. Operating principles along with the steady-state analysis of the proposed converter are thoroughly explained. Then the converter is compared with other similar circuits, and the advantages of the suggested topology are shown. Moreover, the low-frequency behavior of the introduced circuit is obtained and its minimum phase feature is analyzed. The experimental results from a sample prototype 80*W*, 20V-160V have verified the feasibility of the presented converter design. Moreover, the sensitivity analysis of the efficiency and voltage gain at different inductors, switches and diodes are provided.

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In addition, the experimental efficiency of the proposed circuit at different output powers, switch and inductor types at V_o =160 V are measured which are presented in Fig. 13. A Photograph of the sample prototype of the proposed converter is also presented in Fig. 14.

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