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The Design and Simulation of an Efficient Quaternary Full-Adder Based on Carbon Nanotube Field Effect Transistor

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ABSTRACT

An essential reason for implementing multilevel processing systems is to reduce the number of semiconductor elements and hence the complexity of the system. Multilevel processing systems are realized much easier by carbon nanotube field effect transistors (CNTFET) than by MOSFET transistors due to the CNTFET transistors' adjustable threshold voltage capabilities. This paper presents an efficient quaternary full-adder based on CNTFET technology that consists of two half-adder blocks, a quaternary decoder, and a carry generator circuit. The proposed architecture combines the base-two and base-four circuit design techniques to take full advantage of both techniques, namely, simple implementation and low chip area occupation of the entire proposed quaternary full-adder. The proposed structure is evaluated using a Stanford 32nm CNTFET library in HSPICE software. The simulation results for the proposed full-adder structure that utilizes a 0.9-V supply voltage reveal that the power consumption, propagation delay, and energy index are equal to 2.67 μW, 40 ps, and 10.68 aJ, respectively.

NOMENCLATURE

$n_1.n_2$	Chiral vector
D_{cnt}	The diameter Carbon Nanotube (CNT)
E_π	π–π junction energy of carbon
V_{fb}	The flat band voltage
V_{dsi}	The drain to source voltage
δ	The Drain Induced-Barrier Lowering (DIBIL) coefficient in CNT

I. Introduction

While circuits and systems were primarily designed to operate by turning the vacuum tubes on and off, the idea of silicon transistor-based design was quickly considered by the electronics industry after its invention. Silicon (Si), which is an element with semiconductor properties that is found in abundance in nature, has become the main material in making transistors that are smaller and cheaper tools than previously used vacuum tubes, and it was possible to replace vacuum lamps in a short time [1].

Recently in an interesting attempt to follow the path of previous progress, some researchers have suggested replacing Si transistors with carbon nanotubes due to their better performance in realizing logic circuits [2-5]. This is due to the fact that the inevitable reduction in MOSFET transistor channel size and hence the appearance of the nanotechnology properties have posed major problems and challenges to implementing CMOS technology [6]. Issues, such as high leakage current, short channel length and very large channel length modulation, high power consumption, and high sensitivity to process variations have disrupted the dimensional process and degraded the proper performance of CMOS technology [7-9].

In binary logic, the power supply voltage of the circuit is divided into two levels of logic, i.e. 0 and 1. Making multi-level processing circuits reduces the consumption level and the connections between the blocks, but transistors are needed to make these circuits. It should be considered that the construction

of multi-level circuits with CMIS transistors is complicated.

In recent years, in order to provide high-speed processing systems, many researchers have focused on researching optical processing systems, including optical-based processing systems, including full-adders [10-13], multiplexers [14], encoders [15], and decoders [16]. Also, new technologies introduced in recent years, such as carbon nanotube transistors, have facilitated the implementation of this type of circuit and solved some of their problems, causing more and more designers to pay attention to this multilevel logic. One of the most important strengths of carbon nanotube transistors is that their threshold voltage can be adjusted by changing the diameter of the nanotubes, allowing Multi-Valued Logic (MVL) to be designed with less complexity and higher simplicity [2, 17-21]. Since the operation of CNTFET and MOSFET transistors are very similar, it is possible to design and implement simpler multilevel processing circuits by modeling the circuit design process using CMOS transistors. Quantum-dot Cellular Automata (QCA) is a new technology to eliminate some of the problems of existing technologies, such as CMOS. This study was concerned with designing an efficient full-adder circuit by using QCA technology [22].

With these explanations, MVL is a suitable alternative to binary processing systems [18, 24], which can solve and optimize the complexity of connections expressed by binary systems in VLSI circuits [9, 24]. Multilevel circuits can be used to solve binary problems [6].

The most common and efficient way to design MVL circuits is to use the known multi-threshold voltage CMOS technology experiences [11]. Due to the similarity of the MOSFET and CNTFET transistors in terms of their electrical properties, many CMOS structures that have already been designed can be implemented by CNTFET technology without any significant modifications [19]. In general, CNTFET transistors are faster and less energy-consuming than MOSFETs. In addition, in recent years, some multilevel circuits based on CNTFET transistors have been proposed that take advantage of the unique properties of carbon nanotube transistors [18, 13, 26-29]. A 2-trit ternary ALU using CNTFETs and RRAM as the basic design elements has been presented in [30]. The proposed ternary ALU modules are implemented, taking advantage of the variable multi-threshold design method of CNTFET and multilevel cell characteristics of Resistive Random Access Memory (RRAM) [30]. A design of quaternary multiplexer 4:1 with CNFETs has been proposed in which quaternary successor, predecessor, and second-level successor cells are introduced based on CNTFETs with single and three-supply voltage. All the above-mentioned designs have been applied to quaternary half-adder and full-adder circuits [31]. A one-bit full adder has been reported by Ebrahimy [32] designed by the proposed majority gates, which has only 0.75 clock cycle latency and suitable arrangements of inputs and outputs that give them the multi-bit extensibility feature.

A new memory element has reportedly been designed by magnetic tunnel junction spintronic device [33-34]. Magnetic tunnel junctions have special characteristics, such as high endurance, low leakage current, and ease of 3-D integration with CMOS and CNTFET technologies [35].

A fabrication process of CNTFET and magnetic tunnel junctions did not interfere with the fabrication of CMOS. Manufacturing of CNTFET has been reported in [36], which shows the compatibility of CNTFET with CMOS. As a result, it is possible to fabricate CNTFET, magnetic tunnel junction, and CMOS devices in a single chip [37-38].

In recent years, several modern analog and digital circuits have been fabricated based on CNTFET. Also, hybrid circuits in which CNTFET and Magnetic Tunnel Junction (MTJ) are used have been presented [39-40].

This paper proposes quaternary half-adder and full-adder structures realized by converting signals from quaternary to binary. Fewer transistors are used in the proposed architectures applying innovative circuit techniques, resulting in lower power consumption satisfactorily.

The paper is organized as follows. Section 2 explains the physical structure of CNTFET. Section 3 presents the conceptual circuitry and also the CNTFET transistor level realization of two different three-level adders based on CNTFET technology. A unique feature of adjusting the desired threshold voltage using suitable diameters and considering the mobility coefficient has been adopted [3]. In this section, the CNTFET-based quaternary full-adder and half-adder structures are explained in detail. The simulation results are provided in Section 5 and Section 6 concludes the paper.

II. A brief description of CNTFET

Carbon nanotubes are composed of graphite sheets tubed inside concentric cylinders with nanometer diameter and micrometer length. Carbon nanotubes are divided into single-walled (SWNT) and multi-walled (MWNT) based on their number of layers. Single-walled carbon nanotubes are the result of the complexity of a single layer of graphite, while multi-walled carbon nanotubes are the result of the complexity of several layers of nested graphite. The properties of nanotubes depend on their structure and act as metal or semiconductors depending on the chirality. The second characteristic of nanotubes that is affected by their electrical properties is the number of walls. The main difference between single-walled and multi-walled is the diameter of the nanotubes [22].

The arrangement of carbon atoms along the tube defines the chiral vector and is denoted by a correct pair (n1,n2). Based on the chiral vector, CNT can be conductive or semiconductor. If n1=n2 or n1-n2=3i, the nanotube is metal; otherwise, it is a semiconductor [41].

The diameter of CNT has a key role in the electrical characteristics of transistors. The equation of the diameter CNT is:

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \quad (1)$$

where a0=0.142 nm, π=3.14, and n1,n2 are chirality vectors [22].

In the structure of CNTFET components, one or more non-doped semiconductor SWCNTs are used as semiconductor channel material instead of Si bulk in the MOSFET structure [22].

The use of single-walled semiconductor carbon nanotubes as a substitute for Si channel field-effect transistors has major advantages, such as lower electron scattering, higher thermal conductivity, very high electrical conductivity, and high tensile strength.

Therefore, carbon nanotube circuits have much less latency than Si circuits. Also, a CNT transistor, like a MOSFET, has a

threshold voltage that is actually needed to turn on the transistor through the electrostatic gate. A very important advantage of CNTFET is that its threshold voltage can be adjusted by changing the diameter of the carbon nanotubes. In the CNTFET, the mobility of holes and electrons is the same.

This practical feature makes CNTFETs much more flexible for designing digital circuits than MOSFETs. It also makes the technology very suitable for designing multi-voltage threshold circuits.

The threshold voltage of a CNTFET can be calculated by Eq. 2:

$$V_{th} = \frac{2a_0E_\pi}{D_{CNT}} + V_{fb} - \delta \cdot V_{dsi} \quad (2)$$

in which a is the atomic distance of carbon to carbon, Eπ is π–π junction energy of carbon (Eπ =3.3eV), DCNT is the diameter of the carbon nanotube, Vfb is the flat band voltage, Vdsi is the drain to source voltage, and δ is the drain induced barrier lowering (DIBIL) coefficient in CNT [39-40].

This diameter can be calculated by Eq. 3 in which the CNTFET threshold voltage is an inverse function of the CNT diameter:

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1n_2}}{\pi} = 0.0783\sqrt{n_1^2 + n_2^2 + n_1n_2} \quad (3)$$

A carbon nanotube transistor looks like a MOSFET with the same pins. In other words, the principles of operation of carbon nanotube field effect transistors are similar to current Si transistors [22].

Fig. 1 shows the physical appearance of a carbon nanotube transistor. The nanotube remains not doped in the area below the gate.

The two ends of the nanotube that are connected to the source and drain connections are doped areas. The voltage applied to the gate of the transistor can control the electrical conductivity of the carbon nanotube in the area below the gate by changing the electron density in the channel.

The distance between the cross-sectional centers of two adjacent carbon nanotubes below the transistor gate is called a "pitch", which significantly affects the width of the gate and the drain and source of the transistor. Interestingly, the PCNTFET and NCNTFET have the same current rate.

The gate width of the transistor can be estimated based on Eq. 4, in which N is the number of nanotubes under the gate, DCNT is the diameter of the nanotube, and Wmin is the minimum possible width for the gate, which is determined based on lithographic constraints.

$$W_{gate} \approx Max(W_{min}(N-1)pitch + D_{CNT}) \quad (4)$$

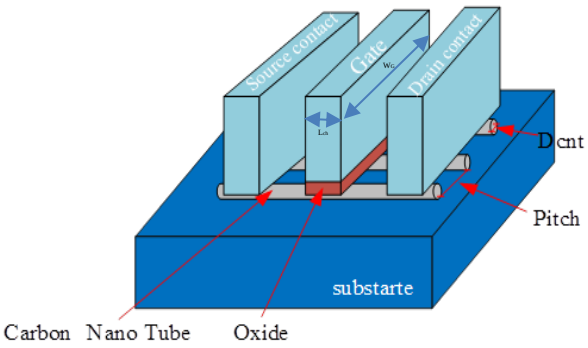


Fig. 1. The structure of CNTFET [23].

III. The Conceptual Scheme for quaternary Full-dder

The quaternary full-adder circuit, like the conventional full-adders, has three inputs, namely A, B, and Cin, and two outputs, namely, Sum and Cout. Quaternary digits A, B, Cin, and Sum have the same quaternary weight while Cout has a higher quaternary weight which must be used by the next addition block. In other words, the Carry input, Cin, of full-adders is supplied from the lower stage, while Cout, which indicates the carry-out, is transmitted to the upper stage, and Sum output is the sum of inputs A and B along with Cin. Unlike the conventional full-adders, which include two half-adders and a carry generator, the proposed quaternary full-adders have some complex design procedures and include half-adders, Q-Decoders, and carry generators. Two quaternary full-adders are proposed, and their half-adders are exhibited by Q- Decoders along with "Sum and Carry" and "Sum and Carry_bar" in Fig. 2 and Fig. 3, respectively [29]. The first quaternary full-adder shown in Fig. 2 that uses "Sum and Carry" in its half-adder is the initial not optimized version, while the second quaternary full-adder uses "Sum and Carry_bar" to reach an optimized design approach. The structure of a quaternary half-adder has two inputs and two outputs. Each input can be 0, 1, 2, or 3. In fact, input 0 means zero voltage, input 1 means VDD/3 voltage level, input 2 means 2VDD/3, and input 3 means VDD voltage level. In the following, we explain the architecture of the whole full-adder circuitry at the transistor level and block diagram.

A. The proposed full-adder architecture

The initial idea to realize a quaternary block is shown in Fig. 2.

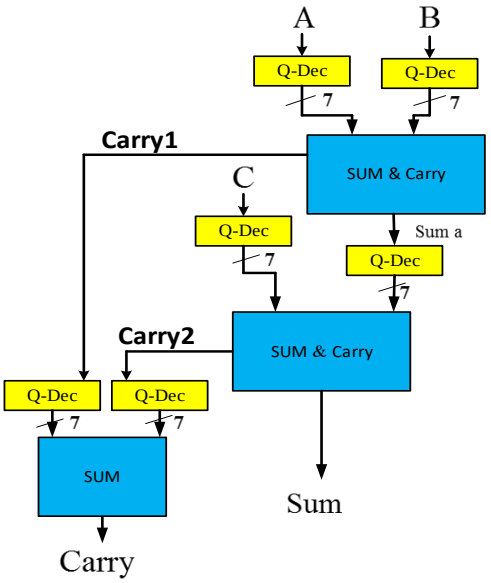


Fig. 2. The initial idea of the quaternary full-adder

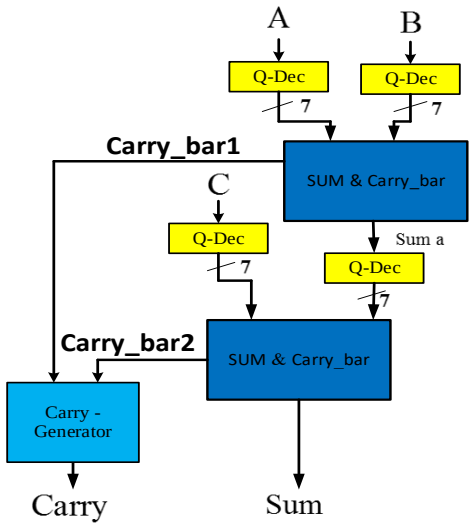


Fig. 3. The proposed optimized quaternary full-adder

To implement the full-adder, two inputs A and B can be added using one half-adder (depicted as SUM & Carry along with its Q-Decoders), and to add the third Cin input with the Sum output of the first half-adder, another half-adder can be used. Carry 1 and 2 related to both half-adders, as shown in Fig. 2, have the same digit weight and are applied to another half-adder to create the final carry digit of the full-adder. There is no need for a carry output for this half-adder because the sum of the carries will eventually be 2.

As previously noted, to implement a quaternary half-adder, a decoder gate, and a sum and carry generator circuit are used as shown in Fig. 2. The quaternary decoder takes one input and generates seven outputs, which will later be used to create a sum. The overall circuit design process is based on using the control signals provided by the decoder circuit output to control the keys that are actually needed to generate the sum and carry values. The basis of this design is adopted from the design procedure of the logic circuits using the CMOS transmission gate. In this regard, the sum and carry output look-up tables are considered to create the desired output values in the transmission paths.

The detailed explanations are provided in Subsections 2.3 and 2.4. The essential bottleneck with this type of design is that when 1 or 2 is needed at the output, the desired path must be designed from node VDD to the ground to supply the required voltage.

Fig. 3 depicts the proposed optimized quaternary full-adder, which has fewer devices.

Referring to Table 1, considering the input numbers in all states, it is clear that the half-adder's carry output does not interestingly have the values of 2 and 3 in any state. So, to reduce the design complexity, we create output 3 instead of generating 1 for caring output. This is due to the fact that the circuit needed to create output 3 is far simpler than the circuit needed to create outputs 1 or 2.

On the other hand, to generate the quaternary full-adder carry-out, the carry generator circuit uses two inputs, which have states 0 and 3. This approach for designing the circuit simplifies both the carry generator circuit of the half-adders and also the final carry generator circuit. With this proposal, two Q-decoders are eliminated, and the carry generator circuit is significantly simplified, so the number of transistors and the overall propagation delay of the full-adder will be reduced. In the following sections, the principle of the operation of the half-adder parts, namely the Q-decoder and sum and carry_bar, are explained, and their CNTFET level circuitry is provided.

B. Quaternary decoder structure

The four-level Quaternary Decoder (QDEC) decoder is shown in Fig. 4-a. It has one input and seven outputs with the corresponding input and output values shown in Table 1 [21]. After determining the logical input value, the appropriate transistor is selected based on Table 1, and the correct path is transmitted to the output. In Table 1, I is the input signal, I_x, and $\bar{I}_x$ are the decoder outputs where x ∈ (1, 2, 3, i). The required chiral vector and control signal connected to the gate of the transistors are given in Table 2.

The control signals which are created by a decoder, are applied to the transistors' gates.

TABLE 1 QDEC OUTPUT VALUE FOR DIFFERENT INPUTS

I	I_0	I_1	$\bar{I}_1$	I_i	$\bar{I}_2$	I_2	I_3	Number of transistors
0	3	0	3	3	3	0	3	18
1	0	3	0	3	3	0	0	
2	0	0	3	0	0	3	0	
3	0	0	3	0	3	0	0	

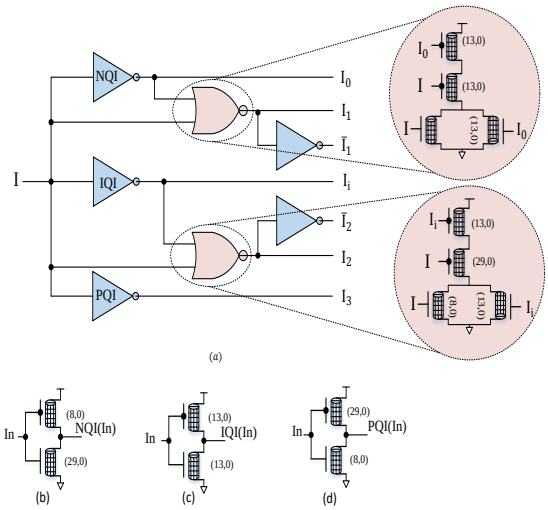


Fig. 4. a) QDEC - Quaternary Inverter; b) NQI c) IQI d) PQI [28]

Fig. 4 shows three types of four-level inverters called PQI (positive four-level standard), IQI (intermediate four-level standard), and NQI (negative four-level standard), which are described using Eq. 5.

$$NQI = \begin{cases} 3 & if \quad in = 0 \\ 0 & if \quad in \neq 0 \end{cases}$$

$$IQI = \begin{cases} 3 & if \quad in = 0 \; or \; 1 \\ 0 & if \quad in = 2 \; or \; 3 \end{cases} \tag{5}$$

$$PQI = \begin{cases} 3 & if \quad in \neq 3 \\ 0 & if \quad in = 3 \end{cases}$$

TABLE 2 THE LOOK-UP TABLE OF FOUR-LEVEL INVERTERS

IN	Out		
	NQI	IQI	PQI
0	3	3	3
1	0	3	3
2	0	0	3
3	0	0	0

C. *Half-adder's sum and inverse carry output*

First of all, let's briefly explain the Sum formula. According to Eq. 5, the four states that the sum output is 3, are when A=3, B=0, A=1, B =2, A=2, B=1 and A=0, B=3.

Note that when A=i (i = 0, 1, 2, 3), Ai is activated. In other words, it is equal to VDD, and all other signals are zero. For example, when A=0, the output A0 is active and A1, A2, and A3 are zero. With these explanations, the Sum output is equal to 2 when (A=0, B=2), (A=1, B=1), (A=2, B=0), and (A=3, B=3), so in Eq. 5, the second sentence must be written as $A_0B_2 + A_1B_1 + A_2B_0 + A_3B_3$ to create output 2. With these conditions, the third sentence also creates the Sum output of 1, and the first sentence creates the Sum output of 3. Note that in any circumstance, only one of the AiBi components is true (or equal to one).

$$\begin{aligned} \text{Sum} = 3(&A_0B_3 + A_1B_2 + A_2B_1 + A_3B_0) \\ &+ 2(A_0B_2 + A_1B_1 + A_2B_0 \\ &+ A_3B_3) \\ &+ 1(A_0B_1 + A_1B_0 + A_2B_3 \\ &+ A_3B_2) \end{aligned} \tag{6}$$

Since parallel transistors operate as OR and series transistors operate as AND, the Sum equation can be realized by transistors connected in series and parallels. As shown in Fig. 5, the half-adder sum output is controlled using QDEC outputs. Using Eq. 6, the Look Up Table of Sum output (Table 3) shows the values.

Table 3 shows the output SUM. For example, if the inputs (A and B) are equal to 2, that means that the output of the half-adder must be 6. If we show the number 6 in base three, the number will be 20, which means that the output SUM must be 2. The rest of the values in Table 3 can be obtained.

TABLE 3 LOOK-UP TABLE OF THE SUM OUTPUT OF HALF-ADDER

	B=0	B=1	B=2	B=3
A=0	0	1	2	3
A=1	1	2	3	0
A=2	2	3	0	1
A=3	3	0	1	2

Now, to fully describe the operation, the circuit of Fig. 5 can be used. Four-level logic is utilized with the voltages equal to 0, VDD/3, 2/3VDD, and VDD volt, which are the same as 0, 1, 2, or 3. Supposing that VDD equals 1 volt, the circuit equivalent to Fig. 6 can be used to create voltages of 0.3 and 0.6 volts. In the case of the output equal to 0.3 volts, keys K1 and K4 should be in the ON state, and keys K3 and K2 should be in the Off state. For the output to be equal to 0.6 volts, keys K2 and K3 should be the ON state, and keys K4 and K1 should be disconnected.

In order to design the sum circuit, the output should be logic 1 or 0.3 volts for (0,1), (1,0), (2,3), and (3,2) inputs. For example, in the case of half-adder inputs (2,3), the outputs (Sum, Carry) are 5 (Decimal); in this case, the value is Sum = '1' and the value Carry = '1'. In the circuit of Fig. 6, if K1 and K4 switches are turned on and K2 and K3 switches are turned off, the output of 0.3 volts or logic 1 is created. With this description, the output should be logic 2 or 0.6 volts for (0,2), (2,0), (1,1), and (3,3) inputs. In this situation, K3 and K1 switches are turned on, and K4 and K2 switches are turned off [30].

In the same way as the description of the sum 6, the inverse carry output (Cbar) can also be written as 6.

Note that the carry inverse is implemented to simplify the circuit design. In the reverse implementation of the carry (carry bar implementation), when the carry output is zero, we consider Cbar = 3 (or VDD), and when the carry output is one, we consider Cbar = 0.

According to Table 5, remember that in cases A=3, B=3 and A=3, B=1 and A=1, B=3 and A=2, B=2, the output of the carry output will be one; otherwise, it will be zero. With these explanations, the logical relation of the Cbar can be written as follows:

$$\text{Cbar} = 3\left(\left(\overline{A_1 B_1}\right) + (A_1 B_2) + (A_2 B_1) + \text{A} + \text{B}\right) \quad (7)$$

In this circuit, the NMOS transistor is used to transfer values 0 and 1, and the PMOS transistor is used for values 2 and 3. The value of their chiral vector is determined using the threshold voltage of each transistor. If we want to calculate the value of the chiral vector for these transistors using Eq. 2 and 3, the value is obtained as n = 7.

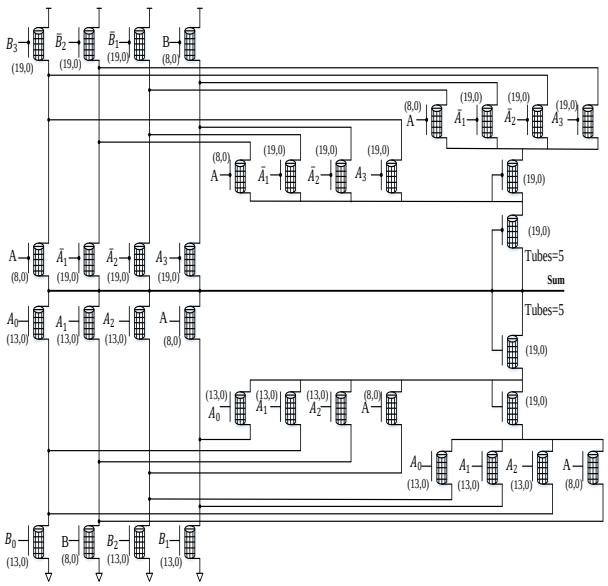


Fig. 5. The quaternary full-adder circuit's sum output realized at CNTFET transistor level [22]

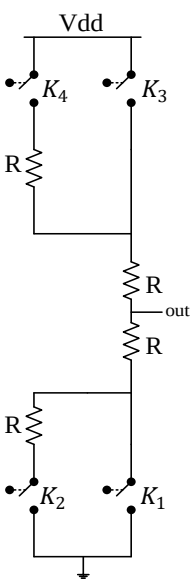


Fig. 6. The sum output equivalent circuit

The communication-aided adaptive protection methods [8, 9] and modified time-current curves for DOCRs [10] are some of the reported solutions to modify the MG protection system against changes in MG protection due to changes in system topologies. Since the adaptive scheme requires the hardware and software infrastructures to activate the suitable setting groups [11], a great deal of attention has also been paid to local measurement-based protection systems [12].

TABLE 4 THE LOOK-UP TABLE OF QUATERNARY SUM, FINAL CARRY, AND CBAR OF THE PROPOSED HALF-ADDER

Input values	Decimal Sum	Quaternary Sum	Carry_out	Cbar
0	0	0	0	3
(0,1) - (1,0)	1	1	0	3
(0,2) - (2,0)- (1-1)	2	2	0	3
(1,2) - (0,3) - (3,0)	3	3	0	3
(2,2) - (1,3) - (3,1)	4	0	1	0
(2,3) - (3,2)	5	1	1	0
(3,3)	6	2	1	0

The values in Table 4 are from 0 to 6 because, based on the quaternary logic's four-level values (i.e., 0, 1, 2, and 3), the maximum sum in the half-adder is 6. This is equal to 12 in the base four, in which digit 1 is carried, and digit 2 is the sum. Fig. 7 shows the transistor-level implementation of the Cbar.

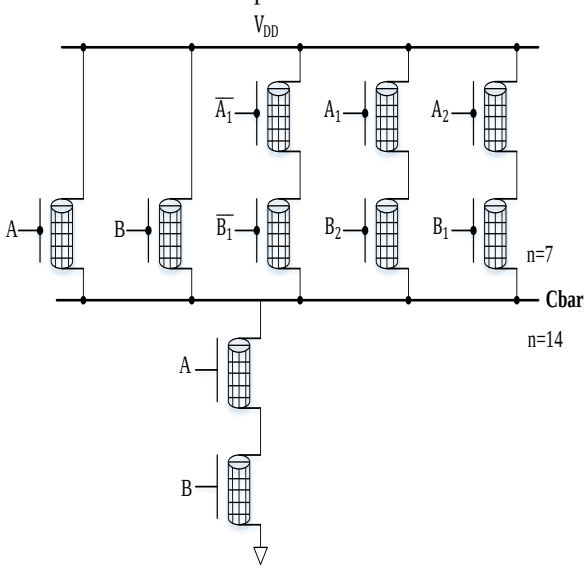


Fig. 7. Carry bar output implementation of the proposed half-adder

D. Final carry generator

Fig. 8 shows the transistor level of the full-adder final carry generator circuit. The carry output circuit consists of two inputs and one output. The inputs of this circuit are given using the reverse outputs of the carry output. In this circuit, the amplitude of the input signals will be zero (0) or VDD (3). Note that each input can be 0 or 3. In fact, the actual value of 3 is equivalent to

1 in the base of 4. Regarding the operation of this circuit, it can be said that this circuit calculates the sum of two inputs A and B.

According to Table 6, four states can occur for inputs A and B, and the carry creator circuit must be designed to operate according to Table 6. In order to realize the circuit, three different values 0, 1, and 2 must be generated at the output. If both inputs are 3, the output must be 0. For this purpose, two N-type series transistors are used. Note that zero-volt transmission is easily done with an N-type transistor. Two P-type series transistors are used to generate a value of 2 at the output when both inputs are zero. To transmit the value of 1 to the output when one of the inputs is 3 and the other is zero, two N-type series transistors and an inverter are used to invert the input with a value of zero. In fact, this inverter works like a binary inverter because inputs A and B have no more than two modes (0 and 3).

TABLE 5 THE LOOK-UP TABLE OF FINAL CARRY GENERATOR

inputs		output
B	A	Carry
0	0	2
0	3	1
3	0	1
3	3	0

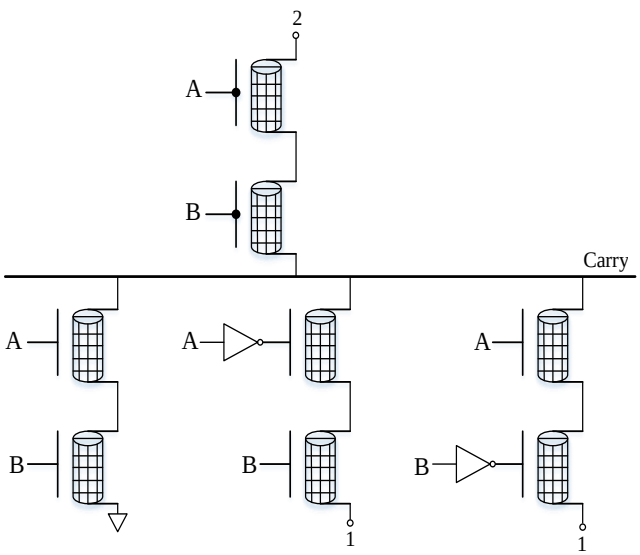


Fig. 8. The Carry generator transistor level circuit (n1=7, n2=0 for all of Transistor)

IV. Simulation results

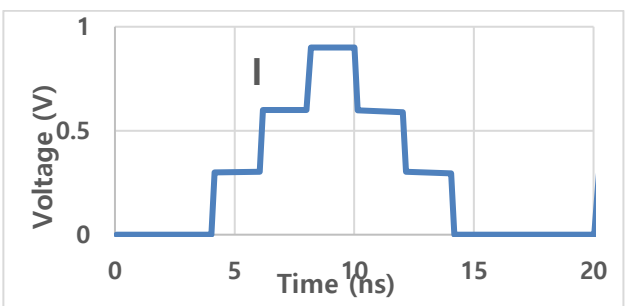
The proposed design was simulated using the Stanford 32 nm CNTFET library in HSPICE software [42-43]. The parameters of the CNTFET transistor and its values are shown in Table 6.

TABLE 6 THE PARAMETERS OF THE CNTFET TRANSISTOR

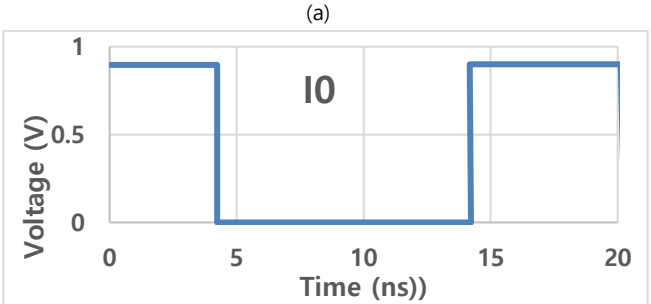
Parameters	Description	Value
$\mathbf{L_{ch}}$	Physical channel length	32 nm
$\mathbf{L_{ss}}$	The length of the doped CNT source extension region	32 nm
$\mathbf{L_{dd}}$	The length of the doped CNT drain extension region	32 nm
Lgeff	The mean-free-path in the intrinsic CNT channel	100 nm
Sub-pitch	The distance between the centers of two adjacent CNTs	4 nm
Kox	The dielectric constant of high-k top gate dielectric material (HfO_2)	16
Tox	The thickness of high-k top (planer) gate dielectric material (HfO_2	4 nm
$\mathbf{K_{sub}}$	The dielectric constant of the substrate	4
$\mathbf{C_{sub}}$	The Coupling capacitor between the channel area and the substrate	40 af/ µm
Efi	The fermi level of the doped source/drain tube	60 eV
Phi-M	The CNT work function	4.6 eV

The QDEC block is simulated by Hspice software. The timing diagram of the input and output signals of this block is shown in Fig. 9.

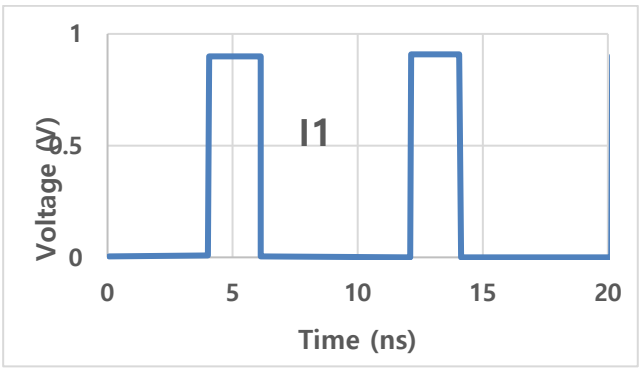
The proposed half-adder block consists of two circuits for creating Cbar and Sum, and the timing diagram of the input and output signals of this block is shown in Fig. 10. The simulation results show that this circuit consumes 1.3679 microwatts of power for proper operation, while the delay in the signal path is equal to 10 picoseconds. These results show that the PDP (Power Delay Product) index of this block is equal to 0.136 fJ.



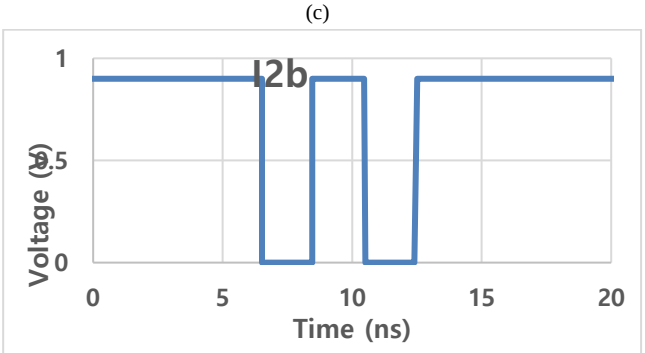
(a)



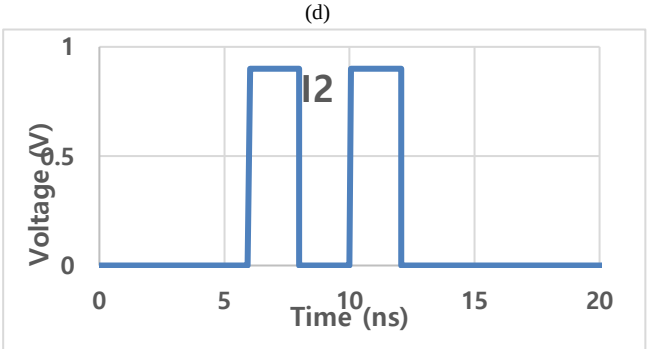
(b)



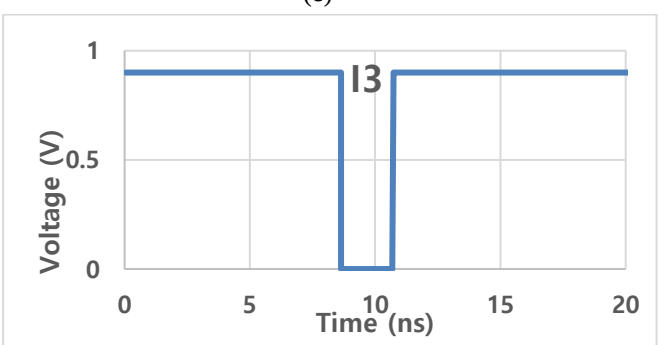
(c)



(d)

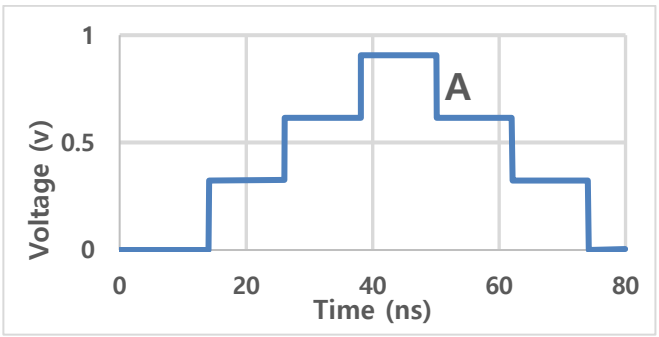


(e)

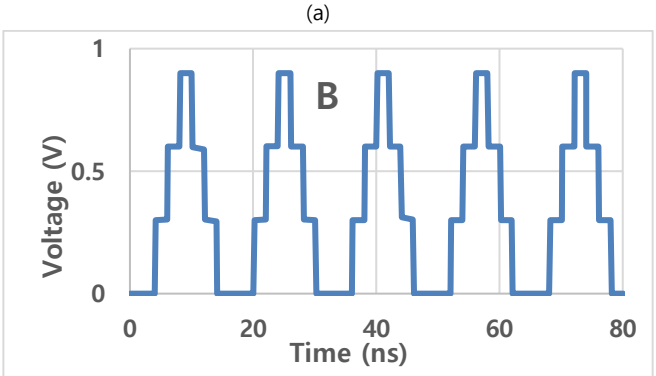


(f)

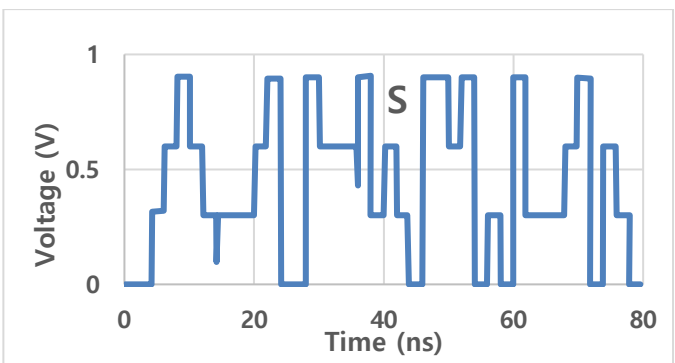
Fig. 9. The simulation result of QDEC- (a): I, (b): I0, (c): I1, (d): I2b, (e): I2, (f): I3



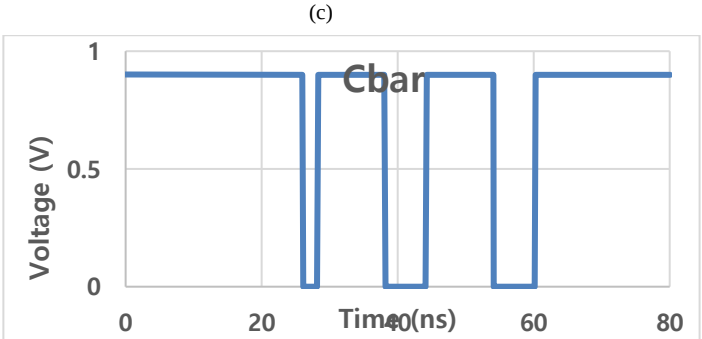
(a)



(b)



(c)



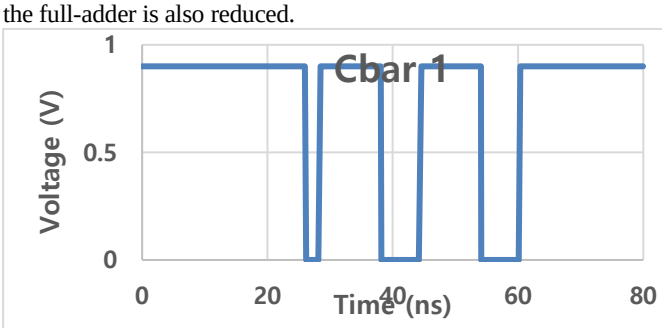
(d)

Fig. 10. The simulation results of the proposed half-adder-(a): A input, B Input, (c): Sum Output, (d): Car output.

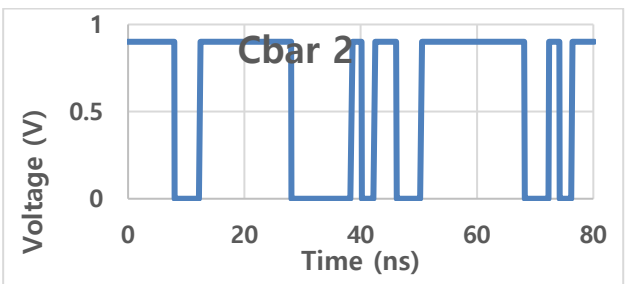
The time diagram of the input signals and the output signals of the carry generator block are shown in Fig. 11. The results show that the circuit operates correctly for all states. In Fig. 11, the Cbar1 and Cbar2 signals are the carry signals of the proposed half-adders.

The final performance of the proposed full-adder is correct in all possible states. The PDP index of the proposed full-adder is equal to 106 fJ.

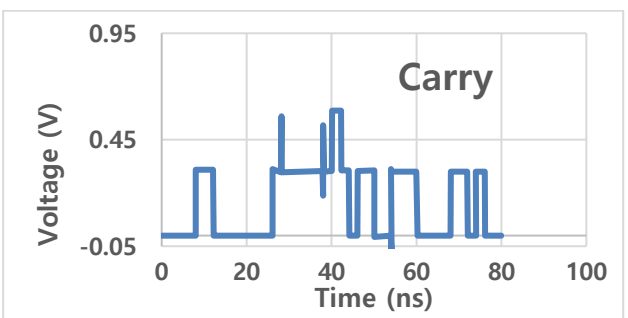
Table 7 shows the performance results of the proposed blocks in comparison with other works. It, indeed, compares the proposed four-level circuits and some three-level reports. There are several important points for a proper comparison of the design reports of the proposed circuits. In the processing circuits, the frequency and load capacitor of the circuits must be the same. Important parameters, including power consumption, propagation delay, and PDP coefficient, are reported in Table 7. Another important indicator of processing circuits is space consumption. For this type of comparison, valid outputs must be provided, and on the other hand, many conditions, including the load capacitor, must be considered. Finally, the results show that the proposed block is in better condition in terms of the energy index, while the space required to implement the final block of the full-adder is also reduced.



(a)

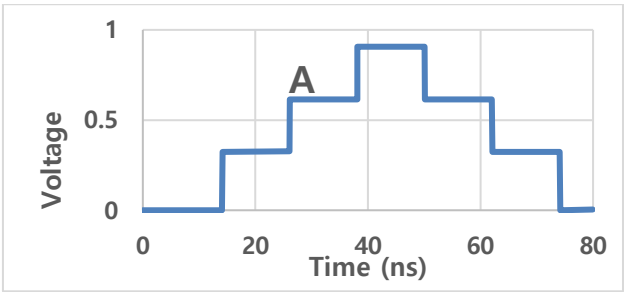


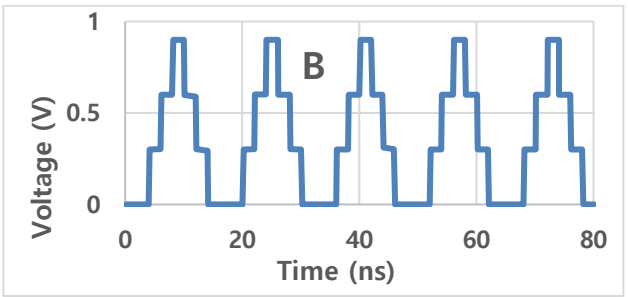
(b)

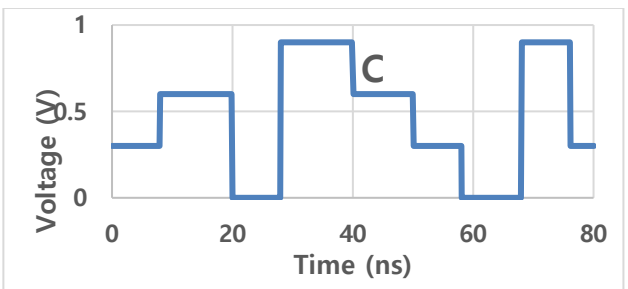


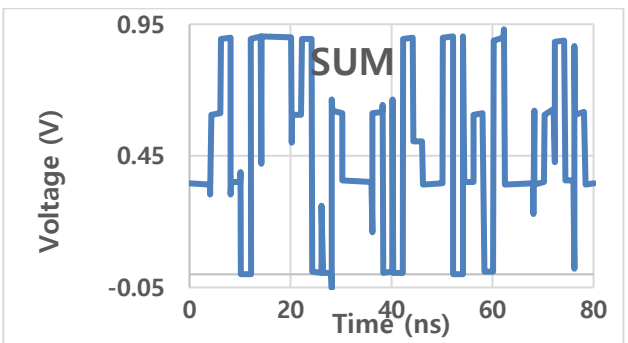
(c)

Fig. 11. The simulation results of the final carry generator-(a): Cbar1 output, (b): Cbar2 output, (c): Carry output.

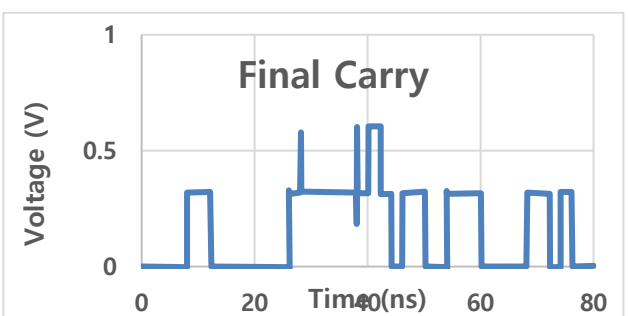








(a)



(b)

Fig. 12. The timing diagram of the proposed full-adder-(a): sum output (b): carry output.

V. Conclusion

Compared to binary circuits, MVL circuits have advantages and disadvantages. Binary processing circuits have a higher noise margin than MVL circuits. The reduction of connections between blocks and higher data density of multi-level circuits are the most important advantages of these circuits compared to processing circuits. In implementing quaternary circuits, it is complicated to produce levels 1 and 2 using transistors. In this article, the output of the Carry-out digit had two logical levels, and the approach adopted to implement the circuits was binary, which reduced the number of transistors and power consumption. The paper presented a quaternary full-adder structure consisting of two half-adders and a carry generator using a new structure. Using the techniques used to reduce the power and chip area in the design of this structure, the power and chip area of the proposed structure was finally optimized. To implement this structure, the four-level to binary conversion technique was used to implement the carry output circuit. The simulation results showed that the PDP of all the proposed full-adder was 10.68 aJ.

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