

A Technical Review on the Proper Design of Gate Drivers in Industrial Power Electronics Applications

Saeid Ahmadi¹ | Kourosh Khalaj Monfared¹ | Mohammad Khalilzadeh² | Hossein Imanini¹

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran, Iran¹

Research Assistant at University of Tarbiat Modarres, Iran²

Corresponding author's email: kourosh.khalaj@ut.ac.ir

Article Info	ABSTRACT
<p>Article type: Review Articles</p> <p>Article history: Received: 7-Dec-2023 Received in revised form: 10-Feb-2023 Accepted: 20-April2024 Published online: 21-June-2024</p> <p>Keywords: Power Semiconductor Devices, Gate Drive Circuit, IGBT Gate Drive, Desat Protection.</p>	<p>Power semiconductor devices are the most important components in power electronics applications. They are also the most fragile components of electronic circuits. A power semiconductor device's switching performance and protection depend on the gate drive circuit specifications. Therefore, choosing an appropriate gate-driver and designing its corresponding circuits is necessary. This paper is a technical review of the proper design of gate drivers for silicon power switches (like Si IGBT and Si MOSFET) in industrial power electronics applications. In this paper first conducts an overview of the main specifications of gate drivers for industrial power electronics applications. Then, concerning the protective role that a gate-driver can provide, crucial points of an effective design are discussed. Finally, a circuit is proposed to test the gate driver's short-circuit protection. The circuit is experimentally evaluated for three gate drives, and the results are discussed. A practical comparison of the protection performance of commercial gate drives ACPL-330J, ACPL331, and PC929 is also conducted.</p>

I. INTRODUCTION

In the present era, power electronic components have become pervasive across many applications, spanning motor drives, switching power supplies, renewable energy systems, flexible AC transmission systems (FACTS), and more. The reliability of these components has become a focal point of concern. A key element within these systems is the power semiconductor device (PSD), encompassing many devices such as Thyristors, MOSFETs, IGBTs, GaN-based switches, and SiC switches [1]. Proper driving techniques for these devices are paramount, as the failure of even a single component could lead to a systemic operational breakdown [2]. Various protection strategies for PSDs have been proposed in the existing literature. Notably, due to the fast operation of

GaN and SiC PSDs, protection methodologies for these PSDs exhibit distinctions from those tailored for Si-based PSDs such as IGBTs and conventional MOSFETs. Comprehensive insights into these variances can be found in scholarly works [3],[4]. Given the prevalence of commercially available power electronic devices reliant on conventional Si-based PSDs, this study focuses primarily on them.

There are several gate drives for different PSDs. Gate drives are generally divided into two categories: isolated and non-isolated. In isolated gate drivers, the input command is isolated from the power. The common mode and noise transmission rejection capability are the most important advantages of isolated gate drivers. On the downside, they are more expensive than non-isolated ones [5]. The Bootstrap method is widely used among the non-isolated methods [6].

TABLE I. COMPARISON OF IGBT PROTECTION METHODS

Measurement Method	Implementation	Feature
V_{ce} Voltage	Requirement of a high voltage diode and simple sampling circuit	The best method with fewer additional circuits and more straightforward implementation (proper for gate drive ICs)
Gate voltage and current	Requirement of special sampling circuits of gate voltage and current and low voltage logic circuit	Due to the low gate current, special measuring circuits are needed, and the possibility of functional error is also high.
I_c Current	Requirement of high-cost power circuit current measurement	The cost of implementing the method is high, increasing the losses in the power section.
Changing the gate current	Requirement of special and expensive current measurement circuit	It requires special and complex measurement circuits and imposes costs and losses to the system.

Bootstrap configurations utilize the voltage across the low-side switch to generate a floating supply voltage for driving the high-side switch. This approach eliminates the need for a separate isolated power supply for the high-side driver, simplifying the overall circuit design and reducing component count and cost. However, this method is limited in high-power applications due to the problem of electromagnetic interference (EMI), and there is interest in using isolated gate drives. A suitable gate driver for the PSD should offer various functionalities. Among these, isolation and safeguarding the switch during short-circuit (SC) scenarios are crucial features. Additionally, essential attributes comprise under-voltage lockout (UVLO), the soft turn-off for the PSD during SC occurrences, high common-mode rejection, etc [7]. Numerous gate drive products in the market incorporate these functionalities, and selecting a specific gate drive type is contingent upon the application.

This paper presents a detailed review of the specifications of proper gate driver ICs for PSDs. In addition, the precise design of SC protection is studied, and a test circuit for evaluating the designed circuit is proposed. By using the proposed circuit, the correct protection functioning can be validated for every gate driver ICs. For instance, the protection circuits for three gate drivers are developed and assessed experimentally using the suggested circuit. The paper aims to enhance power electronic circuit designers' comprehension of the protective attributes of gate drivers for MOSFET and IGBT power switches. It also aims to aid them in creating and testing SC protection strategies to mitigate the potential system failure risks in safety-critical applications like motor drives.

II. DESIRABLE GATE DRIVE SPECIFICATIONS

This section presents some of the desired specifications of the IGBT/MOSFET PSD gate drivers. A gate drive may have some of the following specifications.

A. Electrical isolation

One essential requirement of the IEC 61800-5-1 standard is to ensure electrical isolation between the control and power

sections, as outlined in references [8] and [9]. This practice enhances operational efficiency, safeguards electronic components against malfunctions, and enhances system reliability. The gate drive circuit addresses the electrical isolation challenge, separating the power and control sections. As a result, isolated gate drives have a higher priority in industrial power electronics applications [10].

B. Protections

IGBT protection (voltage and current) is important in power electronic converters. Managing voltage and current overshoot during hard switching processes and SC condition has historically relied on passive methods like fine-tuning gate resistor values and incorporating clamping circuits. However, recent advancements have led to more refined and efficient methodologies, predominantly through advanced gate drivers. This progression signifies a significant move towards enhancing the reliability of IGBT systems without incurring additional costs, capitalizing on the inherent capabilities of modern gate drivers. These advancements in gate driver technology have paved the way for various innovative techniques to enhance IGBT drive reliability [11]. Based on sampling schemes of IGBT current or voltage, cutting-edge protection mechanisms can be classified into distinct approaches: (1) the IGBT collector-emitter voltage-based (VCE) strategy [12], (2) gate sampling-based strategy [13], (3) the IGBT collector current-based strategy [14], and (4) the IGBT collector current rate of change (di/dt) strategy [15]. To facilitate a comprehensive comparison of these methodologies, Table I thoroughly analyzes the approaches above. Each of these approaches offers unique benefits and trade-offs in optimizing the performance and stability of power electronic systems. This paper focuses on the VCE monitoring method because it is a standard method for commercial gate drives. Therefore, an important feature of a gate driver is the ability to protect the PSDs. Based on the type of protection, three important PSD protections are defined: SC protection (with VCE monitoring), protection of switches against dropping the voltage supply of gate below the operational value (under-voltage lockout capability (UVLO)), and soft turn-off capability in SC events [16].

1) Short circuit protection

Protection of IGBT/MOSFET during overcurrent conditions is a critical part of system reliability, both in terms of asset destruction and safety. PSDs such as IGBTs are not regarded as a fail-safe component, and their failure can result in a DC bus capacitor explosion, and complete power electronic system failure. SC protection in industrial gate drives is typically implemented based on desaturation (DESAT) detection (or VCE monitoring) [17], [18].

2) Undervoltage lockout (UVLO)

UVLO is a key feature that protects the system against bias supply failure. In isolated gate driver ICs, the voltage supply is provided at both the primary and secondary sides of the IC. The UVLO setting on the secondary side determines the minimum acceptable drive voltage for the PSD.

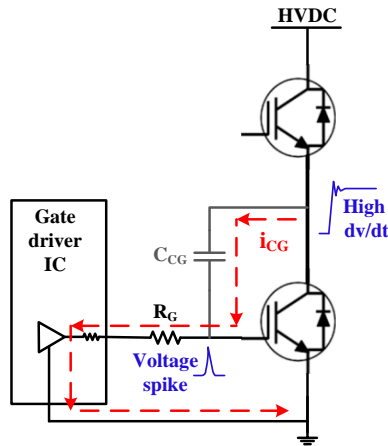


Fig. 1. Active miller effect.

By implementing UVLO in gate drivers, the gate voltage is monitored and prevented from dropping below a specified threshold. The UVLO rating is a determinant factor in high-power applications such as onboard chargers, EV traction inverters, and solar inverters [19]. Differing drive voltage requirements in these PSDs require different UVLO thresholds [20]. If the gate drives do not have UVLO capability, and if the gate supply voltage drops, the power switch will enter its linear region and cause a lot of losses, which can lead to irreparable damage.

3) Soft turn-off

Another important feature of industrial gate drivers is the soft turn-off of the switch in SC conditions. The soft-turn-off method protects the power switch in SC conditions. When the power switch is SC, the current increases to substantial values momentarily. Suppose the power switch is turned off at a high speed (as in normal conditions). In that case, it leads to a very large di/dt , and due to parasitic inductance in the path of the power switches, it leads to considerable voltage spikes that can damage the switch.

Therefore, turning off the switch slower than normal is necessary to avoid voltage spikes (VSPIKE). By implementing soft turn-off, can achieve smoother transitions during switching, reducing electromagnetic interference and enhancing the power electronic system's reliability during SC conditions [21]. The soft turn-off methods are very effective compared to the snubber circuits. This is because slow turn-off is employed only during overcurrent turn-off situations and does not affect the system's performance under normal operating conditions. This feature is achievable without the high cost and increasing the system's size. It increases the system's reliability and effectively achieves cost, performance, and reliability trade-offs [22].

4) Two-level turn-off

The two-level turn-off is another method to prevent the Collector-Emitter/Drain-Source voltage's sudden rise due to the switch turn-off, especially in SC protection conditions [23]. The two-level turn-off introduces a second turn-off voltage level at the gate-driver output between ON and OFF levels. This additional level ensures lower switch voltage overshoots

at turn-off by reducing gate-emitter/source voltage at SC or over-current (OC) conditions.

C. Common-mode rejection

The common-mode (CM) noise is created in power electronic circuits due to switching action and creating dv/dt . This CM noise can be coupled to different parts of the circuit due to the parasitic capacitance in the circuit. Isolated gate drives that isolate the power and control sections have an important specification called CM transient immunity (CMTI). CMTI is defined as the quantification of CM rejection. CMTI criterion shows that the isolation is maintained up to the permissible CM level (dv/dt), and the noise of the power section is not coupled to the control. [24]. For example, if the DC bus is 1500V and the transition time of the gate-driver IC output signal is 100ns, the CMTI required by the IC is 15 V/ns. The gate drivers are specified for CMTI in their datasheet. For example, the ISO5851 and ISO5852S both have a minimum CMTI of 100 kV/ μ s. The higher CMTI for the IC is, the lower the false fault or the false output toggle due to the transient noise is ensured.

D. Gate Current Supply Capability

The IGBT/MOSFET switching time is controlled by charging and discharging its gate. The rise and fall times of the gate drive to the IGBT can be selectively controlled by selecting R_G (on) and R_G (off). When turned on, all current will flow from the IC through R_G (on) and charge the IGBT gate capacitance, so increasing or decreasing R_G (on) will increase or decrease the rise time in the application. With the addition of diode DR_g, the fall time can be controlled independently because the turn-off current flows from the IGBT gate capacitance through R_G (off) and DR_g to the driver in the IC to GND. An increased gate peak current reduces switching losses by decreasing the turn-on and turn-off times. The gate resistors R_G (on) and R_G (off) can control the gate charge currents (Fig. 4). The theoretical gate peak current value can be calculated by:

$$i_{G,Peak} = \frac{V_{G(on)} - V_{G(off)}}{R_G + R_{G(int)}} \quad (1)$$

where V_G (on) and V_G (off) are the gate's turn-on and turn-off supply voltage, respectively. Also, R_G is an external gate resistor. The IGBT module's internal gate resistor R_G (int) must be taken into account when calculating the peak gate current. In practice, stray inductance reduces the peak value below the possible theoretical value [25].

E. Other features

There are also some additional features that some gate drives may provide. They are introduced as follows.

1) Dead-time generation

In normal operation, two switches of a phase-leg of an inverter will be turned on and off one after the other. The simultaneous conduction of both switches results in a rise of current limited only by DC-link stray inductance and the switches' on-resistances.

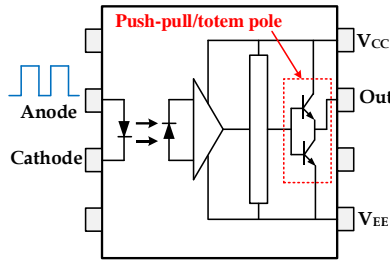


Fig. 2. Output stage with push-pull (or so-called totem-pole) structure.

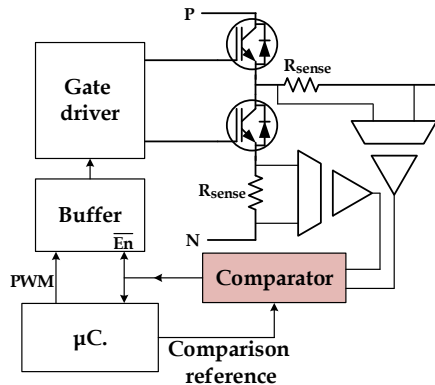


Fig. 3. Hardware-based SC protection circuit.

Although the switches would not be turned on at the same time intentionally, since they are not ideal switches, turn-on and turn-off times are not strictly identical. Adding a “dead time” into the control scheme is necessary to avoid shoot-through. With this additional time, one switch will always be turned off first, and the other will be turned on after the expired dead time. Hence, shoot-through can be avoided. The dead-time is typically generated in two ways; through the software or hardware. In the software-based method, the dead time is created to generate the PWM switching signal process based on the selected microcontroller. On the other hand, hardware-based methods use additional circuit elements to generate dead-time. In the case of hardware implementation, one solution is designing analog circuits [26]. Another solution is using special gate-driver ICs with built-in dead time generation. These ICs are more reliable and easy to implement than user-designed analog circuits. Some commercial examples are IR2104, IR21844, IR2110, etc.

2) Integrated Flyback controller

One of the interesting features of some gate-driver ICs is the integrated Flyback controller for isolated DC-DC converter.

Besides, these ICs contain a built-in MOSFET switch for the Flyback. An external transformer has to be connected to complete the Flyback circuit. This feature is beneficial in omitting an external isolated power supply for the gate driver's secondary side, resulting in a cost-effective design. One of the most famous commercial examples is the ACPL-302J gate drive.

3) Active Miller clamp

Parasitic turn-on due to the Miller capacitor is a common problem when operating an IGBT [27]. This effect is remarkable in 0 to +15 V type gate drivers (single supply driver). Due to the gate-collector coupling through the Miller capacitor, a high dv/dt transient created during IGBT turn-off can induce parasitic turn-on (gate voltage spike), which is potentially problematic. Fig.1 shows this phenomenon schematically.

When turning on the upper IGBT in a half-bridge, a voltage change dv_{CE}/dt occurs across the lower IGBT. A current flows through the parasitic Miller capacitor C_{CG} , the gate resistor R_G , and the internal gate resistor. This current can be approximated by (2) and (3).

$$i_{CG} = C_{CG} \frac{dv_{CE}}{dt} \quad (2)$$

$$V_{CG} = i_{CG} R_G \quad (3)$$

The current creates a voltage drop across R_G . An unwanted parasitic turn-on occurs if this voltage exceeds the IGBT gate threshold voltage. It should be noted that rising IGBT chip temperature would slightly reduce the gate threshold voltage. This parasitic turn-on can also be seen on the upper switch when the lower one is turned on.

III. STANDARD METHODS FOR PSD DRIVING

Various PSDs have been used in power electronic applications. One of them is the IGBT, which has found many applications in the industry. This section focuses on IGBT driving. There are various commercial methods to drive the gate of an IGBT [28]. Using a pulse-transformer is one of these methods, which provides isolation, as previously mentioned in section II. This is a simple and inexpensive method. However, pulse-transformers are more challenging to design than optically based isolation methods. When dealing with pulse transformers, the load becomes more critical than any other type of transformer. Leakage and primary inductance values have added significance because of their effect on the output wave shape [29]. If the load disturbs this wave shape, severe problems may occur. Also, this method cannot achieve a high and safe isolation level. It also does not provide SC protection. Meanwhile, a more advanced method is to exploit gate driver ICs to overcome the pulse-transformer drawbacks and provide most of the added benefits mentioned in the previous sections.

From the protective function point of view, commercial gate drives are divided into two main categories: 1) isolated gate drives without SC protection and 2) isolated gate drives with SC protection.

A. Isolated gate-drives without SC protection

Gate drives of this category provide galvanic isolation between the control and power sections, as shown in Fig.2. They usually have a push-pull (or so-called totem-pole) structure to supply the required sink and source current of the gate of the PSD. A gate driver sinks and sources current, meaning the driver can draw current from and supply current to the semiconductor device's gate terminal. The gate's sink and source current is proportional to PSD's switching speed. Some commercial examples are TLP250, TLP350, IX3180, HCPL-3120, HCPL-3150, etc. As shown in Fig.2, this type of IC has no protection against SC conditions. Therefore, the user should design an external SC protection circuit. One method is detecting the SC current, generating an error signal, and softly turning off the switch.

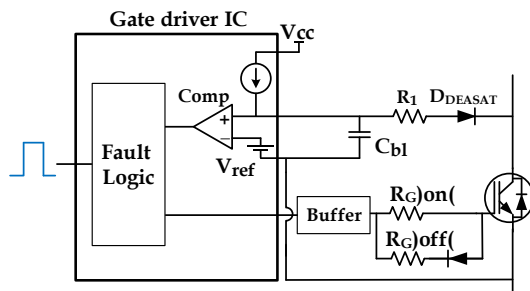


Fig. 4. DESAT circuit integrated with industrial gate drives ICs.

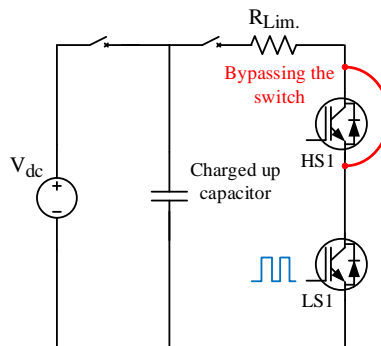


Fig. 5. Designed board for SC test condition.

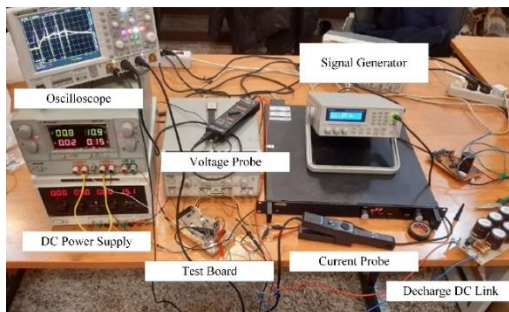


Fig. 6. Experimental setup.

The protection is provided by sending an error signal to the microcontroller and the shutdown command back via the microcontroller. Although the protection of the switch is not guaranteed due to the inherent delay in the method, it can protect the circuit.

A more effective protection strategy is to use hardware directly to detect SC and shut down the switch instead of using the software. This method has a small delay in protecting the switch if designed correctly. An example circuit is shown in Fig.3. As can be seen, the switch current is measured through the shunt resistors. After comparison with a threshold, if an SC is detected, the switch turn-off command is sent from the comparator, and then PWM is deactivated, resulting in the switch protection.

B. Isolated gate-drives with SC protection

In addition to isolation, some commercial gate drivers possess integrated circuits that are used to detect SC and protect switches. The most common method is monitoring the IGBT collector-emitter (VCE) voltage (or drain-source voltage, VDS, in MOSFET). This method is known as desaturation (DESAT) Protection. The VCE (or VDS) is proportional to the current flowing through the collector (IC) of the IGBT or drain (ID) of a MOSFET. The characteristic curve of VCE-IC or VDS-ID is given in the switch datasheets. These gate drivers monitor the VCE (or VDS) and compare it with an internal reference voltage. Once a SC is detected, which is an overvoltage of VCE (or VDS) concerning the reference voltage, the turn-off command is sent to the switch by the driver IC. Then, the switch is softly turned off, and the current is cut off through a mechanism described in section II. The design engineer's responsibility is to make reasonable adjustments to the SC detection threshold. An example of DESAT circuit integrated with industrial gate drives ICs is shown in Fig. 4. Some commercial example gate driver ICs of this category are HCPL316, ACPL-330J, ACPL331, ACPL336, FOD8316, etc. They have a 200 ~ 300 μ A internal current source to charge the capacitor Cb1 to a voltage of VCE-VDESAT linearly. The capacitor voltage is continually compared with the internal Vref (usually 6.5V). The designer can adjust the circuit threshold for different switches by setting the VDESAT (using a Zener diode or several series diodes). According to Fig.4, resistor R1 and capacitor Cb1 filter out noises coming from the power switch side. The filter transfer function is expressed as (4).

$$V_{DESATF} = \frac{1}{1 + R_1 C_b s} V_{DESAT} \quad (4)$$

where V_{DESATF} is the filtered value of voltage V_{DESAT} .

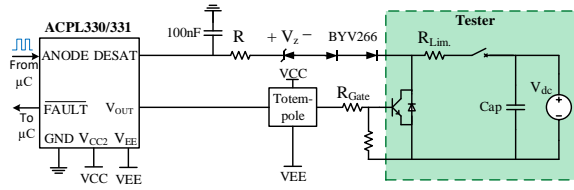


Fig. 7. Schematic of ACPL-330J and ACPL331 gate drive circuit

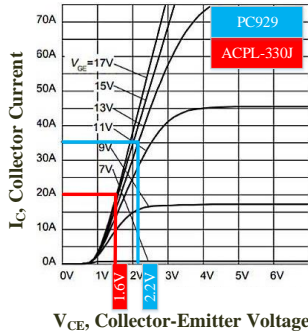


Fig. 8. V_{CE} - I_{CE} characteristic of IKW25T120 IGBT.

IV. DESIGN EXAMPLES AND THE PROPOSED TEST CIRCUIT

In this section, some commercial gate drives, including ACPL330J, ACPL331, and PC929, have been experimentally evaluated for further investigation. A general test circuit is proposed to determine if the designed SC protection can detect SC and shut down the switch correctly. The designed board for SC test condition, is shown in Fig. 5. In this board, the gate drive of high side PSD is the ACPL-330J, and the low side is ACPL-331J. On another similar board, the gate drive of PSD is PC929. The PSDs is an IGBT 1200V, 25A (IKW25T12). Two power supplies supply the gate driver (+15V and -9V). A signal generator is used to generate the switching commands for IGBT. To test each gate drive, SC has another IGBT, and with the gate command, the IGBT of the gate drive under test is placed in an SC condition (by discharging the charged capacitor). The amount of SC current as (5) can be adjusted through the series resistance (R_{Lim}) and the voltage of the charged capacitor (V_{dc}).

$$I_{Lim} \approx \frac{V_{dc}}{R_{Lim}} \quad (5)$$

The SC tests are performed on the experimental system. The DC link uses a capacitive bank connected to the power

supply via a relay. This capacitive bank discharges current into the IGBT, providing an intentional SC situation. The experimental test bench is shown in Fig. 6.

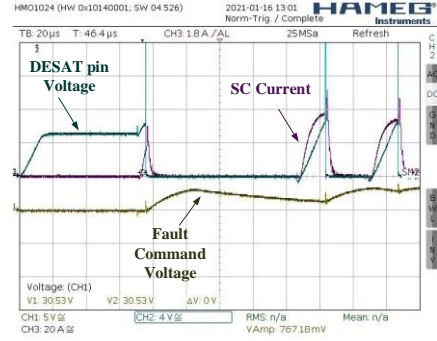


Fig. 9. ACPL-330J gate drive SC test.

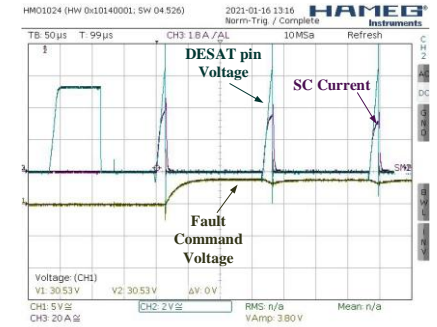


Fig. 10. ACPL-331J gate drive SC test.

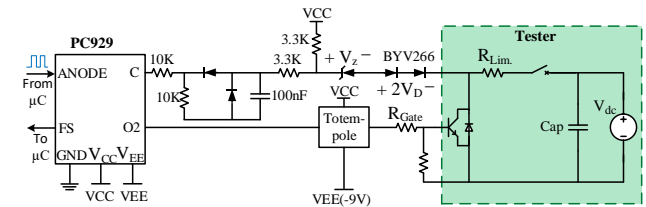


Fig. 11. Schematic of PC929 gate drive circuit

A. ACPL-330J gate drive analysis

ACPL-330J is used in the proposed test circuit, according to Fig. 7, to check its performance. DC link is charged, and the IGBT is commanded to start conduction, resulting in an SC condition. The gate drive must protect IGBT. In the designed circuit, the value of the Zener in the DESAT pin is set to 4.7V. According to Fig. 7 with a KVL in DESAT pin, (6) is obtained.

$$V_{DESAT,Fault} = R \times I_{CHG} + V_Z + 2 \times V_D + V_{CE} \\ 6.5V = 100\Omega \times 250\mu A + 4.7V + 2 \times 0.1V + V_{CE} \quad (6)$$

$$V_{CE} = 1.6V$$

where $V_{DESAT,Fault}$, and I_{CHG} are internal fault reference voltages of IC and internal current sources. Also,

V_z and V_D are Zener and diode voltages. According to the IKW25T12 IGBT (VCE-IC) curve (Fig.8), at about 20A to 30A, the IGBT must be turned off by the ACPL-330J. As shown in Fig.9, the current (purple waveform) is limited to around 30A when a short circuit occurs. In addition, the DESAT pin voltage (green waveform) is reached around 6.5V, and protection is activated.

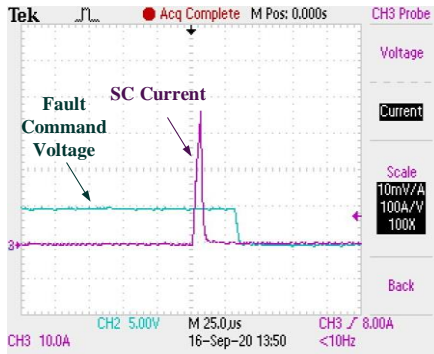


Fig. 12. PC929 gate drive SC test.

Table II. COMPARISON TABLES OF ACPL330, ACPL331, AND PC929 GATE DRIVES

Gate Driver	Desat Protection	Reset Type	Fault Command	Dependency of Protection on Voltage Supply
ACPL330	Yes	Automatic Reset After 25 μ s	Isolated	No
ACPL331	Yes	Automatic Reset After First Pulse	Isolated	No
PC929	Yes	Automatic Reset After First Pulse	Isolated	Yes

The fault command (yellow waveform) also goes high and signals the SC conditions to the microcontroller. For ACPL-330J, the driver will automatically reset the FAULT pin after a fixed mute time of 25 μ s (typical). As a result, the SC conditions are repeated if the fault is not cleared during this mute time, as shown in Fig. 9.

In the first pulse, the applied SC fault is interrupted and then re-applied. In the last two pulses of Fig. 9, the SC fault (connected charged capacitor) remains on the system, and as it is clear, after 25 μ s, the current increases again.

B. ACPL-331J gate drive analysis

An intentional SC condition is created by replacing ACPL-331J gate drive IC in the proposed circuit, charging the DC link, and connecting the IGBT. The gate drive must protect IGBT. Zener setting in the DESAT pin is similar to one mentioned for the ACPL-330J. Similarly, as shown in Fig.10, the current (purple waveform) is limited to about 30A. Also, the DESAT pin voltage (green waveform) reaches about 6.5V, and protection is activated. The fault command (yellow waveform) also goes to a high level and indicates the SC conditions of the microcontroller. The next

turn-on command can reset the fault mechanism after 5 μ s (minimum) mute time. As a result, the SC conditions are repeated if the fault is not cleared during the mute time between two turn-on commands, as shown in Fig. 10.

C. PC929 gate drive analysis

The structure of the test PC929 circuit is shown in Fig. 11. According to the PC929 datasheet, reaching the voltage of pin 9 to about V_{cc} -6V means an SC condition has happened, and the protection system operates. After the SC condition is detected, pin 8 (F_s) goes to low-level voltage (0V), and thus, the error is sent to the microcontroller. According to Fig.11, in the PC929 circuit, two diodes and a 6.5V zener are used. Also, the PC929 operates with a V_{cc} =25V, which, according to (4), the protection voltage is calculated as (7).

$$V_{cc} - 6V = V_Z + 2 \times V_D + V_{CE} - V_{Gate-negative} \quad (7)$$

$$\rightarrow 25 - 6 = 65 + 2 \times 0.6 + V_{CE} + 9 \rightarrow V_{CE} = 2.2V$$

According to the IKW25T12 IGBT (VCE-IC) curve (Fig.8), the current of V_{CE} =2.2V is about 40A. Therefore, the IGBT must be turned off by the PC929 at about 40A. As shown in Fig.12, the current (purple waveform) is limited to about 40A. Also, the fault command (blue waveform) goes to a low level, indicating the short-circuit conditions of the microcontroller.

D. Dependence on supply voltage

Unlike ACPL-330J and ACPL-331J, PC929 gate drive SC protection level depends on the supply voltage (V_{cc}), which is a disadvantage.

In industrial power electronic circuits, the gate drive power supply may have a 10% tolerance, which can negatively affect the protection performance of PC929.

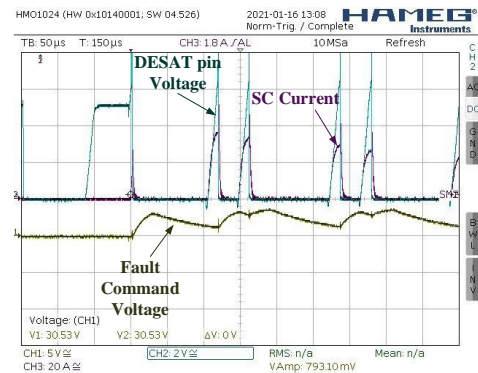


Fig. 13. SC test with 13.1V power supply for ACPL-330J.

TABLE III. COMPARISON OF THE SPECIFICATIONS OF THE MOST WIDELY USED INDUSTRIAL GATE DRIVES

Gate Drive	Peak Current	DESAT	UVLO	Reset Type
FOD8316	2.5A	Yes	Yes	Reset Pin
ACPL330	1.5A	Yes	Yes	Automatic Reset After 25us
ACPL331	1.5A	Yes	Yes	Automatic Reset After First Pulse
ACPL336	2.5A	Yes	Yes	Automatic Reset After First Pulse
HCPL316	2.5A	Yes	Yes	Reset Pin
PC929	0.4A	Yes	No	Automatic Reset After First Pulse
MC33153	1A	Yes	Yes	Automatic Reset After First Pulse
TD350	1.5A	Yes	Yes	Automatic Reset After First Pulse
2ED020H12	2A	No	Yes	-
Gate Drive	Fault Command	Isolation	Dependency of Protection on Supply	Price
FOD8316	Isolated	Yes	No	4\$
ACPL330	Isolated	Yes	No	6\$
ACPL331	Isolated	Yes	No	5.3\$
ACPL336	Isolated	Yes	No	6\$
HCPL316	Isolated	Yes	No	5.5\$
PC929	Isolated	Yes	Yes	3.1\$
MC33153	Non-Isolated	No	No	1.3\$
TD350	Non-Isolated	No	No	2.2\$

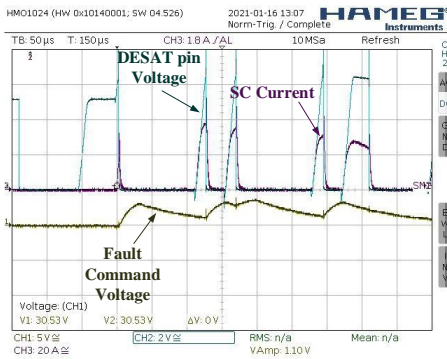


Fig. 14. SC test with 17.5V power supply for ACPL-330J.

To check the dependency of SC protection of ACPL-330J and ACPL-331J to supply voltage (V_{cc}), the voltage is set once to 13.1V and again to 17.5V. The SC protection operation is investigated. It is seen from Fig. 13 and Fig. 14, SC protection in ACPL-330J functions well independently from the supply. For a quick comparison, Table II summarizes the important characteristics of the compared gate drives (ACPL330, ACPL331, and PC929).

E. Comparing the important characteristics of widely used industrial gate drivers

This section provides a qualitative comparison based on widely used industrial gate drivers. Table III presents from the point of view of gate drive power, protection specifications (DESAT protection, UVLO protection, reset type, and fault command), isolation, and price. This comparison allows users to choose based on their desired application.

V. Conclusions

This paper presents a comprehensive overview of the

industrial specifications of gate drives. This paper focuses on the gate drive of silicone power switches (Si IGBT and MOSFET). One of the important features of IGBT and MOSFET gate drives is short circuit protection. Gate drives with SC protection capability are prioritized more in industrial applications than in ordinary ones. As design examples, three commercial gate drive ICs are considered. A test circuit is proposed for experimentally evaluating SC protection's proper design and functioning. The dependency of the protection on the supply voltage of the ICs is also investigated. This dependency is a significant disadvantage for a gate drive. It may result in the malfunctioning of the SC protection and system failure due to a small supply voltage variation. As a result of the comparison between the three ICs, ACPL-330J and ACPL331 are better choices than PC929 for power electronic applications.

REFERENCES

- [1] Disney, Don, and Z. John Shen. "Review of silicon power semiconductor technologies for power supply on chip and power supply in package applications." *IEEE Transactions on Power Electronics* 28.9 (2013): 4168-4181.
- [2] Hernes, Magnar, et al. "Failure analysis and lifetime assessment of IGBT power modules at low temperature stress cycles." *IET Power Electronics* 14.7 (2021): 1271-1283.
- [3] Mocevic, Slavko, et al. "Comparison and discussion on shortcircuit protections for silicon-carbide MOSFET modules: Desaturation versus Rogowski switch-current sensor." *IEEE Transactions on Industry Applications* 56.3 (2020): 2880-2893.
- [4] Min, Sung-Soo, and Rae-Young Kim. "Improved gate-voltage-driven desaturation short-circuit protection circuit with robust switching noise immunity for WBG power semiconductors." *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2022).
- [5] Phukan, Ripun, Lixiang Wei, and Jiangan Hu. "A low profile gate drive power supply." 2019 *IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2019.
- [6] Zoubir, Abdefihak M., and D. Robert Iskander. "Bootstrap methods and applications." *IEEE Signal Processing Magazine* 24.4 (2008): 10-19.
- [7] Yin, Shan, et al. "Design considerations and comparison of high-speed gate drivers for Si IGBT and SiC MOSFET modules." 2016 *IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2016.
- [8] IEC, IEC. "61800 adjustable speed electrical power drive systems—part 5-2: safety requirements—functional." (2007).
- [9] Anurag, Anup, et al. "Gate drivers for medium-voltage SiC devices." *IEEE Journal of Emerging and Selected Topics in Industrial Electronics* 2.1 (2020): 1-12.
- [10] Batra, Tushar, et al. "Isolation design considerations for power supply of medium voltage silicon carbide gate drivers." 2017 *IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2017.
- [11] Radmehr, Mahdi, and Mohammad Mojibi. "Reliability assessment and thermal consideration of a step-down DC/DC converter." *International Journal of Industrial Electronics*

- [12] Peng, Yingzhou, and Huai Wang. "A simplified on-state voltage measurement circuit for power semiconductor devices." *IEEE Transactions on Power Electronics* 36.10 (2021): 10993-10997.
- [13] Horiguchi, Takeshi, et al. "Short-circuit protection method based on a gate charge characteristic." *IEEJ Journal of Industry Applications* 4.4 (2015): 360-369.
- [14] Jiao, Chaogun, et al. "Integrated Rogowski coil sensor for press-pack insulated gate bipolar transistor chips." *Sensors* 20.15 (2020): 4080.
- [15] Yan, Wenyi, et al. "Variable Gate Resistance Drive Circuit Based on di/dt Feedback for IGBT." *Journal of Physics: Conference Series*. Vol. 2492. No. 1. IOP Publishing, 2023.
- [16] Chen, Min, et al. "An improved IGBT short-circuit protection method with self-adaptive blanking circuit based on V_{CE} measurement." *IEEE Transactions on Power Electronics* 33.7 (2017): 6126-6136.
- [17] Wittig, Bjoern, Matthias Boettcher, and Friedrich W. Fuchs. "Analysis and design aspects of a desaturation detection circuit for low voltage power MOSFETs." *Proceedings of 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010*. IEEE, 2010.
- [18] Schlegel, David W., et al. "Characteristics, selection guidelines and performance of circuit protection devices for ASDs." 2013 IEEE Industry Applications Society Annual Meeting. IEEE, 2013.
- [19] Karbalaeei, Alireza, and Mohammad Mardaneh. "Improved symmetric switched-inductor/capacitor quasi Z-source inverter with ability uplifted-boost." *International Journal of Industrial Electronics Control and Optimization* 3.1 (2020): 47-58.
- [20] Cho, Min-Hyeong, et al. "Development of undervoltage lockout (UVLO) circuit configured Schmitt trigger." 2015 International SoC Design Conference (ISOC). IEEE, 2015.
- [21] Bolloju, Vijay, and Jun Yang. "Influence of short circuit conditions on IGBT short circuit current in motor drives." 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2011.
- [22] Khalilzadeh, M., and A. Fereidunian. "A Markovian approach applied to reliability modeling of bidirectional DC-DC converters used in PHEVs and smart grids." *Iranian Journal of Electrical & Electronic Engineering* 12.4 (2016): 301.
- [23] Yin, Shan, et al. "Comparative design of gate drivers with short-circuit protection scheme for SiC MOSFET and Si IGBT." *Energies* 12.23 (2019): 4546.
- [24] Dalal, Dipen Narendra, et al. "Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter." 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe). IEEE, 2017.
- [25] Pluschke, Norbert, and Niklas Hofstoetter. "How to turn off IGBTs with Unipolar Voltage (0V)?" *PCIM Asia 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2015.
- [26] Asad, Mohsin, Amit Kumar Singha, and Ravada Madhu Sudhan Rao. "Dead time optimization in a GaN-based buck converter." *IEEE Transactions on Power Electronics* 37.3 (2021): 2830-2844.
- [27] Aeloiza, Eddy, Arun Kadavelugu, and Rostan Rodrigues. "Novel bipolar active miller clamp for parallel SiC MOSFET power modules." 2018 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2018.
- [28] Zhang, Fan, et al. "Advanced active gate drive for switching performance improvement and overvoltage protection of high-power IGBTs." *IEEE Transactions on Power Electronics* 33.5 (2017): 3802-3815.
- [29] Raki, A., Iman-Eini, H., Monfared, K. K., & Ahmadi, S. (2020, February). A Semi-Controlled Soft Charge Rectifier for Medium/High Power AC Drives: design and implementation. In 2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC) (pp. 1-6). IEEE.



Saeid Ahmadi received the B.Sc. and M.Sc. degrees in electrical engineering with honors from the University of Tehran, Tehran, Iran, in 2018 and 2020, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at University of Tehran, Tehran, Iran. His current research interests include advanced control for modular multilevel converters, and HVDC systems.



Kourosh Khalaj Monfared received the B.Sc. degree in electrical engineering from Shahid Beheshti University, Tehran, Iran, in 2015, M.Sc. and Ph.D. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 2017 and 2022, respectively. He is currently an Assistant Professor of electrical engineering at the School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran. His current research interests include advanced control in power electronics, multilevel converter applications, renewable energy systems, and pulsed power technology.



Mohammad Khalilzadeh was born in Urmia, Iran, in 1990. He received the B.Sc. and Ph.D. degrees in electrical engineering from the University of Tehran, in 2012 and 2021, respectively, and the M.Sc. degree from the K. N. Toosi University of Technology, in 2014. He is currently an Assistant Professor with Faculty of Electrical and Computer Engineering, Tarbiat Modares University, Tehran. His research interests include power electronics and motor drives.



Hossein Iman-Eini (Senior Member, IEEE) received the Ph.D. degree in electrical engineering jointly from the University of Tehran, Tehran, Iran, and Grenoble Alpes University, Grenoble, France, in 2009. He is a Professor of electrical engineering with the School of Electrical and Computer Engineering, University of Tehran. He currently follows a Heisenberg position as the Chair of Power Electronics with Kiel University, Kiel, Germany. His research interests include power electronics and applications of power electronics in power systems/grids.