IECO International Journal Of Industrial Electronics Control and Optimization
Print ISSN: 3517-2645
Online ISSN: 3568-2645
Homepage: https://ieco.usb.ac.ir/

Robust QCA Full Adders Using a Novel Fault Tolerant Five-Input Majority Gate

Farzaneh Jahanshahi Javaran[1] | Somayyeh Jafarali Jassbi[1] | Hossein Khademolhosseini[1,2] | Razieh Farazkish[3]

Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran.[1]
Department of Computer Engineering, Beyza Branch, Islamic Azad University, Beyza, Iran.[2]
Department of Computer Engineering- South Tehran Branch, Islamic Azad University, Tehran, Iran.[3]
Corresponding author's email: h.khademolhosseini@srbiau.ac.ir

Article Info

Article type:
Research Article

Article history:
Received: 2024-Jan-23
Received in revised form: 2024-Mar-03
Accepted: 2024-Mar-05
Published online: 21-June-2024

Keywords:
Quantum Cellular Automata,
Nano Electronics,
Fault-Tolerant,
Majority Gate.

ABSTRACT

A novel technique for creating logic gates and digital circuitry at the nanoscale is quantum cellular automata (*QCA*). The sensitivity of the circuit is enhanced and quantum circuits are more susceptible to unfavorable external conditions when component size are reduced. In this article, we offer a five-input majority gate with fault-tolerant feature in QCA technology, taking into account the significance of constructing circuits that can withstand flaws. We also assess all potential defects in the process of arranging cells in specific locations on the surface. These errors consist of extra cells, rotation, deletion, and displacement. The gate under study is subjected to the aforementioned four failure categories in the first stage. The QCADesigner simulator engine is then used to assess the accuracy of the circuit performance in the second step. *41* quantum cells have been used to make the gate of this five-input majority gate with fault-tolerant feature in QCA technology. Several techniques are explored to discover such a majority gate, such as adding cells (i.e., introducing redundancy into the circuit) and particular cell layout techniques. The goal is to come up with a design that can ideally withstand possible faults with the least amount of overhead on the circuit for fault-tolerant through a certain cell layout. The findings demonstrate the implemented majority gate's notable advantage over comparable scenarios.

I. Introduction

According to the trend of moving towards nano technology, quantum cellular automata (*QCA*) is a new technology for implementing logic gates and digital circuits in the nano scale [1]. This technology has many features such as small area, high processing speed and low power consumption, and also the elimination of electric current and the elimination of the capacitor element is one of the reasons for its popularity. In QCA, the information is expressed by binary numbers, and with this difference, a cell has taken the place of the current switch. One state of the cell indicates a binary *1* and the other a binary *0*, while no current enters or leaves the cell. The field caused by the charge shape of one cell changes the charge shape of another cells [2]. This mutual connection is associated with a timing scheme that regulates the effect between states and this is sufficient for calculation with the lowest amount of power loss. In recent years, QCA have received much attention because designs and simulations show that QCA will have many capabilities compared to complementary metal-oxide semiconductor *(CMOS)*, but it is still not clear that this technology can replace *CMOS*, even though many of the problems and obstacles of building QCA are being solved with the passage of time [3]. So far, a large number of implementations for three- and five-input majority gates have been presented, but a limited number of fault-tolerant five-input majority gates have been introduced and research in this particular field is appropriate.

II. Basic Concepts of QCA and Related Works

The basic and important principle in quantum technology is the cell and in Figure 1 shows a four-point QCA-based cell. These four quantum dots are placed in the shape of a square. Exactly two mobile electrons are placed in the cell, which have the ability to move between different quantum points in a cell using electron tunneling, and stable states are established when the holes are occupied diagonally. According to Coulomb repulsion law, the location of these two electrons in the holes will be in opposite corners, which creates two structures. These two structures show the two poles *+1 and -1*, which in the calculations, we assign logical values *1 and 0* to them, respectively [4].

Fig. 1. QCA cell.

QCA has a clock-based mechanism that includes a four-clock signal with equal frequencies. We consider one of the clock signals as a reference phase (*0*) and the rest with a delay of one ($\frac{\pi}{2}$), two (π) and three ($3\frac{\pi}{2}$) quarters of the period. Clock is an electronic factor that controls the movement of electrons inside the cell [5, 6]. In fact, the way it is controlled is that if information reaches a part of the circuit that needs to be combined with several other inputs to produce an output, if the other inputs arrive at that part of the circuit later, it prevents the dissemination of information in that part until the arrival of the other inputs [7]. As shown in Figure 2, each clock signal is divided into four parts: *switch, hold, release, and relax.*

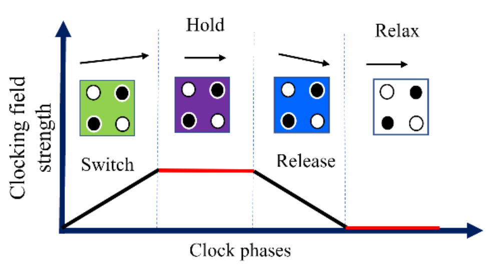


Fig. 2. QCA Clock phases.

Each cell also affects the neighboring cells. If two cells are placed next to each other, they always end up in a state where the repulsive force is minimized. An array of adjacent cells can be used like a wire to transmit information. Also, the cells can be placed in a 45- or 90-degree position, where the 45-degree wire is formed by rotating the cells 45 degrees [8]. In this type of wire, the binary value changes sequentially within the cells. The two wire configurations in QCA are depicted in Figure 3.

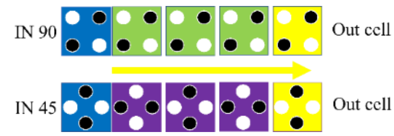


Fig. 3. QCA wires.

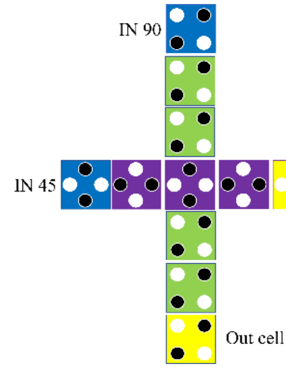


Fig. 4. QCA wiring.

Another benefit of this technology is the capacity to cross wires [9]. Additionally, cables may be arranged in several layers without negatively affecting one another, or two distinct kinds of cells can be bridged by utilizing both kinds of cells. Figure 4 shows wiring with two distinct kinds of cells.

Inverter gate and majority gate are two basic gates in QCA technology. In majority gate, considering all the input states, the output always shows the majority. Most circuits are made based on these two gates [10, 11]. Figure 5 shows two 3- and 5-input majority gates and an inverting gate.

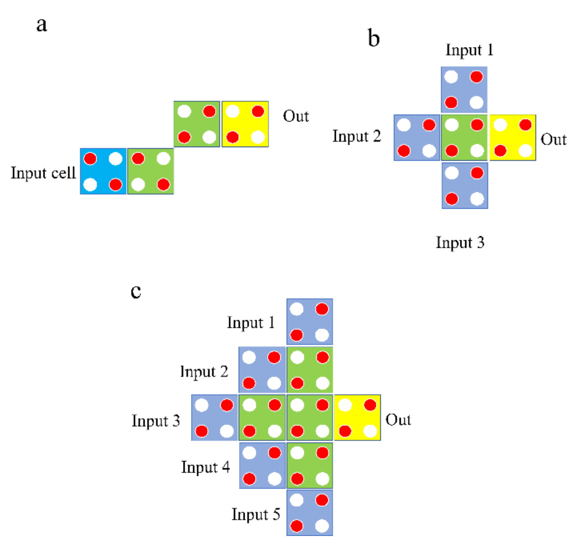


Fig. 5. QCA basic gates: (a) A QCA inverter, (b) a three-input majority gate and (c) a five-input majority gate.

In addition to the cases mentioned, there are types of defects in QCA technology. In the QCA fabrication stage, the occurrence of faults is possible in both the synthesis phase (where individual cells are constructed) and the placement phase (where cells are positioned at specific locations).

Defects in the synthesis phase may cause the cell or cells to lose some of their holes or electrons or gain some extra holes or electrons. Such defects disrupt the correct operation of the cell and are usually easily detectable, but defects in the process of placement are more likely than in the process of synthesis [12]. The defects created in the placement phase are called misplacement. The possible faults that occur in this technology include displacement faults, cell displacement, cell omission, cell rotated, and extra-cell. Displacement faults are faults that quantum cells move in their original direction. The fault of omission is the fault that a cell has been removed from the circuit. The fault of rotation means that the cell rotates in proportion to the adjacent cells in such a way that the direction of the cell changes, and the fault of the extra-cell is the shape that during the process of placing the cells, one or a number of additional cells may be added to the circuit [13]. Figure 6 shows the types of faults of QCA technology.

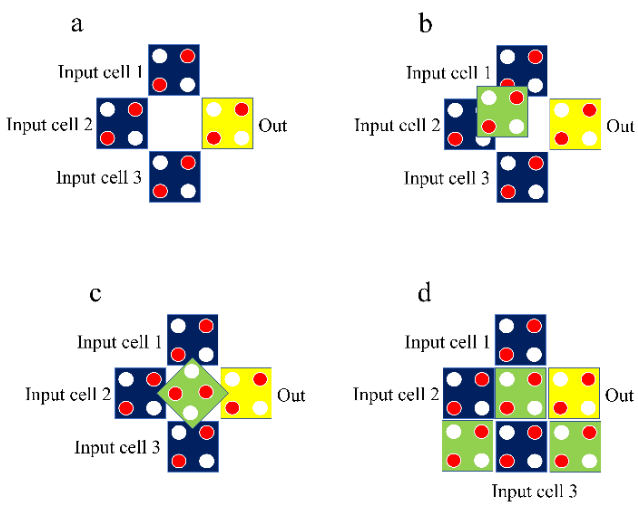


Fig. 6. Type of faults: (a) Cell omission, (b) cell displacement, (c) cell rotation, and (d) extra-cell deposition [14].

In the following, we have reviewed some of the latest designs of fault-tolerant five-input majority gate.

Farazkish [15] created a fault-tolerant five-input majority gate with *50* cells and an area of *0.0352* μm^2. The gate exhibits *13.6%* fault-tolerant to single-cell omission (Figure 7(a)). One of the disadvantages of this gate was that the output was in the middle, necessitating a multilayer structure to construct the circuit. Du, et al. [16] suggested a fault-tolerant five-input majority gate with *22* cells and an occupied area of *0.0163* μm^2, making it *12.5%* fault resistant to the single-cell omission defect (Figure 7 (b)). A fault-tolerant four-input majority gate with *27* cells and an occupied area of *0.0318* μm^2 was given by Goswami, et al. [17]. It is *28%* fault resistant to the single-cell omission defect (Figure 7 (c)). A fault-tolerant five-input majority gate with 27 cells and an occupied area of *0.0135* μm^2 was suggested by Sun, et al. [18]; it has a fault tolerance of up to *47.62%* (Figure 7 (d)).

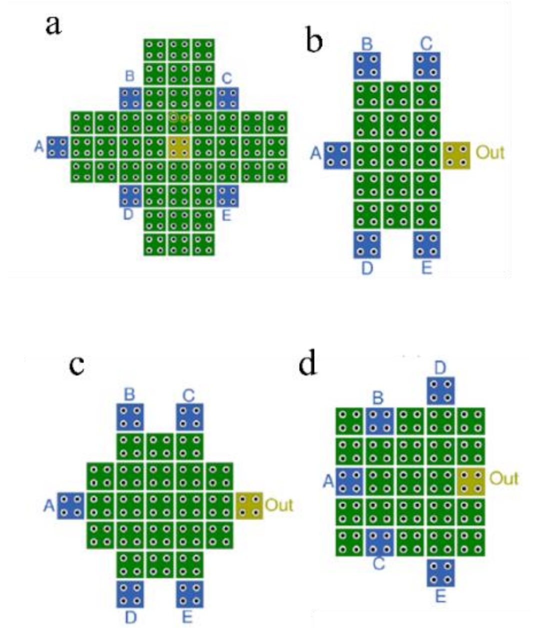


Fig. 7. Cellular structures of fault-tolerant, five-input majority gates: (a) [15], (b) [16], (c) [17], and (d) [18].

III. The Proposed Five-Input Majority Gate

The proposed fault-tolerant five-input majority gate is shown in Figure 8. This gate is designed with *41* quantum cells in the occupied space of *38804 square nanometers*. From the structural point of view, the proper arrangement of the input cells and the length of the used wires have caused their coordinated effect and as a result, the majority of the five input gates have been created. The simulation results from the QCADesigner simulation engines show the correct performance of the circuit for all *32* input combinations. The test vectors are sequentially applied to the inputs and the resulting waveform is examined by each engine separately. Matching the waveforms shows the accuracy of the designed circuit. Figure 9 shows the result of bistable approximation simulation of the circuit.

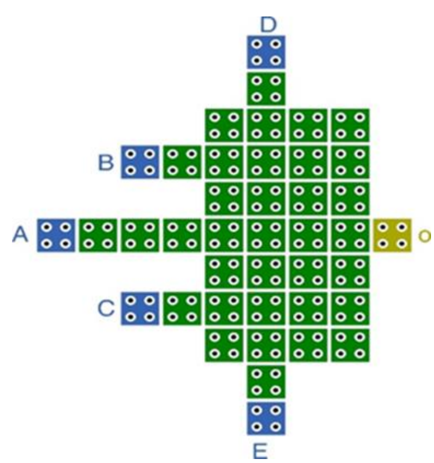


Fig. 8. Proposed defect tolerant five-input majority gate designed with minimal hardware complexity in QCA.

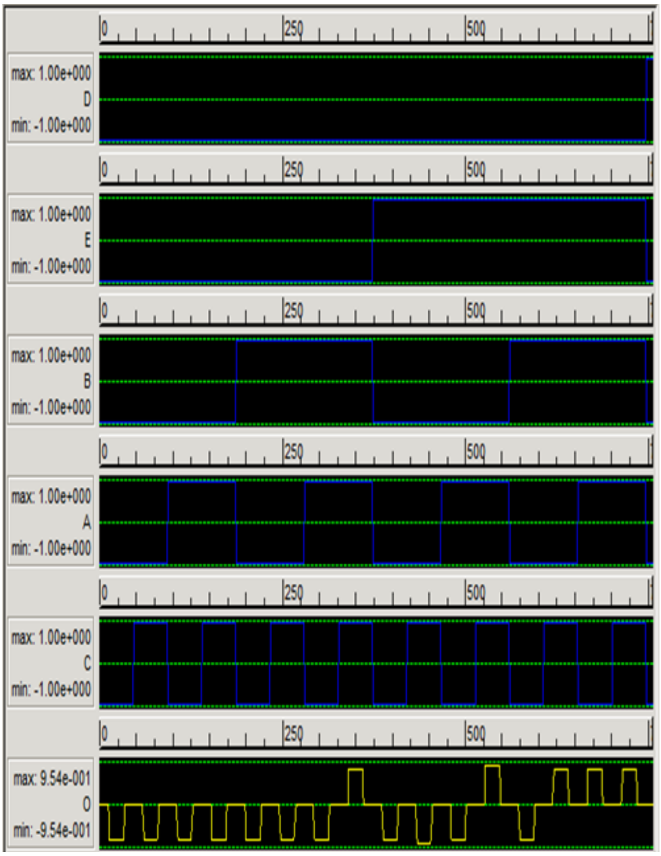


Fig. 9. The simulation results of proposed fault-tolerant five-input majority gate.

IV. Fault Tolerance Analysis

As shown in Figure 10, for applying defects to the majority gate, a number of cells in the circuit are considered as test cells. These cells have been selected for examination in more sensitive areas. The specified numbers indicate the area of application of the faults.

The results of the analysis of the displacement faults of the proposed gate are shown in Table 1. As it is evident, the displacement of *10* selected cells along with input and output cells of the circuit have been investigated as test cells in the four directions of north, south, east and west. The maximum amount of displacement faults allowed in the process of cell arrangement for each of the cells while maintaining the correct function of the output cell (*O*) has been studied. Considering the high importance of the input and output cells, we examine the performance of two cells, for example cell A can move up to *5 and 1 nm* in the west and east (horizontal movement) and on the other hand, 6 nm movement in the vertical direction for this cell is imaginable. Cell D with 5 nm displacement in the horizontal direction and 4 nm in the north direction has significantly increased the tolerance of the circuit. It is worth noting that all the middle cells that are surrounded by other cells have tolerance of 1 nm displacement in the four directions.

TABLE 1
MAXIMUM TOLERANCE AGAINST DISPLACEMENT FAULTS (THE NUMBERS SHOWN ARE THE MAXIMUM ALLOWABLE DISPLACEMENT IN NANOMETERS WHILE MAINTAINING CORRECT OUTPUT PERFORMANCE)

North	South	East	West	Cell
6	6	1	5	**A**
3	3	1	2	**B**
3	3	1	2	**C**
4	1	5	5	**D**
1	4	5	5	**E**
3	3	3	1	**O**
5	1	1	5	**1**
1	1	1	1	**2**
1	1	6	1	**3**
1	1	1	1	**4**
1	1	1	1	**5**
4	4	1	1	**6**
1	1	1	1	**7**
1	1	1	1	**8**
1	7	6	1	**9**
1	1	1	1	**10**

As shown in Table 2, the tolerance of the proposed circuit against the omission faults have been evaluated respectively by measuring the output of the circuit. The waveform obtained from the simulation after removing each cell has been compared with the waveform obtained from the faultless circuit, and if the output is preserved, the result is reported. In Table 2, out of the *10* cells examined for omission faults, ignoring *4* cells did not affect the output, and therefore *40%* can be considered as the tolerance percentage of omission faults.

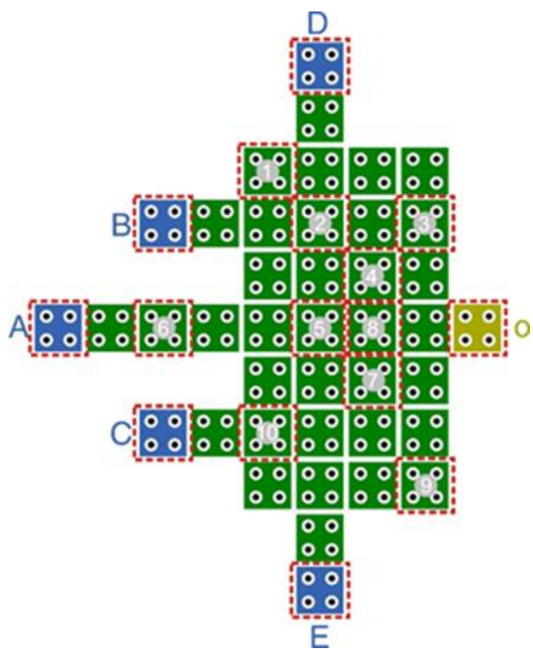


Fig. 10. The proposed majority gate along with the analyzed points for displacement, omission and rotated.

Also, as shown in Table 2, the tolerance of the proposed circuit against the omission faults have been evaluated respectively by measuring the output of the circuit. The waveform obtained from the simulation after removing each cell has been compared with the waveform obtained from the faultless circuit, and if the output is preserved, the result is reported. In Table 2, out of the *10* cells examined for omission faults, ignoring 4 cells did not affect the output, and therefore *40%* can be considered as the tolerance percentage of omission faults.

TABLE 2
TOLERABILITY OF OMISSION FAULTS AND ITS EFFECT ON THE OUTPUT

Output	Omission cell
MV5	**1**
Incorrect	**2**
Incorrect	**3**
Incorrect	**4**
MV5	**5**
Incorrect	**6**
Incorrect	**7**
MV5	**8**
MV5	**9**
Incorrect	**10**

For investigating the effects of cell rotation defects and their impact on the output, Table 3 has been considered. As it has been determined, in *40%* of the cases, the rotation faults have been covered.

TABLE 3
ANALYZING THE ACCEPTABLE TOLERANCE OF THE FAULTS BASED ON THE ACCEPTABLE TOLERANCE OF THE ROTATION FAULTS AND ITS EFFECT ON THE OUTPUT

Output	Rotated cell
MV5	**1**
Incorrect	**2**
Incorrect	**3**
Incorrect	**4**
MV5	**5**
Incorrect	**6**
Incorrect	**7**
MV5	**8**
MV5	**9**
Incorrect	**10**

In order to analyze the extra-cell faults on the majority gate circuit, Figure 11 is considered. The 9 ×11 rectangle shows all the places that can be used for adding cells to the proposed circuit. As shown in Table 4, among these places, *12* places have been selected and numbered according to the sensitivity of the test place. It seems that among all the locations examined, only adding a cell at one specific location has caused a change in the output value, demonstrating that the proposed circuit has a tolerance of *91.6%* against additional defects.

TABLE 4
TOLERABILITY OF REDUNDANCY FAULTS AND ITS EFFECT ON OUTPUT

Output	Additional cell
MV5	**1**
MV5	**2**
Incorrect	**3**
MV5	**4**
MV5	**5**
MV5	**6**
MV5	**7**
MV5	**8**
MV5	**9**
MV5	**10**
MV5	**11**
MV5	**12**

Table 5 shows a comprehensive hardware comparison of the five-input majority gates. In this table, the proposed gate has been compared with the seven previously presented circuits in terms of the number of consumed cells, the occupied area and accessing the input and output cells from the structural aspect. The proposed circuit has the lowest average tolerable percentage of faults compared to the lasted fault-tolerant gates. On the other hand, the new gate in this research along with two last beast designs have simultaneous single-layer access to input and output cells. This significantly facilitates the process of building QCA circuits because there will be no need for multi-layer structures or layered wiring and the inputs and outputs of the circuit can easily be connected to other circuits.

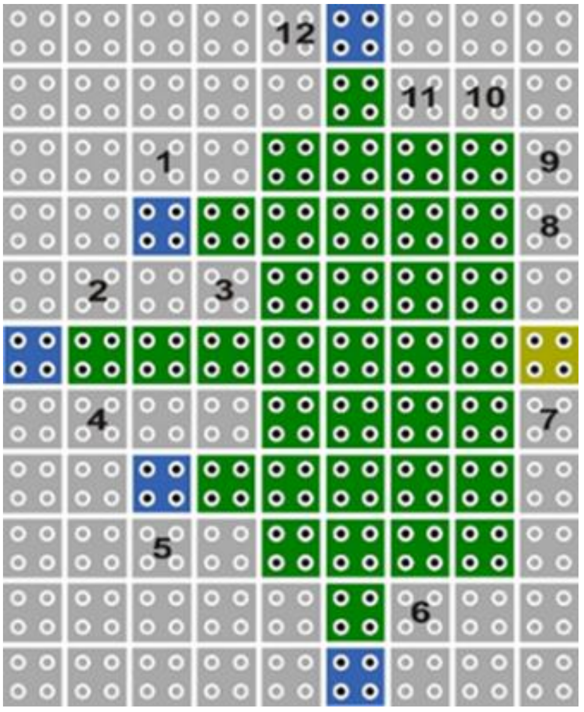


Fig. 11. The proposed five-input fault-tolerant majority gate circuit along with the analyzed points for redundancy fault.

TABLE 5
STRUCTURAL COMPARISON OF THE FIVE-INPUT MAJORITY GATES

Designs	Area (nm^2)	Cell count	Accessibility to the output cells	Accessibility to the input cells	Average Fault-tolerant
Proposed design	38804	41	Yes	Yes	60/75
[19]	34444	42	Yes	Yes	51/20
[15]	38804	51	No	Yes	48/30
[20]	7644	10	Yes	No	Less than 10
[21]	4524	10	No	Yes	Less than 10
[22]	16284	18	Yes	Yes	Less than 10
[23]	9604	13	Yes	Yes	Less than 10
[24]	22400	28	Yes	Yes	34

V. The Proposed Fault-Tolerant QCA Logic Circuits

In the five-input majority gate, by fixing two of the inputs to zero and one, it is possible to design three input AND gate and three input OR gate. In the case that two of the inputs are zero, the output of the function is one only when the other two inputs are one, otherwise the output of the function will be zero. So, the behavior of the system will be like an "*AND*" operator. In the same way, by fixing *+1* polarization to two of the inputs, a two input "*OR*" gate can be designed and they are implemented based on Eq. (1) and (2).

$$AND(A,B,C) = A.B.C = MV5(A,B,C,0,0) \qquad (1)$$

$$OR(A,B,C) = A + B + C = MV5(A,B,C,1,1) \qquad (2)$$

Figure 12 shows the symbols of a three input "*AND*" gate and a three input "*OR*" gate.

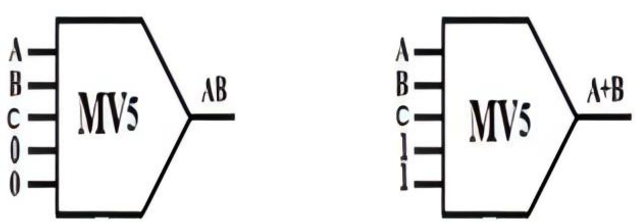


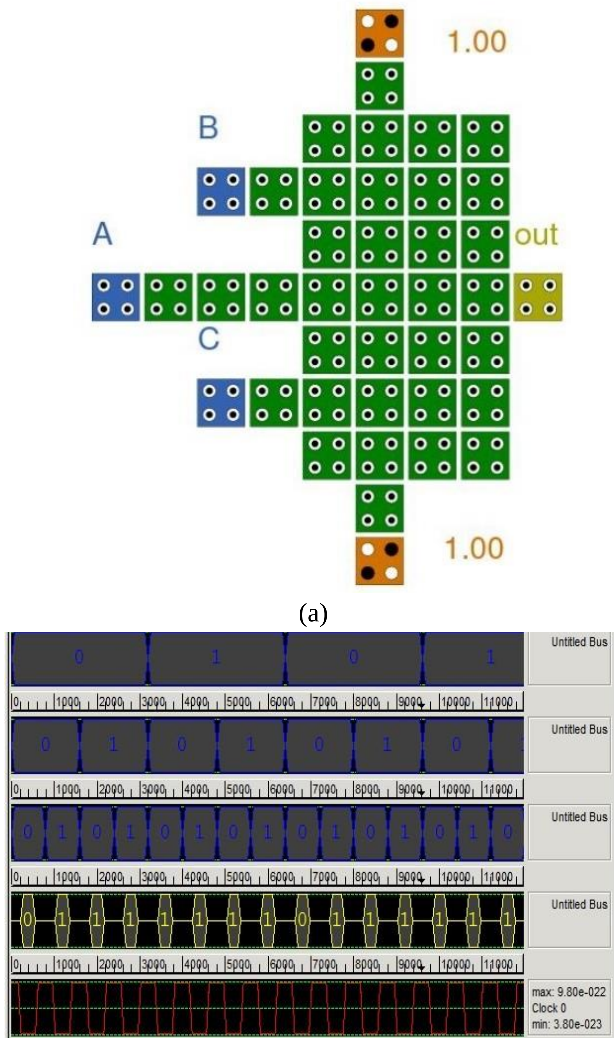
Fig. 12. Symbols of three input *AND* and *OR* gate.

Table 6 shows three input *"AND", "OR", "NAND" and "NOR"* gates.

TABLE 6
IMPLEMENTATIONS OF 3-INPUT *"AND", "OR", "NAND" AND "NOR"* GATES

A	B	C	D	E	OUT
--	--	--	-	-	3-input AND
--	--	--	1	1	
--	--	--	1	1	3-input OR
--	--	--			
--	--	--	1	1	3-input NAND
--	--	--			
--	--	--	-	-	3-input NOR
--	--	--	1	1	

The three input "*AND*" gate using the proposed gate and the related simulation results are shown in Figure 13.

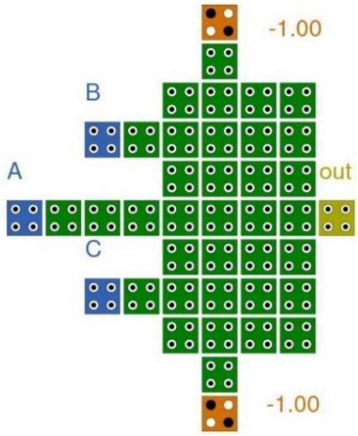


(a)

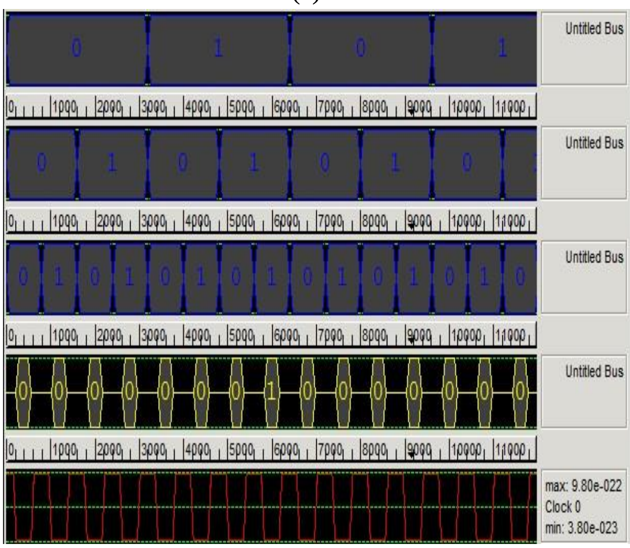
(b)

Fig. 13. (a) The QCA layout of proposed fault-tolerant 3-input AND gate, and (b) simulation results.

The three input "OR" gate using the proposed gate and the related simulation results are shown in Figure 14.



(a)



(b)

Fig. 14. (a) The QCA layout of proposed fault-tolerant 3-input OR gate, and (b) simulation results.

On the other hand; *"XOR"* gate is a logical gate that is applied to two operands, if exactly one of them is true, the output returns the true value or one, and otherwise the output value is false or zero. A two input *"XOR"* gate is implemented based on Eq. (3).

$$2 - input\ XOR(A,B) = \bar{A}B + A\bar{B} = MV5(A,B,0,\overline{MV3(A,B,0),MV3(A,B,0)}) \quad (3)$$

The *"XOR"* gate is designed and implemented with the five-input majority gate proposed in this article and the three-input majority gate, so that two of the five input majority gate inputs named *A and B* and two of the other inputs are connected to the inverted output of three input majority gate and the remaining input of the five-input majority gate is connected to zero. Two of the inputs of the three-input gate are connected to *A and B*, and the third input is connected to *zero*. In Figure 15 the symbol of the two input *"XOR"* gate is shown.

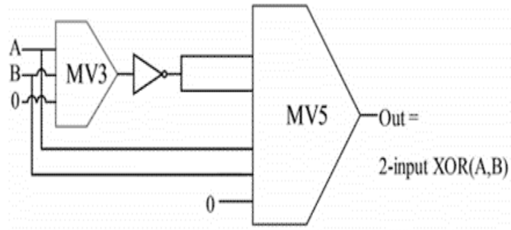
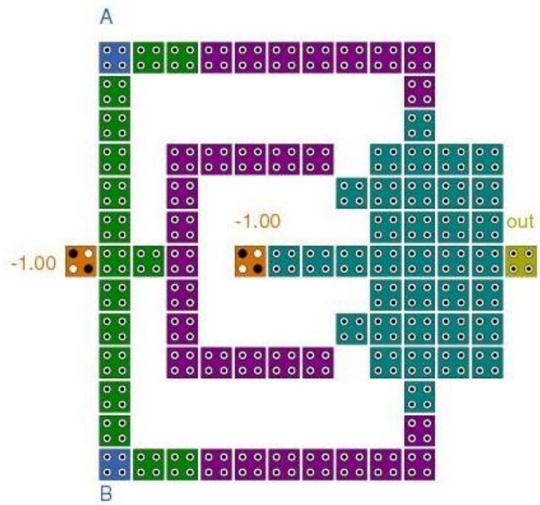
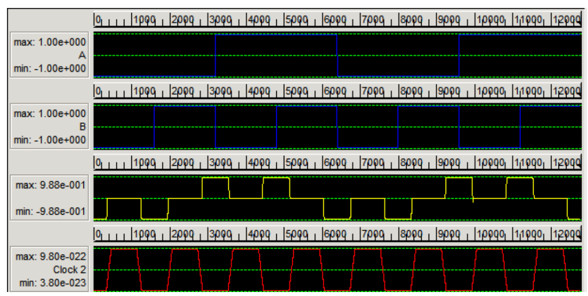


Fig. 15. Symbol of two input XOR gate.

The layout and simulation results of the 2-input "XOR" gate are shown in Figure 16.



(a)



(b)

Fig. 16. The proposed 2-input *"XOR"* gate; (a) QCA layout, and (b) simulation results.

Also, the *"XNOR"* gate is a digital logic gate and actually the complement of the *"XOR"* gate. This gate includes two or more inputs and one output, in the *"XNOR"* gate, the output becomes one if either both inputs are zero or both inputs are one. The two input *"XNOR"* gate is made based on Eq. (4).

$$2 - input\ XNOR(A,B) = A.B + \bar{A}.\bar{B} = MV5(A,B,1,\overline{MV3(A,B,1),MV3(A,B,1)}) \quad (4)$$

The *"XNOR"* gate designed in this article is the same as the *"XOR"* gate with the difference that the inputs are connected to one instead of zero. Figure 17 shows the symbol of the two input *"XNOR"* gate.

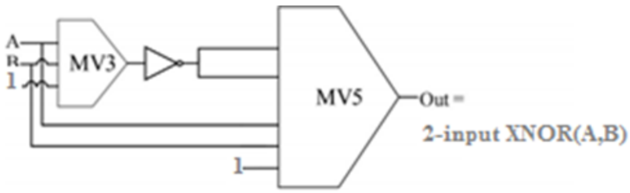
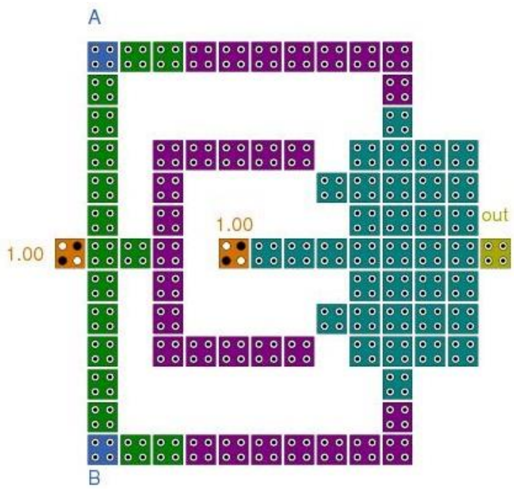
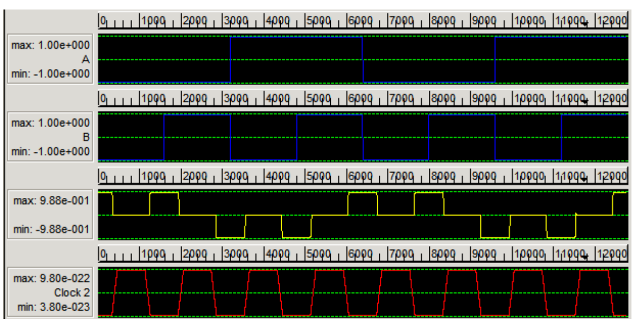


Fig. 17. Symbol of two input XNOR gate.

Figure 18 shows the layout of the two input *"XNOR"* gate and simulation results.



(a)



(b)

Fig. 18. The proposed 2-input *"XNOR"* gate; (a) QCA layout, and (b) simulation results.

Also, the full-adder is implemented based on relations (5) and (6) [25, 26]:

$$Cout = AB + AC + BC = MV5(A, B, C, 0,0) \quad (5)$$

$$Sum = A \oplus B \oplus C = MV5(A, B, C, Cout, Cout) \quad (6)$$

The full-adder designed in this article includes a five-input majority gate and a three-input majority gate and an inverting gate. Figure 19 shows the symbol of the full-adder circuit.

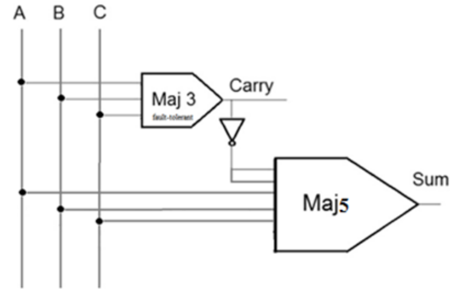
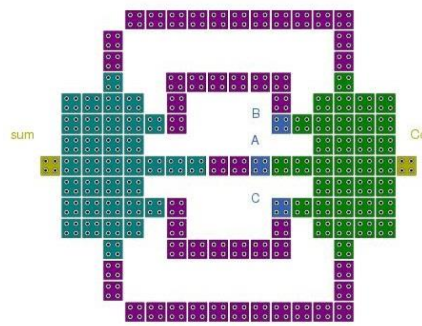
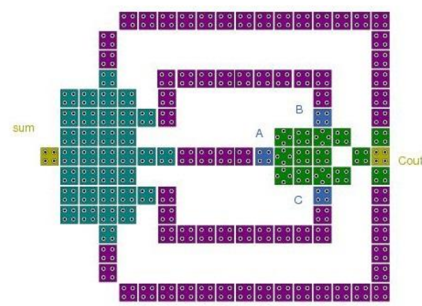


Fig. 19. The Symbol of full-adder.

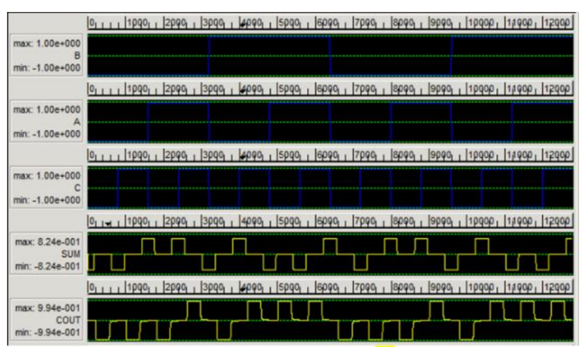
The full-adder circuit is designed and implemented in one layer and works in one clock phase, Figure 20 shows two layouts and simulation results for the full-adder circuit with QCADesigner software.



(a)



(b)



(c)

Fig. 20. The proposed full-adder (a) plan 1, (b) plan 2 and (c) simulation results.

VI. Conclusions

Because of its great density, low power, and rapid speed, QCA technology was seen as one of the finest alternatives to *CMOS* technology. Due to the novelty of QCA technology, some major concerns have yet to be properly explored. One of the most critical issues is fault-tolerant. As a result, the design of fault-tolerant QCA computational circuits is critical. The presentation of fault-tolerant designs in QCA technology, like other technologies, has been of great interest. In this article, a new fault-tolerant five input majority gate with minimal cell overhead has been designed and simulated in QCA technology. The new majority gate in this article is designed in one layer and with one clock phase. This gate is designed with *41* quantum cells in the occupied space of *38804* square nanometers. For this circuit, in addition to the structural analysis, the tolerance analysis of the circuit was investigated when four faults of displacement, deletion, rotation and redundancy were applied, and the correctness of the circuit performance was tested with QCADesigner simulator engines. It was demonstrated that the suggested gate was *60% and 75%* tolerant to single-cell omission and extra-cell deposition errors, respectively. It was also very stable under cell displacement and misalignment errors. Then three input *"AND" and "OR"* gates, two input *"XOR" and "XNOR" gates* and a *full-adder circuits* have been designed and simulated. The evaluation findings demonstrated that the circuits constructed using the suggested structure outperformed those designed using earlier fault-tolerant gates. Finally, we developed and built fault-tolerant single-layer full-adders employing the suggested fault-tolerant QCA majority gate. The circuits suggested in this article can be used as a foundation for future work to create more complicated and fault-tolerant designs such as multipliers, dividers, and so on.

REFERENCES

[1] F. Motalebi and S. Sayedsalehi, "Design of Low Power Full-Adder Circuit Using Quantum-dot Cellular Automata," International Journal of Industrial Electronics Control and Optimization, vol. 5, no. 1, pp. 99-108, 2022.

[2] S. F. Naz, S. Riyaz, and V. K. Sharma, "A Review of QCA Nanotechnology as an Alternate to CMOS," *Current Nanoscience*, vol. 18, no. 1, pp. 18-30, 2022.

[3] A. Shamsi, "A new Mismatch cancelation for Quadrature Delta Sigma Modulator," International Journal of Industrial Electronics Control and Optimization, vol. 3, no. 2, pp. 196-204, 2020.

[4] S. Seyedi and N. J. Navimipour, "A fault-tolerant image processor for executing the morphology operations based on a nanoscale technology," Multimedia Tools and Applications, vol. 82, no. 2, pp. 2489-2502, 2023.

[5] R. Marshal and G. Lakshminarayanan, "Fault resistant coplanar QCA full adder-subtractor using clock zone-based crossover," IETE Journal of Research, vol. 69, no. 1, pp. 584-591, 2023.

[6] K. Pandiammal and D. Meganathan, "Efficient design of QCA based hybrid multiplier using clock zone based crossover," Analog Integrated Circuits and Signal Processing, vol. 102, pp. 63-77, 2020.

[7] L. Wu, Z. Shen, and Y. Ji, "Using nano-scale QCA technology for designing fault-tolerant 2:1 multiplexer," Analog Integrated Circuits and Signal Processing, vol. 109, pp. 553-562, 2021.

[8] L. Zhou et al., "Narrowband photoblinking InP/ZnSe/ZnS quantum dots for super-resolution multifocal structured illumination microscopy enhanced by optical fluctuation," Nanophotonics, no. 0, 2023.

[9] S. Seyedi and B. Pourghebleh, "A new design for 4-bit RCA using Quantum Cellular Automata Technology," Optical and Quantum Electronics, vol. 55, no. 1, p. 11, 2023.

[10] J. Huang and S. Lale, "A novel nano-scale architecture of Vedic multiplier using majority logic in quantum-dot cellular automata technology," Electronics Letters, vol. 58, no. 17, pp. 660-662, 2022.

[11] C. Labrado and H. Thapliyal, "Design of adder and subtractor circuits in majority logic-based field-coupled QCA nanocomputing," Electronics letters, vol. 52, no. 6, pp. 464-466, 2016.

[12] Y. Yin, J. Liu, and C. She, "A new fault-tolerant single-bit comparator in QCA technology using a novel X-NOR gate," Optik, vol. 269, p. 169837, 2022.

[13] D. Pan, B.-N. Wu, Y.-L. Sun, and Y.-P. Xu, "A fault-tolerant and energy-efficient design of a network switch based on a quantum-based nano-communication technique," Sustainable Computing: Informatics and Systems, vol. 37, p. 100827, 2023.

[14] K. Das and D. De, "QCA defect and fault analysis of diverse nanostructure for implementing logic gate," International Journal of Recent Trends in Engineering and Technology, vol. 3, no. 1, p. N/A, 2010.

[15] R. Farazkish, "A new quantum-dot cellular automata fault-tolerant five-input majority gate," Journal of nanoparticle research, vol. 16, pp. 1-7, 2014.

[16] H. Du, H. Lv, Y. Zhang, F. Peng, and G. Xie, "Design and analysis of new fault-tolerant majority gate for quantum-dot cellular automata," Journal of Computational Electronics, vol. 15, pp. 1484-1497, 2016.

[17] M. Goswami, B. Sen, and B. K. Sikdar, "Design of low power 5-input majority voter in quantum-dot cellular automata with effective error resilience," in 2016 sixth international symposium on embedded computing and system design *(ISED)*, 2016: IEEE, pp. 101-105.

[18] M. Sun, H. Lv, Y. Zhang, and G. Xie, "The fundamental primitives with fault-tolerance in quantum-dot cellular automata," Journal of Electronic Testing, vol. 34, no. 2, pp. 109-122, 2018.

[19] R. Farazkish and K. Navi, "New efficient five-input majority gate for quantum-dot cellular automata," Journal of Nanoparticle Research, vol. 14, pp. 1-6, 2012.

[20] K. Navi, R. Farazkish, S. Sayedsalehi, and M. R. Azghadi, "A new quantum-dot cellular automata full-adder," Microelectronics Journal, vol. 41, no. 12, pp. 820-826, 2010.

[21] K. Navi, S. Sayedsalehi, R. Farazkish, and M. R. Azghadi, "Five-input majority gate, a new device for quantum-dot cellular automata," Journal of Computational and Theoretical Nanoscience, vol. 7, no. 8, pp. 1546-1553, 2010.

[22] R. Akeela and M. D. Wagh, "A five-input majority gate in quantum-dot cellular automata," in NSTI Nanotech, 2011, vol. 2, pp. 978-981.

[23] A. Roohi, H. Khademolhosseini, S. Sayedsalehi, and K. Navi, "A symmetric quantum-dot cellular automata design for 5-input majority gate," Journal of Computational Electronics, vol. 13, pp. 701-708, 2014.
[24] S.-S. Ahmadpour, M. Mosleh, and S. R. Heikalabad, "An efficient fault-tolerant arithmetic logic unit using a novel fault-tolerant 5-input majority gate in quantum-dot cellular automata," Computers & Electrical Engineering, vol. 82, p. 106548, 2020.
[25] H. Khademolhosseini and Y. Nemati, "A New Design for Two-input XOR Gate in Quantum-dot Cellular Automata," Journal of Advances in Computer Research, vol. 10, no. 1, pp. 89-96, 2019.
[26] H. Khademolhosseini, S. Angizi, and Y. Nemati, "A fault-tolerant design for 3-input majority gate in quantum-dot cellular automata," Journal of Nanoelectronics and Optoelectronics, vol. 13, no. 1, pp. 93-103, 2018.

Farzaneh Jahanshahi Javaran was born in Kerman, Iran She a PhD student in Computer Systems Architecture from Islamic Azad University, Science and Research Department. University of Science and Research is a prestigious university in the field of computer systems architecture in Iran. Currently, her researching the design of fault-tolerant majority gates in quantum cellular automata. Her current research interests include quantum dot cellular automata, fault tolerance.

Sommayeh Jafarali Jassbi was born in Tehran, Iran, in 1982. She received the MSc degree in computer architecture engineering in 2007, and the Ph.D. degree in computer architecture engineering in 2010 from the Islamic Azad University, Science and Research Branch. In 2010, she joined the Department of computer engineering, Islamic Azad University Science and Research Branch. She became an associate professor in 2011. Her interests are cloud computing, internet of things, wireless sensor network and computer architecture and cryptography. She was head of computer department in 2012. Now she is selected as a head of computer department again. She was also an active member of young researcher club from 2004. She has written, translate and published several professional books and paper in her fields.

Hossein Khademolhosseini received B.Sc. degree in computer engineering in 2008 from Shiraz University, Shiraz, Iran. He also received his M.Sc. and Ph.D. degree in computer architecture at Department of Computer Engineering, Science and Research Branch of Islamic Azad University, Tehran, Iran, in 2011 and 2016, respectively. He is currently an assistant professor with the Department of Computer Engineering, Islamic Azad University, Beyza Branch. His research interests are computer arithmetic, photonic NoC and electronics with emphasis on QCA and VLSI.

Razieh Farazkish received the B.S. degree in computer engineering from the IAU, Central Tehran Branch (2007) and the M.S. (2009) and Ph.D. (2012) degrees in computer engineering from the IAU, Science and Research Branch. In 2012, she joined the Department of Computer Engineering, IAU, South Tehran Branch, as a Professor. Her current research interests include quantum-dot cellular automata, fault tolerance, nanoelectronic circuits, nano computing, testing and design of digital systems.