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Optimized Algorithm for Open-Circuit Fault Detection in Switches and Capacitor Voltage Balancing Control in Modular Multilevel Converters

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ABSTRACT

The modular multilevel converter (MMC) is a favored topology in the industry, but its reliability is at risk with an increase in the number of sub-modules (SMs) due to a rise in switching components. The essential need for maintaining capacitor voltage balance in each arm leads to increased complexity and cost, as numerous voltage sensors are required. This study introduces an innovative approach to minimize the number of voltage sensors by employing an enhanced algorithm for open-circuit fault detection in switches. The proposed scheme organizes each arm into groups, each containing two SMs and one voltage sensor, aiming to reduce the overall sensor count. A novel fault detection mechanism is presented, identifying open-circuit faults by comparing group output voltages in healthy and defective conditions. The capacitor voltage estimation algorithm in the sensor reduction scheme is noted for its simplicity compared to other methods. The effectiveness of these methods is validated through simulations and experimental implementations across diverse scenarios, affirming their reliability.

I. Introduction

Recently, the modular multilevel converter (MMC) has been used frequently for its various advantages [1], [2], [3]. These include fully modular design, easy construction, excellent output waveform quality, and fault tolerance in high and medium power applications [4], [5]. In the range of medium and high power applications, MMC with over 200 sub-modules (SMs) has been used in each arm [6], [7]. As the number of SMs increases, the converter's reliability reduces due to the use of numerous semiconductor switches [8], [9]. One of the most vulnerable components of power electronic converters is semiconductor switches [10], [11]. Typically, open-circuit and short-circuit failures on semiconductor switches are the two most common types of faults. [12], [13].

Short-circuit faults are extremely damaging and immediately cause numerous obstructions to the system [14]. Therefore, short-circuit faults must be identified quickly, and the identification process typically uses hardware methods [12]. On the other hand, open-circuit faults are not dangerous for the system immediately after the occurrence [15]. If such a fault occurs, it will not be detected in the system for an extended period. In such a case, the output voltage and current of the converter will be disturbed [16]. Also, if the open-circuit fault detection time is long, it will be destructive for other parts of the converter or even for the whole system [17], [18]. Therefore, fast and accurate detection of an open-circuit fault in MMC is necessary. For this reason, several studies have been done on detecting the open-circuit fault in MMC.

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TABLE I. COMPARISON OF FAULT DETECTION METHODS

Item	***Reference***													
	[19]	***[20]***	***[21]***	***[22]***	***[23]***	***[24]***	***[25]***	***[26]***	***[27]***	***[28]***	***[29]***	**[30]**	**[31]**	***[Proposed]***
Detection	Yes		Yes			No					Yes			No
Localization			NO	Yes										
Detection time	25 µs	----	100ms	10ms	< 20 ms	----					200 µs	---		
Localization time	85 ms	5 ms	----	120 ms		300µs	150 ms	300 µs		----	200 µs	---	0.33ms	<20 ms
No. arm voltage sensors	N	N+3	N								N+1	N		N/2
No. arm current sensors	1									0	1			
cost	Medium	High	Medium											Low
Computation burden	Low	High			Medium	Low	Medium	Low		Medium	High		Very high	Low

TABLE II. COMPARISON OF SENSOR REDUCTION METHODS

Item	***Reference***									
	[35]	***[36]***	***[37]***	***[38]***	***[39]***	***[40]***	***[41]***	***[42]***	***[43]***	***[Proposed]***
No. arm voltage sensors	N			1				N/2	Number of groups	N/2
No. arm current sensors	0			1						
Fault detection	NO								Yes	
correction factor	NO				Yes					NO
Computation burden	Medium	Low		Medium	Very high			Very low	High	Low

In [20], [21], hardware-based methods are used to detect open-circuit faults. These methods are simple, but increasing the number of SMs requires additional types of equipment, which causes hardware complexity and cost increment. Recently, software-based methods have been developed to detect defective switches in MMC [21]-[31]. A sliding mode observer is used in [19] to estimate the arm current in order to identify the open-circuit fault. The defective SM is then located by the assumption-verification method. In this method, the detection time is long, and many sensors are used. In addition, the defective switch is not detectable. In [22], the Kalman filter (KF) observer estimates the circulating current and detects the open-circuit fault in the SMs. When a fault occurs in the SM switches, there will be a discrepancy between the measured and estimated values of the circulating current. In this way, The SM fault is detected by exceeding the discrepancy value from the specified threshold. The disadvantages of this method include the intricacy of the estimation algorithm, the large number of sensors, the long detection time, and inefficiency in the case of several faults. Using the MMC state-space equations and the Luenberger observer, a method for identifying a defective switch of MMC is proposed in [23]. The time required to detect fault is relatively long, and in the several faults, the proposed method cannot detect defective switches. A fast fault detection method is presented in [24] to increase the reliability of the MMC. In this method, the voltage sensors are installed parallel with the SMs upper switch, and an indicator based on Boolean logic operations is designed to identify defective switches quickly. However, the method's use of several voltage sensors, which raises system costs, is a negative characteristic. Based on capacitor voltage increases, [25] presents a method for locating faults in lower switches of SM. However, there is no solution for fault detection in upper switches. In contrast to the two-step fault detection methods [19], [22], [23], a quick method for locating defective switches is presented in [26], [27] by relocating the location of the voltage sensors of the SMs. Although fast fault detection is possible, this system is expensive and complex due to the use of a large number of voltage sensors. The idea of fault detection is used in [26], [27] in reference [28] without using arm current sensors. However, many voltage sensors are still used in the MMC. Furthermore, the removal of current sensors will

complicate the converter's control of circulating current. A new multiple open-circuit fault detection method is presented in [29], which uses the error between the measured and expected arm voltages for fault detection. The location algorithm is based on assumption-verification, which increases the computation burden to locate the defective switch in MMCs with a large number of SMs. A fault detection method based on double clamp SM (DCSM) is proposed in [30] using the higher order Bayes model (HONBM). However, in industrial applications, half-bridge SMs are mostly used, and the response of the fault detection method in half-bridge SMs is unknown. Using the Entropy of Wavelet Packets (EWP), [31] presents a fault detection method for three-level MMC, the proposed method can detect open circuit faults at high speed. However, as the number of levels increases, the calculation load increases and the detection speed decreases. Table I provides a comprehensive comparison of fault detection methods. As is well known, fault detection methods have several limitations, which are as follows: (a) The speed of detecting and locating the faulty switch is long in most methods. (b) Some methods are complicated and associated with the increased computational burden. (c) Most methods employ a large number of voltage sensors and additional components, which raises the MMC's cost.

In addition to the open-circuit fault in the switches, controlling the voltage balance of the capacitors in the MMC is regarded as a major challenge [32], [33]. The presence of a large number of capacitors in the MMC structure necessitates the use of capacitor voltage balance control methods in this converter, which has resulted in the use of a large number of voltage and current sensors in conventional control methods [34]. Recently, the idea of lowering the number of sensors in MMC has been the subject of extensive research. The comparison of sensor reduction methods is shown in Table II. The removal of arm current sensors was proposed in [35], [36], [37]. However, the removal of these sensors challenges the control of circulating current and fault detection methods. In [38], the voltage of the capacitors is estimated using one voltage sensor in each arm. This method uses the discrepancy among the measured and estimated arm voltages to estimate the capacitor voltages, but capacitor voltage estimation of MMC in high voltage applications is a challenging issue that is not considered.

In [39], [40], [41], several algorithms with correction factor capabilities, such as the adaptive linear neuron, the exponentially weighted recursive least square (ERLS), and the KF, are used to estimate capacitor voltages. These approaches require two voltage sensors in each phase branch to complete the estimate procedure. In these methods, the computational burden increases significantly as the number of SMs increases. Also, high-voltage sensors are required. In addition, on the occasion of an open-circuit fault of the switches, the voltage estimation of the capacitors will be affected, and identifying a defective switch will be challenging.

In [42], a solution to reduce the computational burden is presented using a new topology based on the half-bridge (HB) SM in which high voltage sensors are removed. Each SM consists of two HBs, but solely one voltage sensor is employed among the positive poles of the two capacitors. However, despite decreasing the number of voltage sensors and computational burden, the presented topology does not offer a solution for detecting open-circuit faults. In [43], a new method for group measurement of capacitors voltage is proposed to reduce the number of voltage sensors and detect the switches' open-circuit faults. In the proposed method, the KF algorithm is used to estimate the voltage of the capacitors, which complicates the estimation process. Also, the fault detection method uses assumption-verification, which executes it difficult to apply this method in practical applications.

This paper provides approaches for estimating capacitor voltages with fewer voltage sensors and detecting open-circuit faults in SMs. The capacitor voltages estimation method divides SMs into groups of two SMs and a voltage sensor. Consequently, the number of voltage sensors is reduced by half compared to conventional MMC measurement methods. Furthermore, the proposed estimation method is more straightforward than earlier studies and speeds up the computing process. Also, an open-circuit fault detection method based on monitoring the output voltage of the SM groups is presented to detect defective switches. The proposed method can detect an open-circuit fault in switches in less than one cycle, significantly faster than existing fault detection methods. Based on the simulation and experimental results of using the proposed fault detection method, all SM states can be monitored simultaneously, and all defective switches in different SMs can be detected.

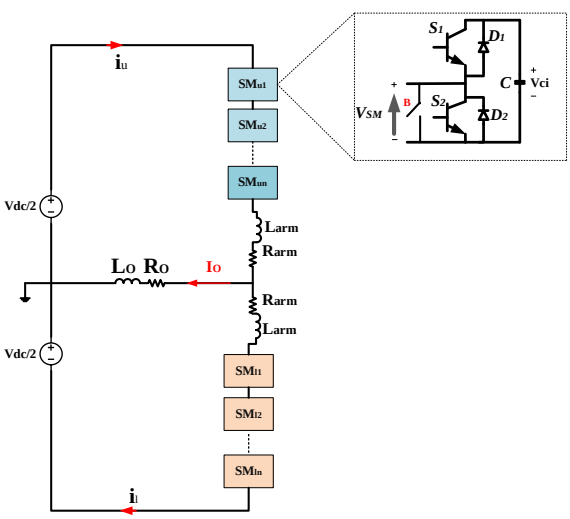


Fig. 1. MMC configuration

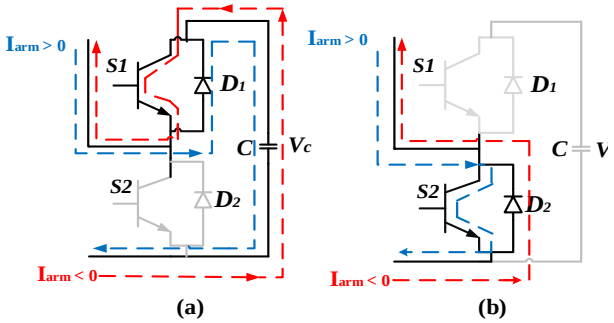


Fig. 2. Arm current paths in different switching of SM, (a) switching $S_1 = 1$, (b) switching $S_1 = 0$

TABLE III. THE SM BEHAVIOR UNDER DIFFERENT PERFORMANCE

state	I_{arm}	Capacitor behavior of the submodule		
		normal	S_1 fault	S_2 fault
S_1=1	< 0	Discharge	Bypass	Discharge
	>0	Charge	Charge	Charge
S_1=0	< 0	Bypass	Bypass	Bypass
	> 0	Bypass	Bypass	Charge

II. Topology and Normal Operation of MMC

In Fig. 1, the schematic representation of the Modular Multilevel Converter (MMC) configuration is depicted. This configuration comprises N series-connected Sub-Modules (SMs) and an inductor (L_{arm}) forming both the upper and lower arms of each phase. To model losses within the arms, a resistor (R_{arm}) is employed. Conventionally, the MMC adopts a half-bridge SM topology, characterized by two complementary Insulated Gate Bipolar Transistor (IGBT) switches, one capacitor, and two anti-parallel diodes. Additionally, a bypass switch (B) is typically integrated into the SM's output to facilitate the short-circuiting of malfunctioning SMs. In the standard SM operation mode, the arm's current paths are shown in Fig. 2. There are four different paths for arm current depending on the SM switching situation. Fig. 2 (a) shows the current paths at $S_1 = 1$ (1 stands for the on-state of a switch). In this case, if $I_{arm}>0$, the capacitor is charged, and if $I_{arm}<0$, the capacitor is discharged. The output voltage of SM is the same as the capacitor's voltage (V_c). The current paths at $S_1= 0$ (0 stands for the off-state of a switch) are shown in Fig. 2 (b). In this case, the SM is bypassed, the current sign does not affect the capacitor, and the output voltage of SM is zero.

III. Operation of SM With Open-Circuit Fault

In the topology of the half-bridge SM, two switches are employed so that there is a possibility of two classes of open-circuit faults in one SM, i.e., a fault on the upper switch (S_1) and a fault on the lower switch (S_2). The state of SM under different operating conditions is given in Table III. In the case of a fault in S_1, if $I_{arm}<0$ and $S_1 = 1$, the arm current will be forced to pass D_2 instead of S_1. In other cases, the SM behavior will be the same as normal operation. In this way, the capacitor will not have a chance to discharge, and the voltage of the defective SM capacitor will always be higher than other SMs. In the occurrence of the fault in S_2, when $I_{arm} > 0$ and $S_1 = 0$, the arm current will pass through D_1 instead of S_2. Therefore, in an S_2 fault, the capacitor charging time will be longer than the discharge. In other cases, the flow path is similar to the normal operation of the SM. In this way, the voltage of the defective SM capacitor is higher than the other SMs in both fault modes. According to Table I, the fault detection in S_1 and S_2 is not simultaneous and requires the specified conditions to be met.

IV. Sensor Configuration and Proposed Fault Detection Method

A. Configuration of Voltage Sensors and Group Measurement of Capacitor Voltages

For normal MMC operation, it is critical to sustaining the SM capacitors' voltage balance. Achieving this goal requires instantaneous information about the capacitor voltages. Hence, the existence of many voltage sensors is mandatory for balancing the capacitor voltages in usual control methods. As a result, the system's intricacy and expense will rise as the number of measuring components increases. In this study, a new scheme for group measurement of the capacitor voltages is proposed to reduce the voltage sensors. The proposed scheme's configuration of voltage sensors is depicted in Fig. 3(a), where each arm is divided into groups consisting of two SMs. Individual sensors are eliminated from the capacitors, and one voltage sensor is installed at the output of each group as the group monitoring sensor. Each group's capacitor voltages are estimated using the group monitoring sensor for the capacitors voltage balancing. Also, by comparing monitoring sensor values across consecutive sampling times, the open-circuit defect can be detected. Fig. 3 (b) displays the *ith* (i = 1, 2, …, N/2) group in the MMC, which is comprised of two HBs (HB_{i1} and HB_{i2}) connected in series. The HB_{ij} (j = 1, 2) consists of one capacitor (C_{ij}) and two switches (S_{uij}, S_{lij}), and the switches gate signal is controlled by the switching function S_{ij}.

The basic equations for implementing the group measurement method with fewer voltage sensors are mentioned in (1) to (6). The mathematical model of the proposed estimation method is created using simple equations based on switching signals and capacitors voltage. In this way, the value of the monitoring sensor in each group is as follows:

$$V_{G_{u,l}i} = V_{HB_{i1}} + V_{HB_{i2}} \quad (1)$$

where $V_{Gu,li}$ is the voltage of the group, V_{HBij} is the voltage of HB_{ij}. The group estimated voltage $\hat{V}_{G_{u,l}(i)}$ equals the summation of HB_{ij} estimated

voltages. The voltage of each HB_{ij} can be written based on the estimated capacitor voltage of each SM ($\hat{V}_{Cij}$) and its switching state (S_{ij}). Hence, the output voltage of each group can be written as:

$$\hat{V}_{G_{u,l(i)}} = S_{i1}\hat{V}_{ci1} + S_{i2}\hat{V}_{ci2} \quad (2)$$

By rewriting (2) based on discrete sampling time, all variables have been changed based on time step x as follows:

$$\hat{\mathrm{V}}_{\mathrm{G_{u,l(i)}}}(\mathrm{x}) = \mathrm{S_{i1}}(\mathrm{x})\hat{\mathrm{V}}_{\mathrm{ci1}}(\mathrm{x}) + \mathrm{S_{i2}}(\mathrm{x})\hat{\mathrm{V}}_{\mathrm{ci2}}(\mathrm{x}) \quad (3)$$

Estimating capacitor voltages in each sample time requires the estimated group voltage discrepancy. The group voltage discrepancy in step *k* is calculated using the estimated capacitor voltages of step *k-1*, which have been stored in an algorithm memory, and the measured value of the monitoring voltage sensor in step *k*:

$$\widehat{\Delta V}_{G_{u,l(i)}}(k) = V_{G_{u,l(i)}}(k) - \sum_{j=1}^{2} S_{ij}(k-1)\hat{V}_{cij}(k-1) \quad (4)$$

The voltage of the capacitors used in a group voltage construction has been changed by flowing current through them. The new voltage of each capacitor in a group $(\hat{V}_{ci1}(k), \hat{V}_{ci2}(k))$ is estimated by dividing the group voltage variation $(\widehat{\Delta V}_{G_{u,l(i)}}(k))$ between the capacitor voltages of the last step $(\hat{V}_{ci1}(k-1), \hat{V}_{ci2}(k-1))$. Hence, the capacitor voltages in step k are estimated as follows:

$$\hat{\mathrm{V}}_{\mathrm{ci1}}(\mathrm{k}) = \hat{\mathrm{V}}_{\mathrm{ci1}}(\mathrm{k\text{-}1}) + \left[\frac{\mathrm{S_{i1}(k\text{-}1)}}{\mathrm{S_{i1}(k\text{-}1)+S_{i2}(k\text{-}1)}}\right]\widehat{\Delta \mathrm{V}}_{\mathrm{G_{u,l(i)}}}(\mathrm{k}) \quad (5)$$

$$\hat{\mathrm{V}}_{\mathrm{ci2}}(\mathrm{k}) = \hat{\mathrm{V}}_{\mathrm{ci2}}(\mathrm{k\text{-}1}) + \left[\frac{\mathrm{S_{i2}(k\text{-}1)}}{\mathrm{S_{i1}(k\text{-}1)+S_{i2}(k\text{-}1)}}\right]\widehat{\Delta \mathrm{V}}_{\mathrm{G_{u,l(i)}}}(\mathrm{k}) \quad (6)$$

Therefore, using (5) and (6), the present voltage of both capacitors in a group is estimated by the latter sample time (*k-1*) capacitor voltages and switching signals. In the estimation process, two essential features help the stability of the system and control the estimation error as follows:

Feature 1: One SM activation in the groups (HB_{i1}=0 & HB_{i2}=1 or HB_{i1}=1 & HB_{i2}=0)

When the modulator sends the command to produce one voltage level in each group, just one capacitor cooperates in the voltage generation. In this operation, the monitoring voltage sensor measures the capacitor voltage directly, which is exactly the same as the estimated value. Therefore, the estimation error in each cycle converges to zero, and the cumulative error will be eliminated.

When the capacitor estimated voltages depart from the standard range, the sorting process tries to bring them back within the acceptable sorting range and minimize the deviation between the estimated and measured voltages. In the case of incremental estimation error, when the capacitor's estimated voltage is greater than the measured value, the capacitor only participates in the switching process with the negative arm current. In this case, the capacitor voltage decreases and nears the measured value. In the decreasing estimation error, when the estimated voltage of one capacitor is lower than the measured value, the capacitor only participates in the switching process with the positive arm current, and its voltage is raised. Therefore, the capacitor voltages will be balanced and never exceed the standard range using the sorting process.

Feature 2: Balancing of estimated voltages with the sorting process

As a result, the estimation procedure is done with the straightforward process of dividing the voltage difference equally among the capacitors participating in a switching operation. Additionally, with the two features mentioned above, the estimation error in each sampling time is converged to zero, and capacitor voltage balancing is done with fewer voltage sensors.

B. Proposed Fault Detection Method

This section identifies the defective switch in MMC using an optimized fault detection process with reduced voltage sensors. According to Fig. 3 (b), the MMC arms are divided into several groups consisting of two SMs with the proposed sensor reduction scheme. The proposed fault detection algorithm constantly searches for the defective switches in each group. The fault detection process is Considering the arm's current sign (I_{arm}), the voltage accomplished by comparing the group voltage ($V_{Gu,l}i$) in normal and faulty operation modes. According to the information in Table III, finding the fault in the special switch depends on the activation of one SM in the group. In this case, the group monitoring sensor measures the capacitor voltage of the active SM. When a fault occurs in a switch, there is a difference between the measured and predicted voltage, and the defective switch can be detectable.

Fig. 4 shows the algorithm flowchart, where the algorithm starts by activating one SM in the group. measured by the group monitoring sensor is compared with one of the voltage thresholds (V_{thmin}, V_{thmax}). In the proposed algorithm, the lower (V_{thmin}) and upper (V_{thmax}) equal $\frac{1}{2}V_{ref}$ and $\frac{3}{2}$Vref, and V_{ref} is the capacitor balancing voltages ($\frac{V_{dc}}{N}$). According to different states in Table IV, if the $V_{Gu,l}$(i) exceeds the threshold values, the fault can be detected in different switches. Moreover, the fault counter (n_{iz}, z=1,2,3,4) has been prepared in the algorithm to prevent the detected faults caused by measuring noise. If the fault is

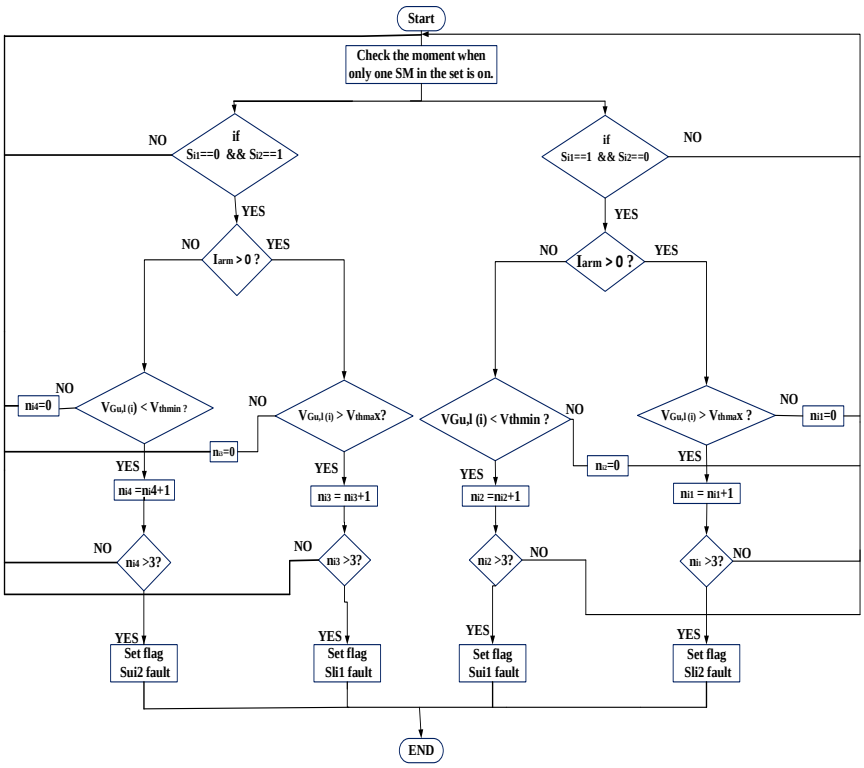


Fig. 4. Flowchart of the proposed fault detection method.

TABLE IV. EFFECT OF SWITCH FAULT ON GROUP OUTPUT VOLTAGE IN DIFFERENT SWITCHING STATES

status			$V_{Gu,l}\,i$				
S_{i1}	S_{i2}	I_{arm}	*Normal state*	*Open-circuit fault*			
				S_{ui1}	S_{li1}	S_{ui2}	S_{li2}
1	1	>0	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$
		<0	$V_{ci1}+V_{ci2}$	V_{ci2}	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$	$V_{ci1}+V_{ci2}$
1	0	>0	V_{ci1}	V_{ci1}	V_{ci1}	V_{ci1}	$V_{ci1}+V_{ci2}$
		<0	V_{ci1}	0	V_{ci1}	V_{ci1}	V_{ci1}
0	1	>0	V_{ci2}	V_{ci2}	$V_{ci1}+V_{ci2}$	V_{ci2}	V_{ci2}
		<0	V_{ci2}	V_{ci2}	V_{ci2}	0	V_{ci2}
0	0	>0	0	0	V_{ci1}	0	V_{ci2}
		<0	0	0	0	0	0

repeated three times, the counter approves the open-circuit fault in the system. The proposed method is implemented identically for all groups, and the algorithm can quickly detect several faulty switches while the number of voltage sensors has been significantly decreased.

V. SIMULATION STUDIES

To assess the viability of the proposed design, a single-phase MMC featuring 14 SMs in each arm is simulated in the MATLAB/Simulink environment. The modulation of the MMC switches is achieved using the phase-carrier-shift (PSC)-PWM modulation method. Key system parameters and threshold values are compiled in Table V. The efficacy of the proposed method is scrutinized across various scenarios, as elaborated in the subsequent cases.

A. Evaluation of proposed scheme under normal condition

Fig. 5 illustrates the performance of the converter employing the proposed scheme under normal conditions, with a constant R-L load applied. In Fig. 5(a), the MMC output voltage and current are displayed, featuring 15 voltage levels in the output voltage and a smooth waveform in the output current. The voltage waveform of the upper and lower arm capacitors is presented in Fig. 5(b), showcasing well-balanced capacitor voltages at the reference value of 2000 V. Fig. 5(c) exhibits the measured and estimated values of the capacitor voltage C_{u1} (the capacitor of the first SM of the upper arm), demonstrating that the estimated value appropriately tracks the measurement. The estimation error of the capacitor voltage

TABLE V. CRITICAL PARAMETERS OF SIMULATION AND EXPERIMENTAL STUDIES

PARAMETER		***Simulation values***	***Experimental values***
Capacitance (C_{ij})		6.8 mF	1.5 mF
DC Link Voltage (V_{dc})		28 kV	120 V
Modulation index (m_a)		0.95	0.85
Fundamental frequency (f)		50 Hz	50 Hz
Switching frequency (f_s)		1 kHz	500 Hz
Number of SM per arm (N)		14	4
Arm inductor (L_{arm})		5.5 mH	4.9 mH
Load	inductor (L_o)	15 mH	17 mH
	Load resistor (R_o)	30 Ω	30 Ω
Sampling period		1e-5 Sec	2e-4 Sec
V_{thmax}		42 kV	45 V
V_{thmin}		14 kV	15 V

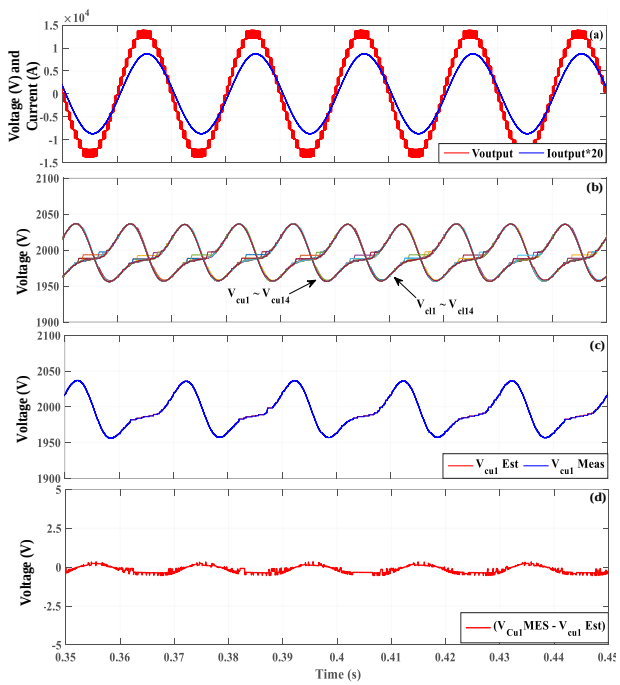


Fig. 5. Performance of the proposed scheme in normal conditions. (a) output voltage and current, (b) upper and lower arm capacitor voltage, (c) measured and estimated voltage V_{cu1}, (d) error of the estimated capacitor voltage V_{cu1}.

V_{cu1} (measured value minus estimated value) is depicted in Fig. 5(d), and its minimal value confirms the efficacy of the proposed scheme. Consequently, the simulations affirm that reducing the number of sensors does not compromise the normal performance of the converter.

B. evaluation of the proposed scheme with deviation in capacitance, and modulation index change

To further investigate the proposed scheme, the capacitance of the upper arm capacitors is simulated in a wide range of deviations. The capacitance deviation values of C_{u1} ~ C_{u14} are selected as follows: -30%, +5%, -7%, -10%, +10%, +5%, -15%, -12%, -6%, +13%, +20%, -3%, +7%, and +20% which results in the values of Cu1~Cu14 as: 4790 µf, 7140 µf, 6324 µf, 6120 µf, 7480 µf, 7140 µf, 5780 µf, 5984 µf, 61392 µf, 7684 µf, 8160 µf, 6596 µf, 7276 µf, and 5440 µf, respectively. Also, the modulation index decreases to 0.7 at t = 0.5 s. The simulation results, in this case, are shown in Fig. 6 and Fig. 7. The output voltage and current waveform under these conditions are shown in Fig. 6. The output voltage initially creates 15 voltage levels well, and after decreasing the modulation index, the number of levels has reduced to 11 levels. The output current waveform is completely sinusoidal, and after decreasing the modulation index, the value of output current has decreased. Fig. 7 (a) shows the voltage across the upper arm capacitors. The voltage ripple of the capacitors has slightly increased due to large deviations in the capacitance of the capacitors. However, the capacitors remain well balanced in their reference value. Capacitor voltage waveform V_{cu1} is shown in Fig. 7 (b) that despite a 30% deviation in capacitance, the estimated voltage value follows the measured value. Also, Fig. 7 (c) shows the voltage estimation error of capacitor V_{cu1}, which has increased due to deviation in capacitance. According to the results of Fig. 6 and Fig. 7, the presence of deviations in the capacitance of capacitors, MMC performance, was not significantly affected. On the other hand, such large deviations in capacitance (e.g., -30%) are unlikely in practical applications.

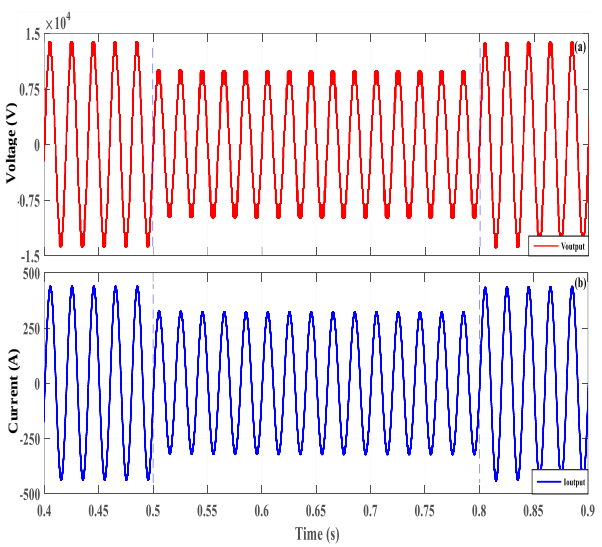


Fig. 6. Performance of the proposed scheme by changing the modulation index and deviation in the capacitance of the upper arm capacitors. (a) output voltage, (b) output current.

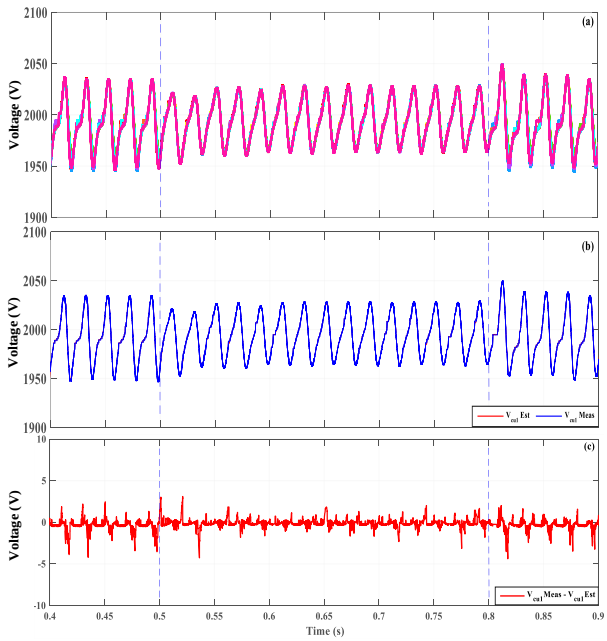


Fig. 7. Performance of the proposed scheme by changing the modulation index and deviation in the capacity of the upper arm capacitors. (a) upper arm capacitor voltage, (b) measured and estimated voltage V_{cu1}, (c) errors of the estimated capacitor voltage V_{cu1}

C. *Evaluation of proposed scheme with open-circuit fault*

The effectiveness of the proposed fault detection method is assessed by inducing open-circuit faults on different switches. At t = 0.4s, an open-circuit fault occurs at the upper switch SM_{u1} (S_{u11}). The simulation results, depicted in Fig. 8 and Fig. 9, underscore the efficacy of the proposed method. Specifically, Fig. 8(a)-(b) portrays the output voltage and current, as well as the arm current, respectively, post the fault occurrence. As anticipated, the output voltage and current experience disruptions and reductions, and the arm current are entirely diverted. In Fig. 8(c), the voltage of the upper arm capacitors is presented. Following the fault in S_{u11}, the capacitor voltages deviate from the reference value, with the defective SM capacitor exhibiting an increase compared to the others. Fig. 9 illustrates the performance of the proposed fault detection method, showcasing switching commands for group G_{u1} (S_{11} and S_{12}) at the fault detection moment in Fig. 9(a) and (b). Fig. 9(c) confirms the proposed method's accurate detection of the defective switch in the upper arm, with a fault detection time of t = 0.41245s, affirming its speed and accuracy in identifying faulty switches.

Fig. 10 displays the assessment results of the proposed fault detection method under an open-circuit fault on the SMu2 lower switch (S_{l12}). The outcomes reveal disturbances in the output voltage and current due to a failure in one of the switches. As illustrated in Fig. 10(b), the arm currents are entirely disrupted owing to power

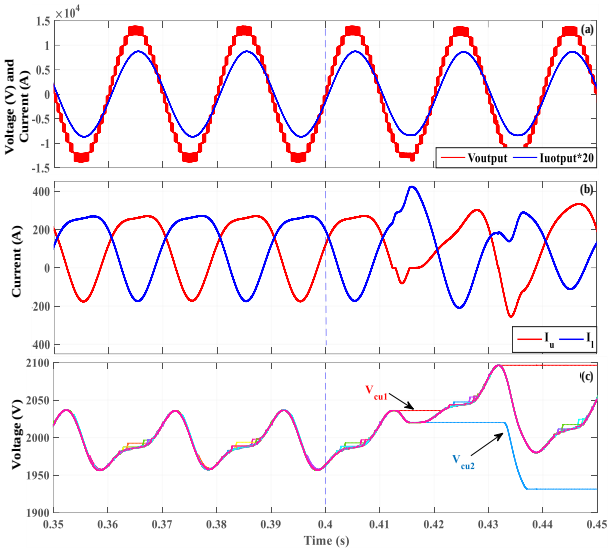


Fig. 8. Performance of the proposed scheme with lower switch fault (a) output voltage and current, (b) upper and lower arm current, (c) upper arm capacitor voltage.

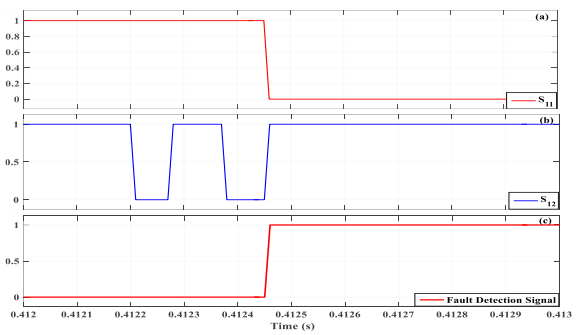


Fig. 9. Performance of fault detection method with a fault in the upper switch (a) switching command signal S_{11}, (b) switching command signal S_{12}, (c) fault detection signal.

imbalances in the arms. Moreover, the capacitor voltage of the defective SM experiences an increase. Fig. 11 demonstrates the performance of the proposed fault detection method in the presence of a fault on S_{l12}. The switching commands for the G_{u1} group are presented in Fig. 11(a) and (b) of the proposed scheme. The fault detection signal in Fig. 11(c) indicates that the proposed method accurately detects the defective switch at t = 0.40004s.

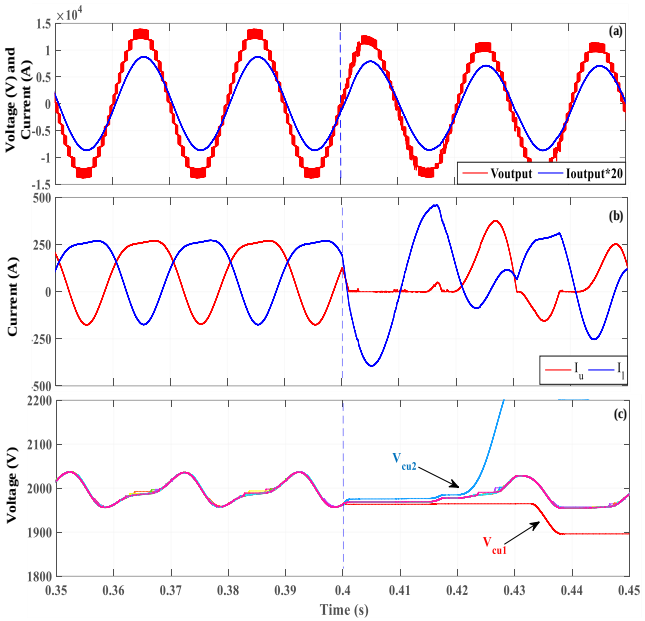


Fig. 10. Performance of the proposed scheme with lower switch fault. (a) output voltage and current, (b) upper and lower arm current, (c) upper arm capacitor voltage.

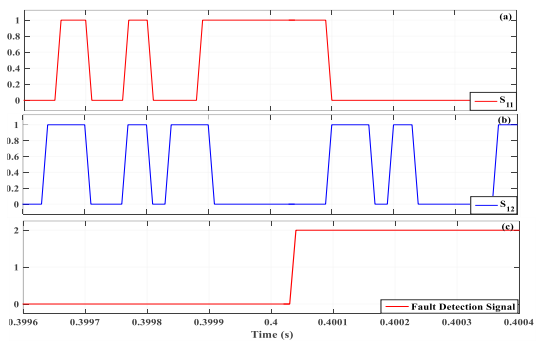


Fig. 11. Performance of the fault detection method a fault in the upper switch. (a) switching command signal S_{11}, (b) switching command signal S_{12}, (c) fault detection signal.

VI. Experimental Studies

For practical validation of the proposed approach, a laboratory prototype of a single-phase MMC with four SMs per arm has been constructed. The components of the laboratory prototype are illustrated in Fig. 5. IRF640N semiconductor switches are employed in the SMs, and the converter is controlled by a DSP TMS320F2812 microcontroller, which also executes the proposed scheme. The key parameters of the laboratory prototype are detailed in Table V.

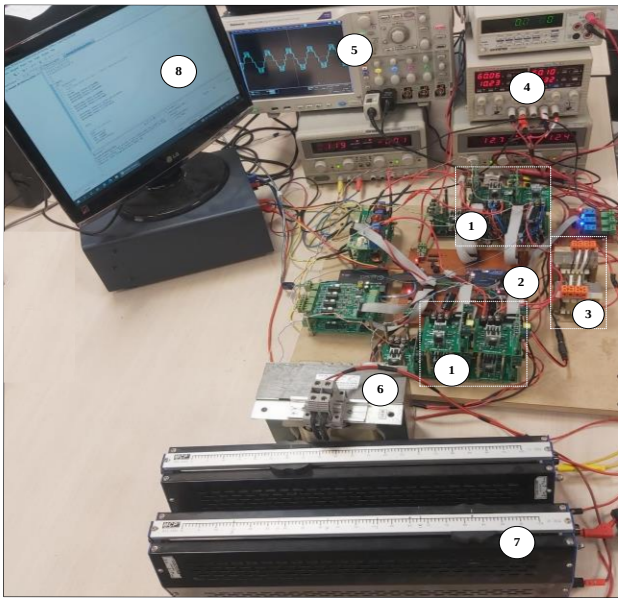


Fig. 12. Experimental topology of single-phase MMC (1) upper and lower arm, (2) DSP tms320F2812, (3) arm inductor, (4) DC source, (5) oscilloscope, (6) load inductor, (7) load resistor, (8) computer.

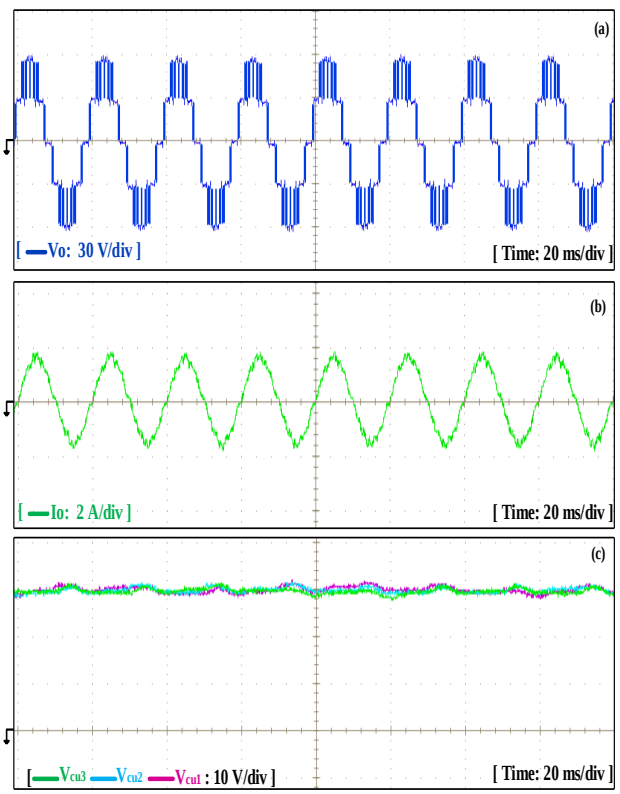


Fig. 13. Experimental results of MMC, under normal conditions (a) AC output voltage, (b) AC output current, (c) upper arm capacitor voltage.

A. Evaluation of proposed scheme under normal conditions

The experimental outcomes under normal conditions are presented in Fig. 13. In Fig. 13(a), the AC output voltage is shown with five levels. Fig. 13(b) displays the output current of the converter, featuring a sinusoidal shape. The voltages of the upper arm capacitors, illustrated in Fig. 13(c), demonstrate a well-balanced state at the reference value of 30V. According to the findings in Fig. 13, it is verified that the proposed scheme does not have a detrimental effect on the normal operation of the MMC.

B. Evaluation of proposed scheme with modulation index change

The experimental results of the proposed scheme are illustrated in Fig. 14, wherein the modulation index is varied from 0.85 to 0.4. In Fig. 14(a) and (b), the output voltage and current are depicted, revealing a reduction to 3 levels in the output voltage and a corresponding decrease in the output current after the modulation index reduction. Fig. 14(c) demonstrates that, despite the modulation change, the voltages across the upper arm capacitors continue to remain balanced.

C. Evaluation of proposed scheme with load change

The experimental outcomes with a sudden load change are presented in Fig. 15. Notably, the output current experiences a decrease following an abrupt increase in load impedance. Nevertheless, the voltages across the capacitors, as depicted in the figure, remain balanced. This observation underscores the effective performance of the proposed scheme under dynamic load conditions.

D. Evaluation of proposed scheme open-circuit fault

The fault detection algorithm relies on the identification of open-circuit faults through a comparison of group voltage output in normal and fault conditions. To validate this approach, an open-circuit fault is induced at time t_0 by manipulating the upper switch of SM_{u4}. This disruption affects the output current and voltage, as well as the voltage balance of the capacitors in the upper arm. The upper arm current is also impacted, and the proposed fault detection method successfully identifies the fault on the upper switch within 20ms, as illustrated in Fig. 16.

The experimental outcomes of applying single open circuit faults to three switches are outlined in Table VI (the fault time is consistent across all cases). As evident, the detection time of defective switches varies based on the switching status.

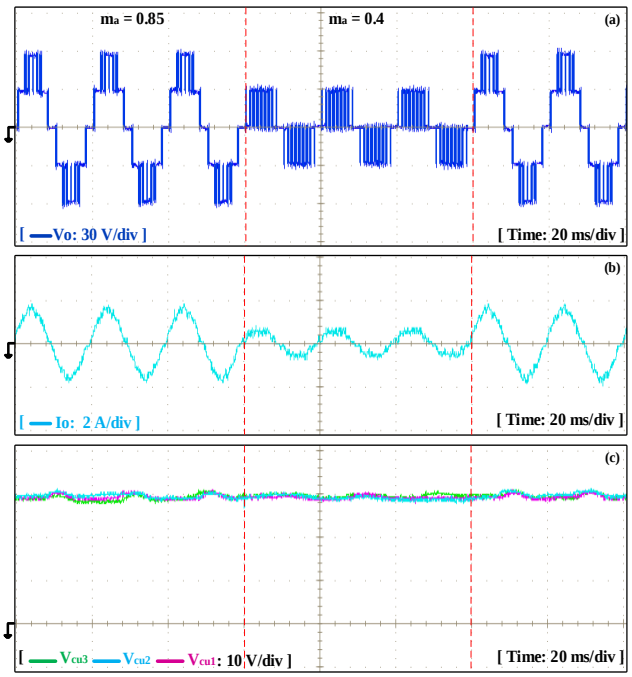


Fig. 14. Experimental results of MMC with changing the modulation index. (a) AC output voltage, (b) AC output current, (c) upper arm capacitor voltage.

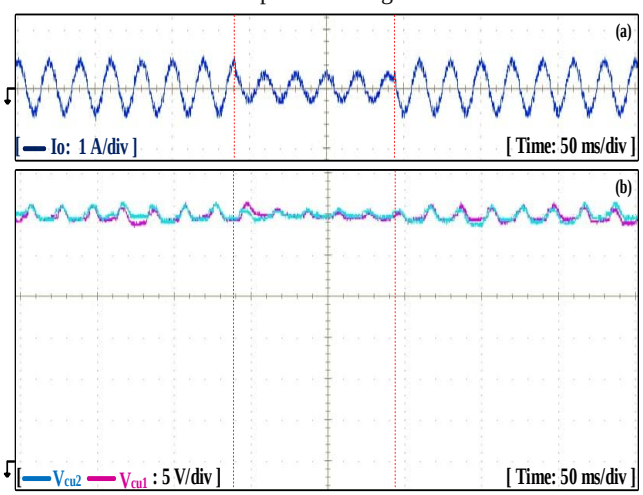


Fig. 15. Experimental results of MMC with a sudden increase in load impedance from 50% to 100% (a) AC output Current, (b) upper arm capacitor voltage.

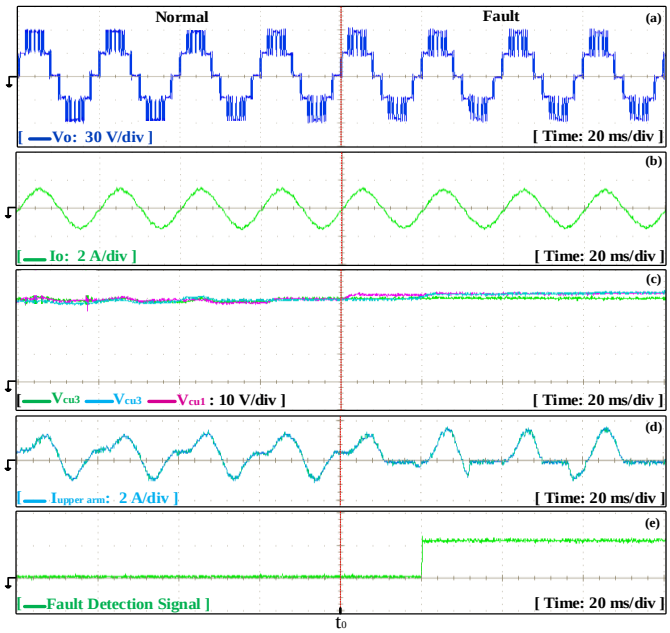


Fig. 16. Performance of the fault detection method with the occurrence of a fault in the upper switch. (a) AC output voltage, (b) AC output Current, (c) upper arm capacitor voltage, (d) upper arm current, (e) fault detection signal.

Table VI. EXPERIMENTAL RESULTS OF FAULT DETECTION

Location	*Detection time (Δt)*
SM_{u1} lower switch	6.2 ms
SM_{u2} upper switch	11.8 ms
SM_{u3} lower switch	9.8 ms

VII. Conclusion

This study introduces a technique aimed at diminishing the number of voltage sensors within SMs of MMC, with a specific focus on open-circuit fault detection. The approach involves halving the total number of voltage sensors through the reorganization of arm submodules and the estimation of capacitor voltages. This reduction in voltage sensors not only cuts down on system costs and complexity but also contributes to an enhancement in system reliability. Furthermore, in the estimation of capacitor voltages, the leverage of circuit relations governing MMC's topology is employed to alleviate computational burdens. The proposed method for fault detection involves a comparison of output voltages from each group of SMs under normal and defective conditions. This streamlined process enables the swift and straightforward identification of an open-circuit fault, surpassing the speed of many preceding methods. The fault detection method achieves remarkable accuracy, identifying open-circuit faults in less than one cycle. This swift detection significantly bolsters system reliability, rendering it more resilient for industrial applications. The proposed scheme exhibits potential for extension to a three-phase structure and is currently under investigation for future research endeavors.

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