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Advanced Inrush Current Mitigation Techniques for Microprocessor-Less High Power AC/DC/DC Synch-Buck Converters: A Start-up Perspective

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ABSTRACT

This paper investigates the starting current of an AC/DC/DC converter, consisting of a three-phase diode bridge rectifier and a synchronous buck converter. The use of microprocessors in such converters increases the total cost and also reduces reliability due to EMI phenomena. For this reason, by removing the microprocessor, a start-up plan including a limiting starting resistor and then soft starting the switching module is proposed in this paper. By modeling the system under different operating modes, a solution is presented to minimize the circuit startup period, which includes minimizing the bypass time of the startup resistor and reducing the switching soft startup period as possible. The proposed method has been implemented on a 15-kW converter feeding from a three-phase 380 V power grid and provides up to 300 V_{dc}/50 A_{dc} to supply an electroplating pool. The results show that the sequential startup procedure, including using a 50 ohm/1500 w resistor for 3 seconds, and then bypassing it, then soft start switching after half a second and during 1.5 s, can move this circuit to a steady state in 5 seconds, keeping current in all parts below half rated current.

NOMENCLATURE

D_n	The final value of pulse width	V_m	Phase voltage peak value
f_n	The fundamental frequency of the power grid	V_S	Three-phase input voltage
fs	Switching frequency	α	Damping factor
Ip	C_1 Charging peak current	ω	Angular frequency of the power grid
T	Pulse-signal period	ω_0	Resonance frequency
t_0	The end time of the first phase	ω_n	Damped natural frequency
t_f	The end time of the second phase	V_m	Phase voltage peak value
t_p	The time when the current reaches its peak value in the second phase		
t_s	The time variable from the moment of triggering the main switches		
Δt_{ss}	Soft-start interval		
V_F	Capacitor steady-state voltage in each phase		
V_{in}	Diode bridge output voltage		

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I. INTRODUCTION

Switching power supplies are widely used due to their high efficiency, compact size, and low weight. At lower power levels, higher switching frequencies (above 40kHz) allow the use of smaller inductors and capacitors. However, at high power levels, limitations of semiconductor devices necessitate lower switching frequencies. Larger inductors are then required, increasing costs. To mitigate this, lower inductance is utilized along with higher capacitor values. However, the resulting inrush current during start-up can damage semiconductors, circuitry, and capacitors. Methods to limit inrush current are thus needed which can be open or closed loop operation. While closed-loop operation enhances regulation, it necessitates a microprocessor for control. Without a microprocessor, staged start-up and shutdown procedures become challenging so a careful design is required to manage inrush current and transients during mode transitions without digital control capabilities. Overall, optimizing the switching topology and control scheme requires balancing frequency and component selections against complexity, performance, and cost.

Among the techniques that have been investigated in recent studies for AC-DC converters, the modulation method is based on an analytical expression for the MB-DAB half-bridge, which can be directly implemented on a microprocessor proposed in [1]. It can achieve almost full ZVS cycle brightness of all MOSFETs and unity power factor. Also, an overview of the power imbalance problem and the analysis of its reducing control technique for two-phase and single-phase isolated MVAC-LVDC converters have been discussed in [2]. To achieve zero voltage switching (ZVS) in the full range of AC current, a combined phase shift and frequency modulation scheme of a double active bridge AC-DC converter (DAB) is presented in [3]. A directly applicable closed-form analytical solution for an efficient zero-voltage switching (ZVS) modulation scheme for DAB converters is also presented to minimize conduction losses under ZVS conditions [4]. A technique to limit the inrush current of an AC/DC converter is introduced in [5], where the DC bus capacitor voltage is gradually increased to limit the charging current.

Among the widely used strategies for limiting the inrush current in DC-DC converters, modulation control topologies can be mentioned. Similarly, PWM mask [6] and investigating domain response of the system during start-up [7] have been introduced

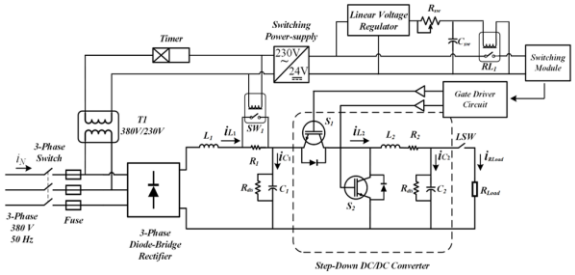


Fig. 1. Diagram of the under-study power circuit

in this field. Also, as a new technique, a soft start modulation method is presented by Sante Pugliese et al. where a fast voltage balancing control is hired to prevent overvoltage and unbalanced voltage conditions [8]. Other soft start techniques include the methods of using auxiliary circuits to improve starting and limiting components [9, 10]. Despite the effectiveness, reliability, and efficiency of these procedures in limiting the current and achieving short start-up times, they are generally used at low power levels due to high working frequency, and their main limitation is their applicability in high powers. In addition, the use of an auxiliary circuit will increase the need for additional parts like sensors, power supplies, etc., and of course, the final cost of the circuit.

Digital control schemes are also widely used to control inrush current in power converters including start-up response analysis or introducing digital soft-start circuits [11], [12]. Other control methods reviewed in the literature, are (VRSPV) [13] and (AGC) [14], which can provide soft-start without using high frequency and shorten converter settle time, respectively.

To design a control algorithm, a new feeding strategy for a three-phase modular multilevel converter is proposed in [15]. Also, the control scheme based on passive communication and improved damping allocation is proposed in [16], which is used to adjust the dynamic characteristics of the system. In another approach, an offset-free model predictive control (MPC) has been proposed for a buck converter feeding a constant power load (CPL) [17]. Although prior literature references provide practical and accurate designs, due to the need to use microcontrollers and microprocessor-based auxiliary circuits, the limitation of implementing these methods at high power levels cannot be ignored.

Another common control method is presented as a sliding mode control for efficient LLC resonant DC-DC converters in EV chargers, optimizing size and cost that achieves a notable peak efficiency [18]. Additionally, an integrated bidirectional

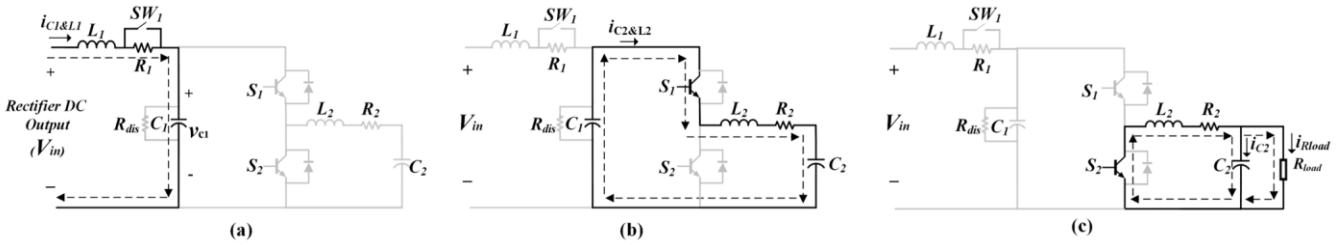


Fig. 2. The equivalent system circuit for a) phase 1, b) phase 2, c) phase 3

multiport DC-DC converter for plug-in EV charging, employing a half-bridge CLLC converter, ensures effective battery charge control and stable DC-link voltage [19]. A. Nabieh et.al proposed a simplified optimal path control (SOTC) to control a 1 MHz LLC converter. By implementing the proposed model, the optimal transient performance can be achieved and the settling time can be minimized [20]. Other soft start methods include the pulse jump control scheme to prevent inrush current and output voltage during the start-up period of DC-DC converters, which was presented by Pang-Jung Liu. [21]. Also, to eliminate the current and voltage stress in the resonance cycle during the soft start process, this process has been optimized based on the path condition analysis [22]. In another study, the differential evolution (DE) method was used to extract the parameters of the dynamic model of a converter, which is used to predict and model the inrush current phenomenon [23].

As mentioned, the precision regulation afforded by microprocessor-based digital control enables optimally efficient closed-loop operation in power supplies. However, at high power levels, microprocessor limitations can impede efficiency. The supplementary circuitry required further elevates complexity and expenditures. For applications without stringent regulation prerequisites, open-loop operation may suffice and eliminate the microprocessor. Devoid of a microprocessor, staged power-up and power-down sequences become challenging endeavors. Safely transitioning through these sequences without inrush currents necessitates meticulous design. Overall, the advantages of digital control must be weighed against its limitations at high power. Selecting topology and control schemes requires optimization across performance, complexity, and cost. Open or closed-loop configurations can be chosen to accommodate requirements while balancing capabilities, efficiency, and cost.

The focus of this paper is to provide a simple and efficient technique to restrict the inrush current in an industrial high-power AC/DC/DC converter. The circuit architecture includes a bridge rectifier, an LC filter, and a synchronous buck converter. The proposed start-up procedure includes three different phases, the pre-charge phase, the full charge phase, and the soft start switching phase.

This way, the converter moves from the zero initial state to the load connection state under nominal voltage, without any damaging inrush and transient.

II. SYSTEM MODELING

Fig. 1 shows the general outline of the system under study. At the input of the power circuit, a three-phase diode bridge and an LC filter consisting of an inductor L_1 and a capacitor bank with a total capacitance of C_1 are used. To limit the capacitor charging current, starting resistor R_1 is used, and to bypass this resistor, the contactor switch SW_1 is implemented in parallel with it. The power semiconductor switches of this circuit are S_1 and S_2, respectively, which usually come in a double-IGBT module. Considering that this converter operates in synchronous mode, both switches trigger with complementary pulses. Also, a high-frequency inductor L_2 has been used at the output of the power module and a capacitor set at the output of the converter with a total capacitance of C_2. It should be mentioned that using a diode bridge leads to undesirable harmonic content. If the THD and harmonic content of the AC side current should satisfy specific standards, using an additional Power-Factor-Correction circuit is recommended.

Fig. 1 also shows the proposed sequential start-up control circuit. A timer module activates the SW_1 contactor switch and the switching power supply. Then a linear regulator, feeding an $R_{SW}C_{SW}$ delay circuit, makes a tunable delay between activating SW_1 and relay switch RL_1. Closing RL_1 activates the switching module, which starts softly, in the pre–tuned time interval. This way, the start-up process of the power circuit consists of three different phases as follows:

A- The Pre-Charge phase

This phase starts from the moment the circuit is energized by connecting the three-phase switch 3phsw in Fig.1 and continues until the switch SW_1 is closed at $t=t_0$ by the timer module activation in Fig. 1. During this period, the capacitor C_1 is charged from the three-phase power supply, and the limiting resistor R_1, along with the inductor L_1, are in its current path. In this working mode, the switches S_1 and S_2 are both kept off, so the circuit is unloaded, and the capacitor C_2 remains uncharged. The equivalent circuit of the system in this working mode will be in the form of Fig. 2(a). Based on the maximum permissible current in this phase; the R_1 value will be:

$$R_1 = \frac{Vin}{Ip} \tag{1}$$

To determine the power rating of this resistor, the current RMS value and total power consumption will be:

$$i_{C1,rms} = \sqrt{\frac{1}{t_0}\int_0^{t_0} i^2(t)dt} \tag{2}$$

$$P = R_1 \cdot (i_{C1rms})^2 \tag{3}$$

The RLC loop current is equal to:

$$i_{C1} = C_1 \frac{dV_{C1}}{dt} \tag{4}$$

From Fig. 2(a), the KVL low gives:

$$L_1 \frac{dV_{C1}}{dt} + R_1 i_{C1} + V_{C1} = V_{in} \tag{5}$$

Considering that the value of the ripple coefficient of the output voltage of the three-phase diode rectifier is so negligible that it can be ignored, therefore, the value of V_{in} can be assumed to be constant in the upcoming calculations for the investigated circuit (cf. [24]). Also, the draining resistance of the R_{dis} capacitor bank is selected to a large extent so that it does not affect the circuit's performance. For this reason, this resistance is ignored in the calculations. By inserting (4) in (5), the differential equation is obtained as follows:

$$\frac{d^2V_{C1}}{dt^2}+\frac{R_1}{C_1}\frac{dV_{C1}}{dt}+\frac{V_{C1}}{L_1C_1}=\frac{V_{in}}{L_1C_1} \quad (6)$$

The roots of the characteristic equation will be calculated as:

$$s_{1,2}=-\frac{R_1}{2L_1}\pm\sqrt{\left(\frac{R_1}{L_1}\right)^2-\frac{4}{L_1C_1}} \quad (7)$$

$$\Rightarrow s_{1,2}=-\alpha\pm\sqrt{\alpha^2-\omega_0^2}$$

$$\alpha=\frac{R_1}{2L_1} \quad (8)$$

$$\omega_0=\frac{1}{\sqrt{L_1C_1}} \quad (9)$$

If $\alpha > \omega_0$ will give:

$$V_C(t)=V_F+k_1e^{s_1t}+k_2e^{s_2t} \quad (10)$$

And for $\alpha = \omega_0$:

$$V_C(t)=V_F+k_1te^{-\alpha t}+k_2e^{-\alpha t} \quad (11)$$

For $\alpha < \omega_0$, the general form of the output voltage is:

$$V_C(t)=V_F+e^{-\alpha t}\left(k_1cos_nt+k_rsin_1\omega_nt\right) \quad (12)$$

Now the current equation can be driven using (1). R_1 is selected in a range that makes $\alpha > \omega_0$ to have a stable response. To determine k_1 and k_2 in (10), considering $V_{C1}(0) = 0$ and $I_{C1}(0) = 0$ in (10) gives:

$$V_{C1}(0)=V_F+k_1+k_2 \quad (13)$$

Using (1), the inductor L_1 current will be:

$$i_{C1}=i_{L1}=\left(k_1s_1e^{s_1t}+k_2s_2e^{st}\right)C_1 \quad (14)$$

Considering its initial state, (14) will give the following:

$$i_{L1}(0)=\left(k_1s_1+k_2s_2\right)C_1 \quad (15)$$

$$k_1=-(V_F+k_2) \quad (16)$$

$$k_2=\frac{V_Fs_1}{s_2-s_1} \quad (17)$$

Having k_1 and k_2, the C_1 voltage at the final moment of phase 1 (right before switching SW_1 on) will be:

$$V_{C1}(t_0)=V_{in}+k_1e^{s_1t_0}+k_2e^{s_2t_0} \quad (18)$$

Likely, the L_1 current at $t=t_0$ will be:

$$i_{C1}(t_0)=\left(k_1s_1e^{s_2t_0}+k_2s_2e^{s_2t_0}\right)C_1 \quad (19)$$

These two values are used as the initials for the second operating phase.

B- The Full-Charge phase

This phase starts when the R_1 resistor is bypassed by the SW_1 switch and continues until the capacitor C_1 reaches full charge, where the relay switch RL_1 in Fig. 1 is closed. According to the power circuit of this phase shown in Fig. 2(b):

$$L_1\frac{di_{L1}}{dt}+\frac{1}{C_1}\int i_1dt=\sqrt{3}V_m\cos(\omega t+\theta) \quad (20)$$

$$\Rightarrow\frac{d^2i_{L1}}{dt^2}+\frac{1}{L_1C_1}i_{L1}=-\frac{\sqrt{3}V_m\omega}{L_1}\sin(\omega t+\theta) \quad (21)$$

The roots of the characteristic equation will be:

$$s_{1,2}=\sqrt{-\omega_0^2}=\pm j\omega_0 \quad (22)$$

where:

$$\omega_0=\frac{1}{\sqrt{L_1C_1}} \quad (23)$$

And the final form of the current equation will be:

$$i_1(t)=k_1cos\ \omega_0t+k_2sin\ \omega_0t+Z\sin\left(\omega t+\theta\right) \quad (24)$$

where:

$$Z=\frac{\sqrt{3}V_m}{\sqrt{\left(\frac{1}{\omega C_1}-\omega L_1\right)^2}} \quad (25)$$

where $\omega=2\pi f_n$. Using initial state of $I_0=0$, k_1 and k_2 will be driven as:

$$k_1=-Z \quad (26)$$

$$\left(\frac{di}{dt}\right)_o=\frac{(V_s-V_{C1(to)})}{L_1} \quad (27)$$

$$\Rightarrow k_2=\frac{V_{L1}(0)-Z\omega}{\omega_0} \quad (28)$$

After determining k_1 and k_2 and replacing them in (24), the current equation of C_1 in phase 2 will be derived. From equalizing the I_{c1} derivative with zero, t_p the time for I_{c1} to get to its peak point is determined:

$$di(t)/dt=-k_1\omega_0\sin(\omega_0t_0)+k_2\omega_0\cos(\omega_0t_0)+...$$
$$...Z\omega\cos\left(\omega t_0+\theta\right)=0\rightarrow t_p=... \quad (29)$$

Replacing t_p into (24), the peak current in phase 2 will be determined:

$$i_{peak}=k_1\cos(\omega_0t_p)+k_2\sin(\omega_0t_p)+Z\sin\left(\omega t_p+\theta\right) \quad (30)$$

To limit the peak current in the second phase to the desired value, the time range of the first phase can be increased. This way, it is possible to limit the value of I_p so that no destructive

inrush current at the start of the second phase will happen. Also, by setting (24) equal to zero, the time range of the second phase can be obtained called t_f. The capacitor charge V_{C1} after the first cycle in the second phase, when the current reaches zero, will be:

$$\Delta V_{C1}\left(t_f\right)=\frac{1}{C_1}\int i_1 dt_f=\frac{1}{C_1}(\frac{k_1}{\omega}\sin\omega_0 t_f+... \\ ...Z\sin\left(\omega t_f+\theta\right)-\frac{k_2}{\omega}\cos\omega_0 t_f) \quad (31)$$

C- The Switching Soft-Start phase

This phase starts after the relay switch RL_1 in Fig. 1 is closed, and consists of two modes. The first mode is the L_2/C_2 charging mode, in which the S_1 switch is ON and feeds the output capacitor charging circuit. The second mode is called *the* L_2 discharging mode when S_2 gets ON.

Charging Mode

As the C_1 capacitor has reached its full charge, V_{C1} is assumed to be constant from now on. As the output voltage is lower than the rated, the load stands unconnected. So, based on Fig. 2(b):

$$L_2\frac{di_{C2}}{dt}+R_2 i_{C2}+V_{C2}=V_{C1} \quad (32)$$

Replacing $i_{C2}=C_2 dV_{C_2}/dt$ will give:

$$\frac{d^2V_{C2}}{dt^2}+\frac{R_2}{C_2}\frac{dV_{C2}}{dt}+\frac{V_{C2}}{L_2C_2}=\frac{V_{C1(t)}}{L_2C_2} \quad (33)$$

The roots of the characteristic equation will be:

$$s_{1,2}=-\frac{R_2}{2L_2}\pm\sqrt{\left(\frac{R_2}{L_2}\right)^2-\frac{4}{L_2C_2}} \\ \Rightarrow s_{1,2}=-\alpha\pm\sqrt{\alpha^2-\omega_0^2} \quad (34)$$

where α and ω_0 are:

$$\alpha=\frac{R_2}{2L_2} \quad (35)$$

$$\omega_0=\frac{1}{\sqrt{L_2C_2}} \quad (36)$$

The internal resistance of the HF inductor is very small, making $\alpha<\omega_0$, so:

$$V_{C2}(t)=V_F+e^{-\alpha t}\left(k_1 cos\omega_n t+k_2 sin_1\omega_n t\right) \quad (37)$$

where:

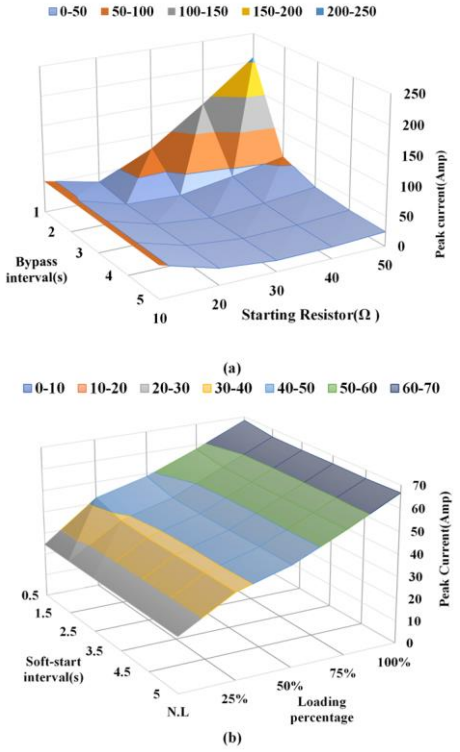


Fig. 3. Peak current in the DC link at the first and second phases a) Based on startup time and starting resistance value b) Based on system loading percentage

$$\omega_n=\sqrt{\omega_0^2-\alpha^2} \quad (38)$$

Using initial stats of $V_{C2}(0)=I_{C2}(0)=0$ will give:

$$k_1=-V_{C1} \quad (39)$$

$$k_2=-\frac{\alpha V_{C1}}{\omega_n} \quad (40)$$

The output filter current will be:

$$i_{L2}(t)=i_{C2}(t)=C_2(-\alpha e^{-\alpha t}(k_1\cos(\omega_n t)+k_2\sin(\omega_n t))+... \\ ...e^{-\alpha t}(-k_1\omega_n\sin(\omega_n t)+k_2\omega_n\cos(\omega_n t))) \quad (41)$$

This operating mode will continue for $t=\%D/f_s$ and:

$$D=\left\lfloor t\frac{D_n}{\Delta t_{ss}}.100\right\rfloor \quad (42)$$

Discharge Mode

The equivalent circuit of this mode can be seen in Fig. 2(c). Since in this phase, the capacitor C_2 is not fully charged, the second-order RLC loop is formed to obtain the values of the capacitor voltage and the inductor current in this state, according to the KVL in Fig. 2(c):

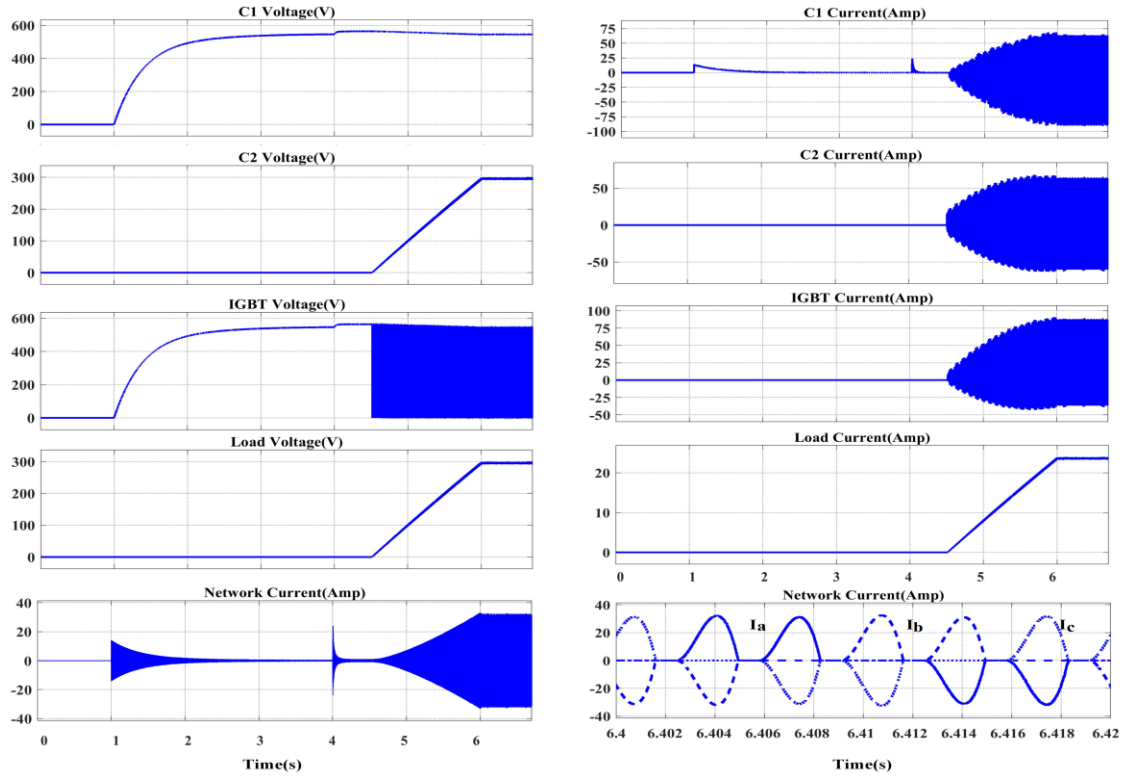


Fig. 4. Waveforms of simulation results of the proposed method

$$L_2 \frac{dV_{C2}}{dt} + R_2 i_{C2} + V_{C2} = 0 \tag{43}$$

$$i_{C2(t)} = C_2 \frac{dV_{C_2}}{dt} \tag{44}$$

$$\Rightarrow \frac{d^2 V_{C2}}{dt^2} + \frac{R_2}{C_2}\frac{dV_{C2}}{dt} + \frac{V_{C2}}{L_2 C_2} = 0 \tag{45}$$

Then the roots of the characteristic equation will be:

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \tag{46}$$

where:

$$\alpha = \frac{R_2}{2L_2} \tag{47}$$

$$\omega_0 = \frac{1}{\sqrt{L_2 C_2}} \tag{48}$$

As previously mentioned, in this phase $\alpha < \omega_0$, the output voltage and current will be:

$$V_{C2}(t) = V_F + e^{-\alpha t}\left(k_1 cos\omega_n t + k_2 sin\omega_n t\right) \tag{49}$$

$$i_{C2(t)} = C_2\left(-\alpha e^{-\alpha t}(k_1\cos(\omega_n t) + k_2\sin(\omega_n t)) + \ldots \right.$$
$$\left. \ldots e^{-\alpha t}(-k_1\omega_n\sin(\omega_n t) + k_2\omega_n\cos(\omega_n t))\right) \tag{50}$$

The initial states to determine k_1 and k_2 will be evaluated from (41) and (37) using $t=\%DT$, k_1 and k_2 will be driven as:

$$k_1 = V_{C_1}(DT - 1) \tag{51}$$

$$k_2 = \frac{\frac{DT(V_{C1})}{R_2} - \alpha C_2 V_{C1}(DT-1)}{C_2\omega_n} \tag{52}$$

The final values of C_2 voltage and current can be evaluated from(49) and (50) with $t=T$.

TABLE I
PARAMETERS OF THE SYSTEM UNDER STUDY

Component	Parameter	Value
Grid	3 Phase	380 V 50 Hz
Buck-Converter	Rated power	15 KW
	Switching frequency	7.24 KHz
	Inductor L_1	300 µH
	Capacitor C_1	10000 µF
	Inductor L_2	189 µH
	Capacitor C_2	8000 µF
	R_1	50 Ω
	Inductor DC Resistance R_2	0.02 Ω
	R_{load}	8 Ω for a full load 15 Ω for a half load
	R_{dis1}, R_{dis2}	9400 Ω 100 W
	Nominal Output Voltage	300 V
	Nominal Output Current	50 A
	IGBT Module	SKM300GB12T4
	Gate Driver	HCPL316J
	Diode Bridge	SKD 210/16

TABLE II
PERFORMANCE COMPARISON WITH OTHER PUBLISHED DESIGNS

References	**Proposed converter**	[22]	[25]	[26]	[27]	[28]
Topology	**Step-down Buck Converter**	LLC Converter	Bidirectional Converter	GaN-based dual-output LLC Converter	DCM-Buck Converter	Phase-Shift Full-Bridge (PSFB) Converter
Input voltage (V_{DC})	**540**	400	400	600	500	400-600
Switching frequency (kHz)	**7.2**	120	100	600	50	18
No. of semiconductor switches	**2**	4	8	8	4	4
Output power (KW)	**15**	0.3	1.5	1.5	6.6	12
Output voltage (V)	**300**	12	200	250	200-450	40
Full load efficiency (%)	**96**	N.A	95.8	96.1	93	96
Soft-start interval(s)	**1.5**	1	2.7	20	2.2	2

The Same procedure can be followed for the next cycles with new values of *%D* from (42).

III. RESULTS AND DISCUSSION

The system under study consists of a 15 KW converter, which is fed by a three-phase 380 V power grid. The converter gives a nominal voltage of up to 300 V_{dc} with a maximum current of 50 A_{dc} to the load. Other parameters of this system are listed in detail in Table I. This set has been designed and implemented for a Car Shock-Absorber Manufacturing Company, as a power supply for the Electro-Plating Pool. Some of the designing constraints required by the client, like the set being designed on wheels, the cooling system to be air forced, etc., have reduced the power density. But the system still has better power density than thyristor-based rectifiers (which are usually used for this application), as it has removed the three-phase internal power transformer.

The system has been simulated in Matlab/Simulink first, with the same parameters as the experimental set, for the results to be comparable. Fig. 3(a) shows the peak of inrush current during phases 1 & 2 of the start-up procedure, concerning the starting resistor size and the phase#1 time duration. As illustrated by this figure, to keep current in the DC link under 15 A during start-up, a minimum starter resistor size of 35 Ω with a minimum time duration of 2.5 s is needed. On the other hand, Fig. 3(b) shows the peak current transient during the soft-start interval of the switching module. This figure shows that the current in this phase is highly dependent on load, but the minimum soft-start time of 1.2 s is enough to have the minimum transient current at no-load condition.

As a result, a 50 Ω/1500-watt resistor has been hired in the experimental set and also used in simulations. The time intervals for the three start-up procedure phases have taken 3, 0.5, and 1.5 seconds, respectively

To validate the modeling and the proposed approach, the simulation of this system has been performed in MATLAB/Simulink using the parameters of Table I.

The proposed start-up method, contains the pre-charge phase, full-charge phase, and the switching soft-start phase for 3, 0.5, and 1.5 s, respectively. Fig. 4 shows the system performance during the start-up procedure.

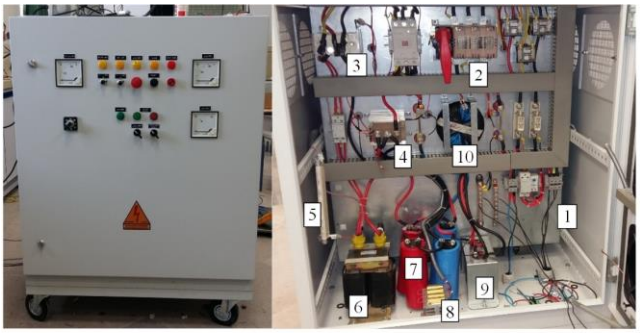
According to Fig.4, after 1 second of energizing the circuit, the charging phase of capacitor C_1 starts and after 3 seconds at 540 voltage, it is fully charged. At the same time as the R_1 resistor is bypassed, a voltage jump up to 560 will occur in the C_1 capacitor, and after 0.5 s, the main switches will be switched with a soft start time of 1.5 s and 55% pulse width at t=4.5 s. Meanwhile, when the switch SW_1 is closed, the resistor R_1 is bypassed and the peak current of 25 amps is applied to the capacitor. Similarly, after the soft start switching at t=4.5 s, the maximum current of the capacitor is equal to 68 amps, and after passing the start-up period, it reaches stability in the range of 63 amps.

After R_1 resistance is bypassed, the soft start switching process takes place, and in this case, the maximum current passing through switch S_1 will be 91 amps. In this case, the main switch current changes will be continuous without abnormal spikes. The voltage remains at its maximum value at 562 and 545 during the start-up period and in the steady-state respectively.

The process of charging capacitor C_2 takes place completely linearly without any abnormality until it reaches full charge in t=6 seconds. During the charging process, the current of the capacitor is continuous and without destructive spikes, the maximum current applied to the capacitor in this case reaches 68 amps. Similarly to capacitor C_1, after passing the start-up period, the current will stabilize and be limited to 63 amps.

With the desired pre-charge resistor R_1, the charging current is limited to 14 amps at the beginning of the start-up and is limited to 3 amps within 1.7 s.

Considering the pre-charge phase as 3 seconds, after removing the limiting resistor R_1 at t=4 the current pulse at the beginning



1: 3-Phase Input Voltage
2: Master Switch
3: Diode-Bridge Rectifier
4: IGBT Module
5: Charging Resistors
6: L1 Inductor
7: C1 Capacitor
8: Discharge Resistors
9: C2 Capacitor
10: L2 Inductor

Fig. 5 Experimental set

of the full charge phase is limited to 25 amps. After the soft start switching at t=4.5, the current stabilizes at 31 amps for 1.5 s, and no destructive current pulses are observed.

The experimental results on a 15 KW AC/DC/DC converter shown in Fig. 5 are presented in this section. The design preferences specifications, our design targeted a portable, air-cooled converter in a single enclosure. The final converter dimensions measured 80 by 75 by 110 cm and the mass was approximately 80 kg, which has been acceptable according to the customer's needs. All the parameters of the system are listed in Table I. As seen in Fig. 3, the changes in the initial inrush current become insignificant compared to the increase in the duration of the soft start after the value of 1.2 s So, for the results to be compared with the simulations, the time duration of the three phases of the start-up process has been set to 3, 0.5, and 1.5 s, respectively. To protect the system, the charging resistor R_1 has chosen 50 Ω/ 1500 w in the experimental set.

Fig. 6 shows the results of phases 1 & 2, the energization period of capacitor C_1. The charging current with the R_1 resistor is limited to 10.5 amps. The transient of the resistor removal moment for t_0=3 is 15.7 amps, which is acceptable compared to 50 A nominal current. After bypassing R_1, the C_1 voltage jumps to 560 V in 0.5 s. It should be noted that in this test, to be able to recognize the start-up period, after bypassing the resistor R_1, the switching circuit is disabled.

Fig. 7 shows the voltage/ current of high/low IGBTs at the start of switching and the steady state. As the system starts no-loaded, the current average is zero. The peak-to-peak current in both switches remains under 65 amps (38 amps peak value at soft-start period). The DC link voltage has fallen to 544 V after switching start-up. Fig. 8(a) shows the HF inductor L_2 current at the soft starting period, which proves no transient inrush happened. The steady-state current of L_2 in Fig. 8(b) shows a continuous waveform with a 25 amps ripple amplitude. The system is now loaded with half nominal load (R_{load}=15 Ω). Figs 8(c) and 8(d) show the transient and steady-state waveform of the HF inductor L_2 current, which proves no transient current at the loading moment happened. The current ripple is also unchanged. Fig. 8(a) shows the HF inductor L_2 current at the soft starting period, which proves no transient inrush happened. The steady-state current of L_2 in Fig. 8(b) shows a continuous waveform with a 25 amps ripple amplitude. The system is now loaded with half nominal load (R_{load}=15 Ω).

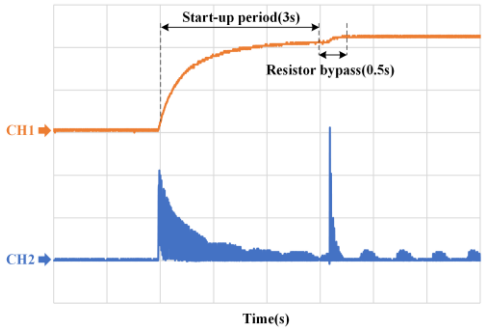


Fig. 6 Experimental results for capacitor C1 energization Ch1: voltage (250 V/div), Ch2: Current (5 A/div) for t_0=3

Figs 8(c) and 8(d) show the transient and steady-state waveform of the HF inductor L_2 current, which proves no transient current at the
loading moment happened. The current ripple is also unchanged.

At last, the under-load soft-switching start-up test results are shown in Fig. 9. The soft-starting switching period happens in 1.5 s, no transient inrush current happens, and the voltage/current ripple at steady-state is 2.4V/ 1.1 A (lower than 1% / 2.5%). All the results prove that the proposed start-up strategy has conducted the system from an unloaded zero (initial) state to the loaded steady state, without any transient inrush current at any part of the circuit. It should be noted that the efficiency was calculated using the output power plus the total losses, which included the core losses multiplied by 1.5 to account for additional assembly losses. The core losses consisted of switching losses, iron core losses, and coil winding losses for this particular assembly.

The key parameters in this work and the performance comparison of the proposed method with prior literature are listed in Table II. It can be seen that compared with other published designs, the proposed converter has an obvious advantage in efficiency, without using a microcontroller or different sensors. Furthermore, it has a lower working frequency and higher power levels. Its 96% efficiency is higher compared to the Bidirectional (95.8%) and DCM-buck converter (93%) proposed in [25] and [27] respectively. Also, the use of fewer switches (2) compared to other references (4 and more), in addition to reducing the cost of construction, will increase the overall reliability of the converter. Its gain range is as good as the phase-shift converter in [28]. The rated power is larger than all listed literature. Therefore, the proposed method is a good choice for implementing a DC–DC converter with a high-power level and industrial application.

IV. Conclusion

In this paper, the problem of inrush current at the moment of energization and start-up of AC/DC/DC converters composed of a three-phase diode rectifier and synchronous buck converter at high powers was investigated. Due to the use of high-capacitance capacitors at the input and output of the converter, the direct drive of the circuit leads to a current up to several times the rated current and damages various parts, especially semiconductor switches. The proposed start-up method contains the application of a starting resistor and soft starting of the switching circuit. The method of calculating and designing all parameters of the circuit start-up, including the size of the start-up resistor and the timing of the start-up phases, were described and analyzed in this paper. The simulation results and experimental tests of the proposed method on a 380Vac to 300VDC three-phase converter showed that the maximum time required between the circuit start-up and the start of feeding the load in this method is 5 seconds. The input current, IGBTs current, HF inductor current, and the capacitors are all well limited to less than half their nominal values in this period. No transient inrush happened on any part of the system, and the final loading output voltage/current has no ripple and transient.

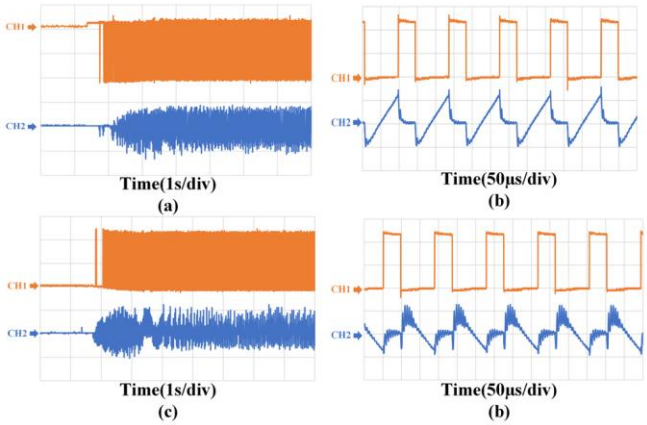


Fig. 7 Experimental results for IGBT switches, Ch1: voltage (250 V/div), Ch2: Current (25 A/div) a) high side switch start-up b) high side switch steady-state c) low side switch start-up d) low side switch steady-state

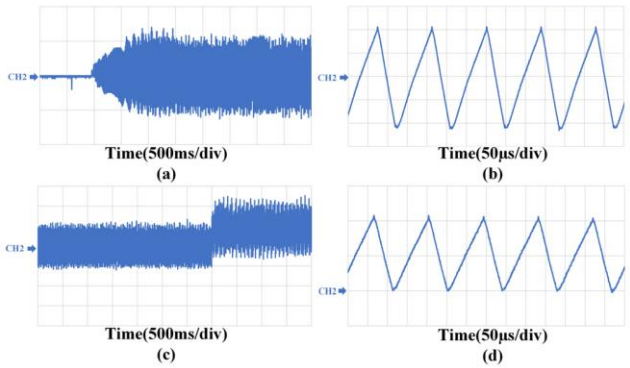


Fig. 8 Experimental results for HF inductor current a) switching start-up (25 A/div) b) no-load steady-state (12.5 A/div) c) half-loading (25 A/div) d) half-loaded steady-state (25 A/div)

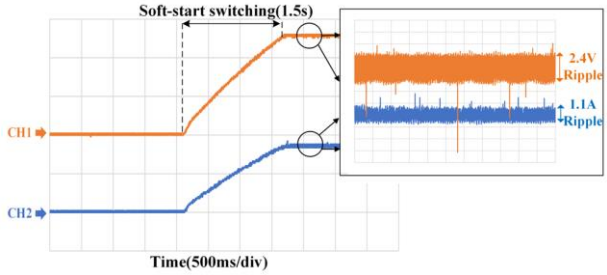


Fig. 9 Experimental results for Ch1: output voltage(120 V/div) Ch2: load current(15 A/div)

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