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Model Predictive Voltage Balance Control of Single-Phase Half-Bridge Active Front End Rectifier

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ABSTRACT

Single-phase rectifiers are one of the most practical instruments with various applications. Among them, active front-end (AFE) rectifiers are introduced with bidirectional power transfer capability for power factor correction and the elimination of current harmonics. This paper proposes an adaptive model predictive control (MPC) for a single-phase AFE rectifier. The AFE topology used in this paper is a half-bridge boost converter. This topology has higher efficiency than other single-phase AFEs due to the fewer number of active semiconductor devices. Considering the presence of one leg of capacitors in this topology, balancing the voltages of these capacitors is a challenge, along with other control objectives. Also, this paper benefits from an MPC approach by which the switching signal for every switching state is chosen such that the defined cost function is minimized in the operation state to achieve all control goals based on the predefined model of the rectifier. Furthermore, an adaptive algorithm for the inductor current estimation is presented to robustify the control system against any unwanted disturbance in the control system. As a demonstration of the superior performance of the proposed method, a 1kW rectifier setup with 700Vdc output voltage fed from a 230Vrms/50Hz grid is built in the laboratory. The applicability of the MPC controller is verified and all operation waveforms of the test setup are presented. The proposed method offers a high-quality input current with total harmonic distortion (THD) below 5% and a high-power factor (PF) close to one. Also, the efficiency is comparable with the available commercialized rectifiers

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I. Introduction

Switch-mode power supplies and rectifiers have high demand in various industrial applications and home appliances such as telecom power supplies, uninterruptible power supplies (UPSs), chargers, motor drive systems, and LED drivers. Diode and thyristor bridge-rectifiers are the simplest AC-DC circuits. But, these rectifiers suffer from many problems including a poor quality input current with high harmonic contents and a low power factor. Therefore, new rectifier circuits are proposed for reducing the grid current harmonic content and improving its quality, which are known as power factor correction (PFC) rectifiers. These rectifiers can be categorized into active and passive groups. The passive PFC rectifiers include boost PFC rectifiers and Vienna rectifiers, while the active type includes active front-end (AFE) rectifiers presented in [1]-[11].

The AFE rectifiers have a wide range of applications from low-power systems to high-voltage DC transmission systems and UPSs. Unlike diode rectifiers, AFE rectifiers offer bidirectional power flow with a high control capability and waveform quality. Therefore, these rectifiers are suitable to be employed for energy recovery braking systems, wind turbines, variable speed drives, and active power filters. Also, they are used in electrolysis, transportation, controlled power supplies, and many other appliances. However, regulating the output voltage of AFE rectifiers and their input current PFC need a multi-closed-loop control process, which complicates its implementation.

The predictive control method is widely used in power electronics due to its design simplicity, flexibility, and robust operation with various types of multi-variable and nonlinear systems. Besides, the high computational burden is no longer a negative point for implementing predictive control methods since powerful processors have been commercialized in recent years [12]. The main concept of predictive control methods is to use the present system state and its model for predicting the next state of the system. This data is used to follow the future behavior of the controlled variables in an optimized and predefined way. Predictive control methods are mainly known as deadbeat control, hysteresis-based, trajectory-based, and model predictive control (MPC) methods [13].

The deadbeat predictive control method is a model-based method that calculates the controlled variable such that the error of the reference value and the measured one become as close to zero as possible in each sampling period. This method has been successfully employed for inverters [14]-[16], rectifiers [17], active power filters [18], and PFC converters [19]. The basic concept of the hysteresis-based predictive control method is trying to maintain the controlled variables within the boundaries of a region or hysteresis space [20], while in the trajectory-based predictive control method, the controlled variable follows a predefined trajectory [21]. MPC is known as the most powerful method in which a cost function is defined and the controlled variables are calculated for optimizing the cost functions. The continuous control set MPC and finite control set MPC are the most well-known types in the literature. The main difference between these two types is in modeling, implementation, and complexity [22]-[25]. The main drawback of the MPC method is that its switching frequency is not fixed, which incurs higher switching losses compared to the deadbeat predictive control method, which uses a modulator with a constant frequency.

In this paper, a half-bridge boost AFE converter with one capacitors leg is used as the output voltage filter. This topology offers a high efficiency due to its fewer number of semiconductor devices. However, balancing the voltages of its output capacitors has always been a serious challenge. Two approaches have been discussed in the literature for balancing the voltages of the capacitors. The first method is to measure the unbalance of the capacitors' voltages and add it to the current reference as a DC value [26]-[29]. The main drawback of this method is that the PI controller coefficients need to be updated after every parameter change, e.g. load current, which leads to the unbalance of the capacitors' voltages. This means that for the sake of maintaining the fast dynamic performance of the converter, the PI controller should operate like an adaptive controller, resulting in a more complicated control process. The second approach is to replace the circuit topology with a full bridge converter, which is not desirable due to its higher power loss and cost with more switching devices [30]-[33].

This paper studies the performance and advantages of the predictive controller for balancing the voltages of the capacitors in a conventional converter, along with regulating its output voltage and maintaining an input current power factor close to one.

The paper is organized as follows. Section II describes the topology and its operating principles. Section III introduces the proposed controller, and Section IV presents the simulation and experimental results.

II. Selected Topology and Performance Analysis

Fig. 1 shows the topology. In this circuit, the grid current can only be controlled if the voltage of each of the output capacitors is higher than the grid peak voltage. Two possible states in Fig. 1 are shown in Fig. 2 and 3, where S1(S2) is ON(OFF) and S1(S2) is OFF(ON). In the following, the circuit equations are derived in each of the two so-called states, and the model is discretized by using the Forward-Euler method.

According to Fig. 2, the inductor voltage can be obtained by KVL in the loop including the input source and capacitor C1. Accordingly, one can write,

$$V_{L_S}(t) = V_S(t) - R_s i_{L_s}(t) - V_{C1}(t) \quad (1)$$

$$\frac{di_{L_S}(t)}{dt} = \frac{1}{L_s}(V_S(t) - R_S i_{L_s}(t) - V_{C1}(t)) \quad (2)$$

where V_{Ls} is the inductor voltage, V_S is the input source voltage, L_S is the input inductor, R_S is the equivalent series resistor (ESR) of the inductor, V_{C1} is the voltage of the capacitor C_1, and i_{Ls} is the input source current. According to the predictive controller nature, the continuous-time domain equations should be converted to the discrete-time domain. For this purpose, this paper uses the Forward-Euler method. Therefore, (2) is written as,

$$i_{L_s}(k+1) = \frac{\Delta t}{L_S}(V_S(k) - V_{C1}(k)) + i_{L_s}(k)(1 - \frac{R_s \Delta t}{L_S}) \quad (3)$$

where Δt is sampling period, k is the current sample, and (k+1) is the next sample. By using (3) and the input voltage, capacitor C_1 voltage, and input current in the k-th sampling period, the input current in the next sample can be derived. Also, the voltages of the output capacitors in the next sample can be obtained using the follwong equations.

$$V_{C1}(k+1) = \frac{\Delta t}{C} i_{L_s}(k) + V_{C1}(k) - \frac{\Delta t}{C \times R_{Load}}(V_{C1}(k) + V_{C2}(k)) \quad (4)$$

$$V_{C2}(k+1) = V_{C2}(k) - \frac{\Delta t}{C \times R_{Load}}(V_{C1}(k) + V_{C2}(k)) \quad (5)$$

where C=$C1$=$C2$, R_{Load} is the resistance of the load, and V_{C2} is the voltage of the capacitor C_2.

Following the same procedure for the circuit shown in Fig.3, (1)-(5) can be rewritten as follows,

$$V_{L_s}(t) = V_S(t) - R_s i_{L_s}(t) + V_{C2}(t) \quad (6)$$

$$\frac{di_{L_s}(t)}{dt} = \frac{1}{L_s}(V_S(t) - R_S i_{L_s}(t) + V_{C2}(t)) \quad (7)$$

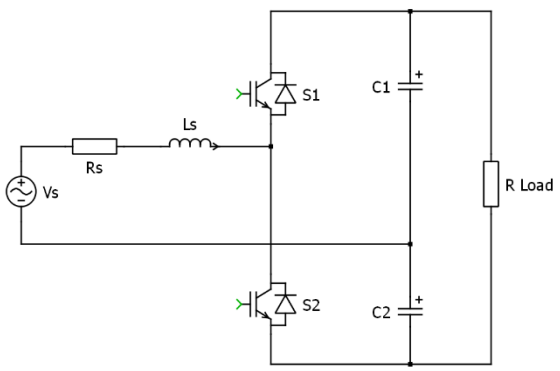


Fig. 1. Single-phase half-bridge AFE rectifier.

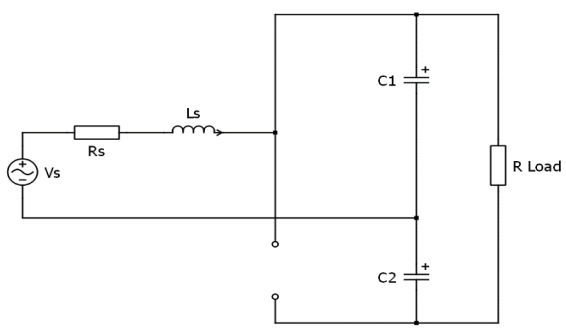


Fig. 2. Converter structure when S1 is on.

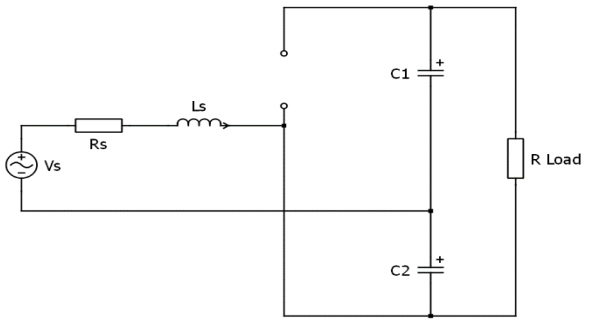


Fig. 3. Converter structure when S2 is on.

$$i_{L_s}(k+1) = \frac{\Delta t}{L_S}(V_S(k) + V_{C2}(k)) + i_{L_s}(k)(1 - \frac{R_s \Delta t}{L_S}) \quad (8)$$

$$V_{C1}(k+1) = V_{C1}(k) - \frac{\Delta t}{C \times R_{Load}}(V_{C1}(k) + V_{C2}(k)) \quad (9)$$

$$V_{C2}(k+1) = \frac{-\Delta t}{C} i_{L_s}(k) + V_{C2}(k) - \frac{\Delta t}{C \times R_{Load}}(V_{C1}(k) + V_{C2}(k)) \quad (10)$$

III. Proposed Control Algorithm

According to the discretized model of the converter and based on the MPC requirements, the predefined cost function is derived as,

$$g = \alpha \left| i_{L_s}(k+1) - i_{L_s}^{\mathrm{Ref}} \right|^2 + \beta \left| V_{C1}(k+1) - V_{C2}(k+1) \right|^2 \quad (11)$$

where g is the cost function, i_{Ls}^{Ref} is the input current reference, and α and β are the weight factors of the cost function. As is seen in the cost function, balancing the voltages of the capacitors is added as a penalty in addition to input current control. Moreover, the squared error is selected for each term of the cost function since (11) is a binomial cost function. Obviously, by appropriately selecting the weight factors, a tradeoff can be made between the control objectives.

Fig. 4 shows the proposed flowchart of the control algorithm. As shown, the input current reference is calculated by a PI controller with the measured values. Then, given that in each instance, one can decide which power switch should conduct. The input current and capacitors voltages are calculated for every possible switching operation, along with its corresponding cost function output. Finally, the power switch with the lower cost function output should conduct in the next instance.

IV. Simulation And Experimental Results

A. Simulation Result

To analyze the performance of the proposed method, the power and control stages are first simulated in PLECS with parameters given in Table I. Fig. 5 shows the steady-state input current and voltage of the converter. The input current harmonic spectrum is shown in Fig. 6 in comparison with the IEC61000-3-2 standard. According to Fig. 6, the total harmonic distortion (THD) of the input current is 2.7%. Also, the power factor is close to unity (Fig. 5). The output voltage of the converter and the voltages of the output capacitors are

also shown in Fig. 7. According to this fig., the output ripple is about 2%, and the voltages of the capacitors are balanced. It should be noted that balancing the voltages of the capacitors depends on the control method, load current, capacitance of the capacitors, etc. [26], [27], [30]. The output power changes are shown in Fig. 8 where the mean value of the power is 1kW.

In the second stage, the converter is constructed in the laboratory. The system parameters are listed in Table I.

B. Experimental Result

This paper used the MSOGI-FLL technique to detect the input voltage phase and derive its fundamental components (without distortion). Phase-locked loop (PLL) is a common method of voltage phase detection. The MSOGI-FLL technique is replaced with the conventional PLL for the following reasons:

- The control goals considered can be affected by uncontrollable factors such as input voltage distortion and harmonics;
- The delay in the conventional PLL causes moving away from control goals;
- MSOGI-FLL has faster and more accurate than the conventional PLL;
- MSOGI-FLL is an appropriate approach to getting the frequency and reference phase in power system frequency fluctuations and input voltage harmonics conditions.

Fig. 9 shows the MSOGI-FLL structure. According to this fig., by harmonic analysis of the input voltage and determining the desired harmonic number, MSOGI-FLL extracts this harmonic component in the output. In this paper, we considered fundamental, third, and fifth harmonic components in the MSOGI-FLL structure [34]-[36].

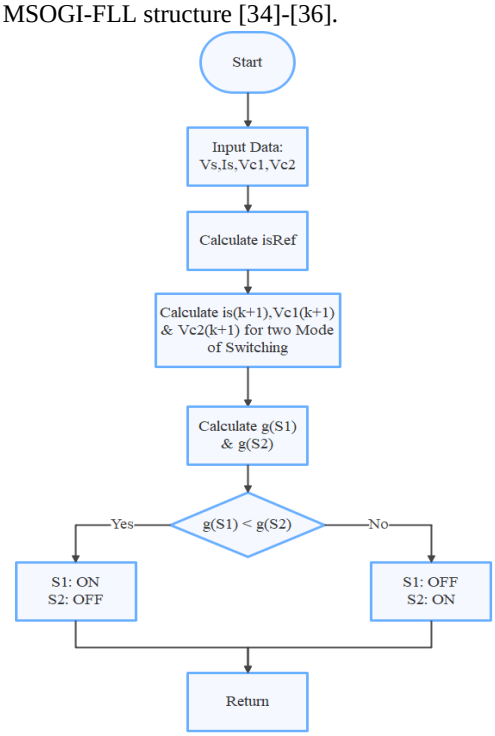


Fig. 4. The proposed flowchart of the control algorithm.

TABLE 1
SIMULATION AND EXPERIMENTAL PARAMETERS

Description	Values
Rated Power (P_o)	$1kW$
Input AC Voltage (V_S)	$220V_{rms}$
Frequency (f)	$50\,Hz$
Output DC Voltage (V_{DC}^{Ref})	$700V$
Capacitor (C_1, C_2)	$1200\,\mu F$
Input Inductor (L_S)	$8mH\,(ESR = 0.2\Omega)$
IGBT Switch (S_1, S_2)	FGL40N120AND
Sampling Time (Δt)	$25\,\mu S$
Microcontroller	STM32F407

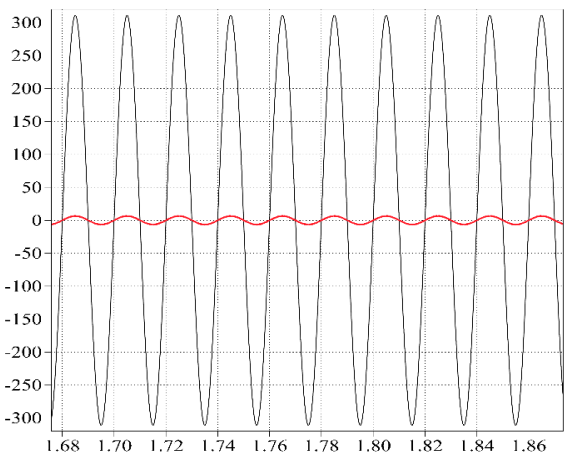


Fig. 5. Simulation results: input voltage (black) and input current (red).

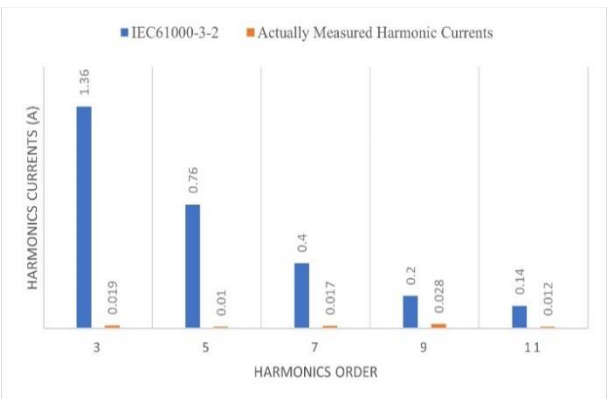


Fig. 6. Comparison between the converter input current harmonic spectrum with the standard spectrum.

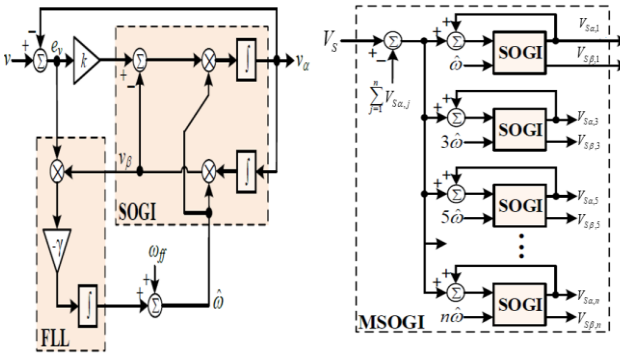


Fig. 9. MSOGI-FLL structure [34]-[36].



Fig. 10. Laboratory setup.

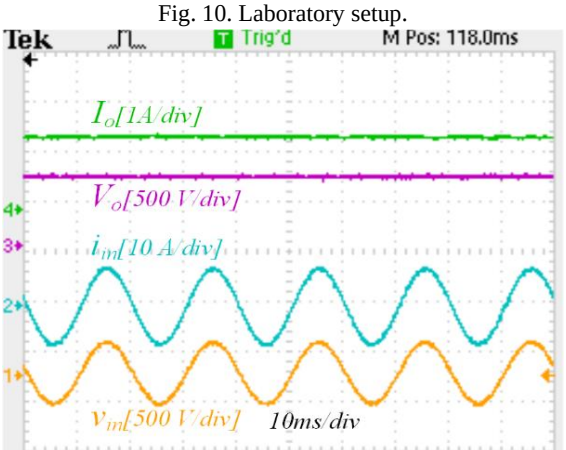


Fig. 11. Experimental results: CH1: input voltage (yellow), CH2: input current (cyan), CH3: output voltage (purple) and CH4: output current (green).

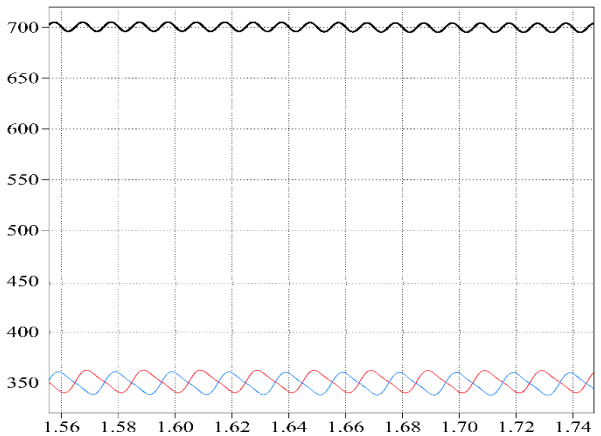


Fig. 7. Simulation results: output voltage (black), capacitor C1 voltage (blue) and capacitor C2 voltage (red).

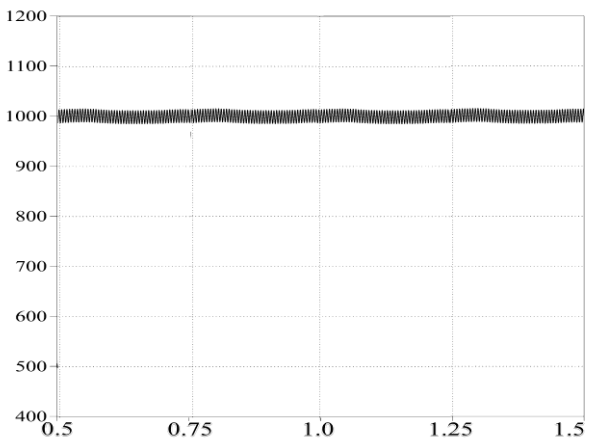


Fig. 8. Simulation results: output power.

To confirm the theoretical and simulation results, a laboratory setup of the proposed method is built, which is shown in Fig. 10. The setup parameters are listed in Table I.

The steady-state input voltage and current, and output voltage and current are shown in Fig. 11. As can be seen, the input current has a sinusoidal waveform with THD<5%, and the output voltage reaches its reference value with a voltage ripple lower than 2%. The steady-state output voltage with capacitors voltages is also shown in Fig. 12.

The capacitors voltages are balanced at the same DC voltage (350V), and the output voltage ripple is lower than 2%.

The steady-state output voltage, current, and power are shown in Fig. 13. According to this fig., the output power is 1kW with a very low ripple. Therefore, the successful performance of the proposed method is confirmed.

The THD and the PF of the proposed method are measured by using a FLUKE-435 power analyzer. The results show that THD is lower than the standard limits at nominal power. The power factor and THD at different output powers are also shown in Fig. 14 and 15. The power factor is almost always near unity.

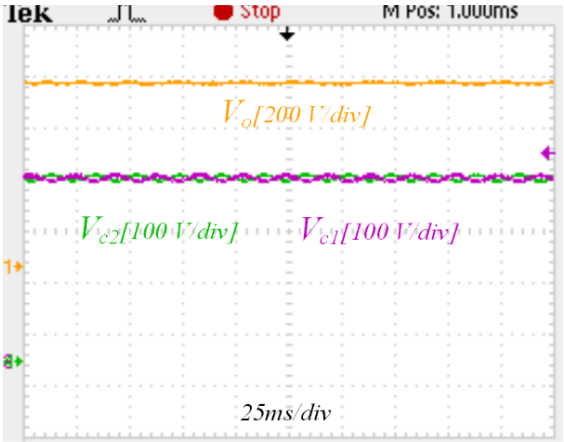


Fig. 12. Experimental results: CH1: output voltage (yellow), CH3: capacitor C1 voltage (purple) and CH4: capacitor C2 voltage (green).

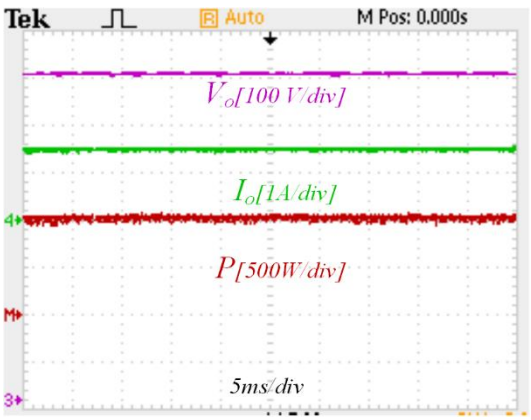


Fig. 13. Experimental results: CH3: output voltage (purple) and CH4: output current (green) and CH-M: output power (red).

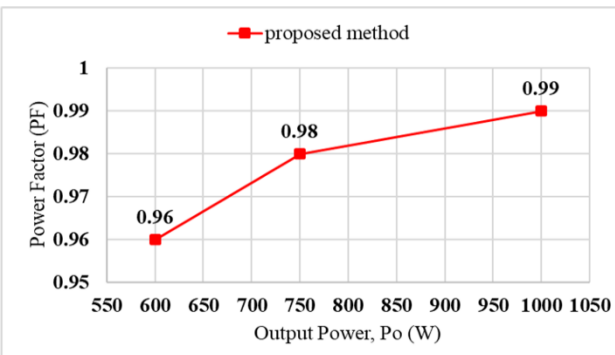


Fig. 14. Measured converter power factor at different output power.

Table II presents previous studies in which the controller structure has been modified to help achieve a balance in the voltage of the capacitors. As can be seen, some studies were limited to proving their results in the simulation environment. Considering the difference between the simulation results and experimental results, the studies with experimental results are more reliable. The output voltages of the works mentioned in Table II are not more than 530V. Meanwhile, the voltage unbalance of the capacitors will be higher at high voltages.

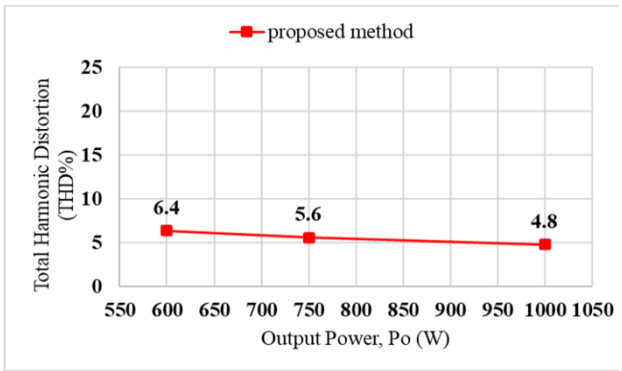


Fig. 15. Measured grid current THD at different output power.

As a result, the effectiveness of the methods used in past research for the high output voltage and output power of the converter is ambiguous. Also, according to Table II, references 6 and 7, which have considered a higher output power for the converter, used analog control to balance the voltage of the output capacitors. The experimental results of this paper show the effectiveness and appropriate performance of the controller in reducing input current THD and balancing output capacitors voltage in higher output voltage and power versus the previous works.

V. Conclusion

In this paper, a single-phase AFE rectifier with predictive control and output power of 1 kW was designed and built in order to verify the feasibility of the proposed control method. Simulation and laboratory results show that the predictive controller accurately balance the voltage across the capacitors while regulating the output voltage. Also, this method has the ability to maintain the high quality of the grid current in a wide range of load change.

Therefore, this method is a suitable alternative for previous solutions. The single-phase AFE circuit is a more advantageous topology than other well-known counterparts, especially in terms of cost and power loss.

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TABLE 2
COMPARISON BETWEEN THE PRESENT WORK WITH PREVIOUS RESEARCHES

Ref.	Controller	Vin (V)	Vout (V)	Pout (W)	THD (%)	Simulation / Experimental Result
[37]	Linear Control	120	450	80	2.5	EXPERIMENTAL
[28]	Hysteresis Current Control	90	300	300	1.7	EXPERIMENTAL
[23]	Hysteresis Current Control	100	260	130	N A	EXPERIMENTAL
[38]	PWM Average Model	70	150	375	13	SIMULATION
[29]	Dead Beat	170	400	80	2	SIMULATION
[39]	Analog Control	220	530	800	3.6	EXPERIMENTAL
[40]	Analog Control	150	400	1000	N.A	EXPERIMENTAL
Present Work	Model Predictive Control	220	700	1000	4	EXPERIMENTAL

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