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Design a PLL for Fractional Frequency Synthesizers using DDSM with Reduced Hardware

Leila Jahanpanah[1], Seyed Ali Sadatnoori[2,†], Iman Chaharmahali[3]

[1] Department of Electrical Engineering, Mahshahr Branch, Islamic Azad University, Mahshahr, Iran
[2] Department of Electrical Engineering, Shoushtar Branch, Islamic Azad University, Shoushtar, Iran
[3] Department of Electrical Engineering, Andimeshk Branch, Islamic Azad University, Andimeshk, Iran

ABSTRACT

Phase locked loop (PLL) circuits are widely used in fractional frequency synthesizers. In these synthesizers, fractional multiples of the reference frequency can be synthesized, so the reference frequency and the bandwidth of the loop can be increased. This frequency synthesizer is commonly used due to its flexibility and convenient frequency adjustment. In this paper, a PLL circuit of the transistor level is designed in which a hybrid digital sigma-delta modulator with reduced hardware is used. This Digital Delta-Sigma Modulator (DDSM) has four stages that have a lower noise level and power consumption than the conventional type. This PLL circuit has a third-order loop filter and a voltage-controlled oscillator of the NMOS type. In the PLL circuit, two counters are used in its feedback path. In the proposed divider, there is a dual divider P / P + 1 (in this case 5, 6) which divides its input signal by 5, 6 according to the control input. A design example for the PLL is provided. A third stage digital Delta-Sigma modulator with reduced hardware is also used to control these counters. This modulator has less power consumption than the conventional method and has less number of transistors by 85%.

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I. INTRODUCTION

Frequency synthesizers are an important part of multi-frequency wireless transmitter / receiver circuits. The phase locked loop in the frequency synthesizer is primarily used as a local oscillator in wireless receivers, lowering the carrier frequency to the intermediate frequency (IF). Phase locked loop circuits are used for modulation phase and frequency modulation, clocked pulse recovery, communication noise prevention, frequency synthesizer, deflection prevention, edge detection and many other applications.

Phase locked loop (PLL) circuits are widely used in fractional frequency synthesizers. In these synthesizers, fractional multiples of the reference frequency can be synthesized, so the reference frequency and the bandwidth of the loop can be increased. This frequency synthesizer is commonly used due to its flexibility and convenient frequency adjustment.

Most frequency synthesizers use phase locked loop circuits. Each PLL circuit includes a phase comparator (PC), a low-pass filter (LPF), a charge pumping (CP), and a voltage-controlled oscillator (VCO). [1]

The blocked diagram of a PLL circuit is shown in Fig.1. A digital sigma-delta modulator is used to control the division ratio in the phase locked loop circuit. In Fig.1 X is the modulator input, N_0 is the correct division ratio and M is the modulator module. Therefore, the following relation is established in the fractional frequency synthesizer. Usually,

†**Corresponding Author:** a.sadatnoori@iau-shoushtar.ac.ir
Tel: +989166401872, University of Shoushtar Branch,
Faculty of Electrical Engineering, Islamic Azad University, Shoushtar Branch, Shoushtar, Iran

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the modulus M is a multiple of two.

$$f_{out} = \left(N_0 + \frac{X}{M}\right).f_{ref} \quad (1)$$

where f_{ref} is the input frequency at the input to the phase comparator. In fractional frequency synthesizer architecture, both f_{out} and f_{ref} are integer multiples of f_s, where $f_s = \frac{f_{ref}}{M}$ is the channel spacing.

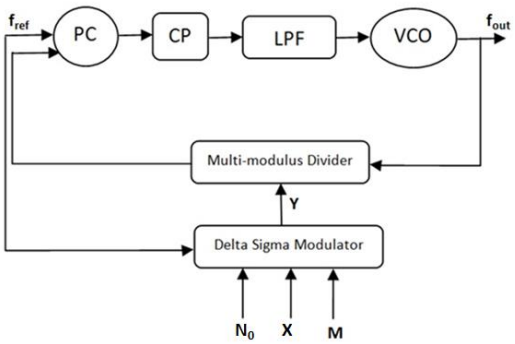


Fig.1: Blocked diagram of a PLL based fractional frequency synthesizer.

Digital Delta-Sigma modulators generally use two methods to increase the output period: Stochastic method and deterministic method.

The stochastic method uses a single-bit dither signal to randomize the output. This dither signal is either directly or filtered or effectively applied to the modulator input [2-6].

The deterministic method causes a change in the internal structure of the modulator to increase the periodicity of the output signal. Some of the deterministic methods used before are: Use the initial conditions for the first stage of the modulator [7], use the delay feedback path in each stage of the modulator [8-9], use the quantizer with the prime module [10], use the straight forward path to add the output of each stage to the next stage of the modulator [11].

Wang *et al.* [12] recommended a method for avoiding the development of spurs by substituting the sigma-delta modulator for a new type of digital quantizer and a charge pump offset incorporated with a sampled loop filter.

In [13-14], a solution is presented based on mixed-radix algebra, where the required ratio is formed by combining two and three different modulus. In [15-17], a novel method is proposed for applying periodic dither to a DDSM to obtain minimized spurious tones. The effects of adding the pseudorandom dither signal in different stages within the proposed Multi-stAge noise SHaping (MASH) modulator are expressed in a set of equations. In [18], the design of a new architecture of Continuous-Time (CT) MASH 2-2 (multi-stage noise shaping modulators) full feedforward Sigma-Delta (ΣΔ) modulator is presented. In [19], it is shown that applying a linear feedback shift register (LFSR) dither to a digital delta-sigma modulator (DDSM) cannot always increase its fundamental period.

The purpose of this paper is to introduce and design a new four stage Sigma-Delta modulator that has less hardware and power consumption than conventional methods. This modulator is used in a phase locked loop to properly adjust the division ratio of the modulator.

In the present work, we introduce hybrid DDSM 1-2-3-4 modulator architecture. In this method, the First Order Error Feedback Modulator (EFM1) in the first stage has a variable programmable modulus M_1 that is not a power of 2. The modulators in the second, third and four stages (M_2, M_3, and M_4, respectively) are the power of 2. The planning methodology relies on error masking [20-21]. Thus, the frequency synthesizer can produce the required frequency accurately without declining the performance and increasing hardware complexity. In this paper, a new phase locked loop circuit is designed which includes a third-order loop filter, a charge pump circuit, a voltage-controlled oscillator with the NMOS method, and a divider with two counters. The counters use the proposed digital Delta-Sigma modulator, which reduces hardware consumption.

The remainder of this paper is structured as follows: Section 2 describes the overall operation of the DDSM and summarizes related works. Section 3 describes the proposed hybrid modulator. The calculation of periodic length for hybrid MASH modulators is presented in Section 4. The parts of the phase locked loop circuit proposed in Section 5 are presented. Section 6 illustrates the design example and simulation results. Finally, conclusions are made in Section 7.

II. RELATED WORKS

Before presenting our plan methodology in detail, we first review a conventional MASH DDSM architecture. Here, a structure based on the error feedback modulator model (Fig.2) is considered. The signal v[n] is the sum of the digital words x[n] and s[n]. When v[n] is greater than M, the quantizer overflows and the output signal will be 1. In comparison, when v[n] is less than M, the quantizer does not overflow and y[n] will then be 0. Mathematically, we write:

$$y[n] = Q(v[n]) = \begin{cases} 0, & v[n] < M \\ 1, & v[n] \geq M \end{cases} \quad (2)$$

where M is the modulus of the quantizer and v[n] is the input to the quantizer [1].

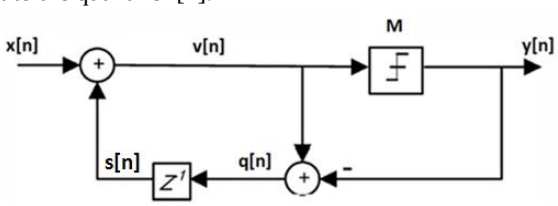


Fig.2: Blocked diagram of the first order error feedback modulator.

Fig.3 shows the blocked diagram of a classical l^{th} order

MASH DDSM comprising a cascade of l N-bit EFM1 blocks and a noise cancellation network.

The output of the classical MASH DDSMl can be expressed in the z-domain as [1]:

$$Y(z) = \frac{1}{M}.X(z) + (1 - z^{-1})^{l}.Q_{l}(z) \quad (3)$$

where $X(z)$ and $Q_l(z)$ are the z-transforms of the input and the quantizer noise introduced by stage l.

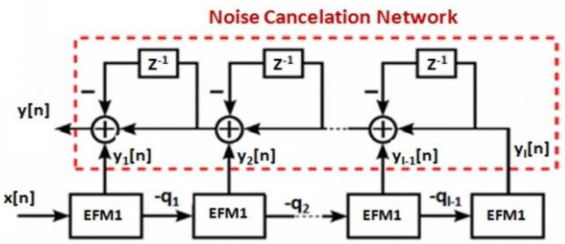


Fig.3: Blocked diagram of an l^{th} order MASH DDSM incorporating a cascade of EFM1s [1].

The structure of the HK-EFM1 (Hosseini and Kennedy EFM) used in the HK-MASH (Hosseini and Kennedy MASH) is illustrated in Fig.4. There is just one difference between this structure and the classical EFM1 in Fig.2; i.e., the existence of the feedback blocked az^{-1}. Here, a is a selected small integer to make (M−a) the maximum prime number below M. The cycle length of it is $(M - a)^{l} = (2^{N} - a)^{l}$, where l is the order of the modulator. Song and Park [11] proposed the modified MASH 1-1-1, as shown in Fig.5. The modified MASH structure cascades several first-order digital accumulators like the traditional MASH structure but has a supernumerary feedforward connection between two adjoining categories and increases the sequence period of quantization error.

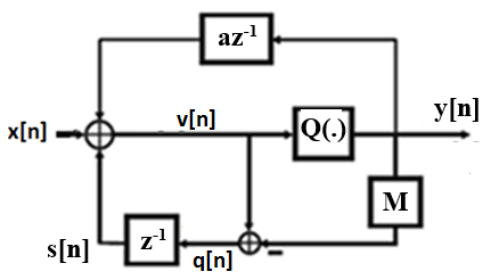


Fig.4: The modified EFM1 used in HK-MASH [10].

Le and Chen [23] presents a self-adaptive Sigma-Delta modulator, which offers opportunity to simplify the process of tuning parameters and further improve the noise performance.

Mazzaro and Kennedy [24] presents a Fractional-N Charge Pump (CP) PLL with a MASH 1-1-1 divider controller to exhibit pairs of spurious tones called “horn spurs”. Mai and Kennedy [25] describes a detailed analysis of the cause of wandering spur patterns in a MASH 1-1-1 DDSM-based fractional-N frequency synthesizer, supported by experimental measurements.

Shamsi proposes a new mismatch cancelation technique for quadrature delta-sigma modulators (QDSM). In this approach, a high speed and simple structure dynamic element matching (DEM) based on homogenization and time-division (HTD) is designed. [26]

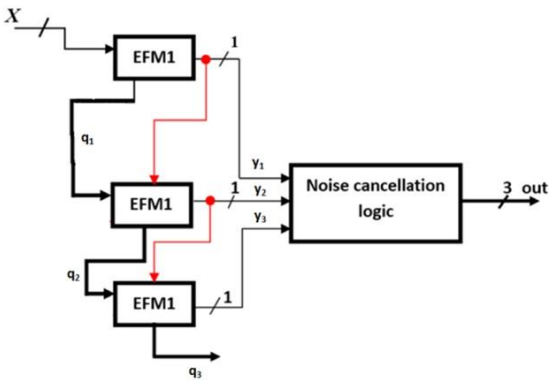


Fig.5: Blocked diagram of the modified MASH 1-1-1 proposed in Song and Park [11].

Mai et all presents two methods. It describes a 4.9-GHz 180-nm SiGe BiCMOS charge-pump phase-locked loop (CP-PLL) fractional-N frequency synthesizer platform with a divider controller that can function as: 1) a standard MASH 1-1-1; 2) a MASH 1-1-1 with high-amplitude dither; and 3) a MASH 1-1-1 with a modified third stage. [27]

Abdul and Nelakuditi presents the design and implementation of Charge Pump (CP) circuit to improve the mismatch in currents with good linearization in Low Voltage Fractional-N PLL suitable for RF applications. [28]

The Global System for Mobile communication (GSM) system is a time and frequency division system in which a carrier frequency and a time slot number characterize each physical channel.

Thus, in GSM 1800, the problem of synthesizing is considered an (f_{out}) output frequency of 1.80 GHz from a 13 MHz (f_{ref}) reference clocked. In this example, $f_{ref} = 13\ MHz, f_s = 200\ KHz, f_{out} = 1.80\ GHz$ yielding, $N_0 = 138$, and $X = 15123$, $M = 2^{15}$. In conventional MASH 1-1-1 based fractional frequency synthesizers having $M = 2^{15}$, the required division number can be approximated as follows:

$$f_{out} = \left(138 + \frac{15123}{2^{15}}\right).f_{ref} = 1.799999725\ GHz \quad (4)$$

Hence, a frequency offset is approximately 274.65 Hz.

The approximation noise can be reduced using a larger value of modulus M. Also, it correlates with increasing the word length of the modulator, hardware complexity, and power consumption.

III. THE PROPOSED HYBRID DIGITAL SIGMA DELTA MODULATOR

In this section, we introduce a novel structure for the

dithered MASH DDSM 1-2-3-4 that produces a long sequence period.

This paper attempts to reduce the hardware and power consumption of the fourth-order Digital Sigma-Delta Modulator and improve the noise level. Therefore, a fourth-order sigma-delta modulator with a high bit number is broken down into several smaller sigma-delta modulators with fewer bits. Then, the input of the fourth-order modulator is divided into four segments so that each part of it is subdivided into first, second, third, and fourth-order modulators. We call this modulator, which consists of 4 sub-sections, a hybrid modulator.

The hybrid modulator architecture is shown in Fig.6. In this architecture, instead of a single classical power-of-two modulus sigma-delta modulator in the fractional-N frequency synthesizer, we can use four modulators. The first stage modulator is a Variable Modulus EFM1 (VM-EFM1) and has a programmable modulus M_1 that is not a power of 2. The VM-EFM1 is shown in Fig.7. The modulator has two inputs: X is the input signal and M_1 is an optional modulus. By using the modulus M_1, we can change the quantizer accuracy. The output of the VM-EFM1 can be expressed in the z-domain as:

$$Y(z) = \frac{X(z)}{M_1} + (1 - z^{-1})^{-1}.Q(z) \quad (5)$$

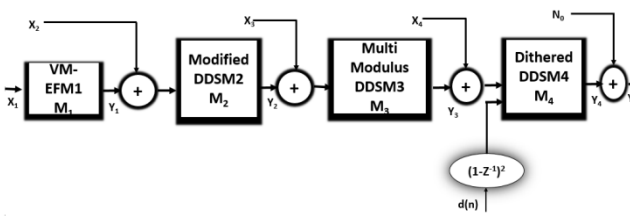


Fig.6: Blocked diagram of the hybrid modulator DDSM 1-2-3-4 used in fractional frequency synthesizer.

where X(z) and Q(z) are the z-transforms of the input and the quantization noise introduced by the VM-EFM1.In the fractional-frequency synthesizer, we can control the numerator and denominator of the fraction.

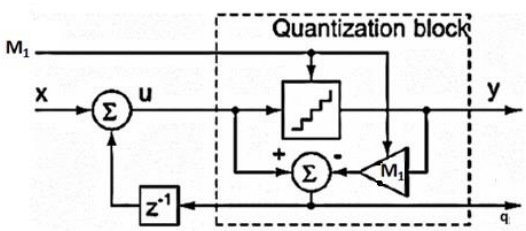


Fig.7: The variable modulus first order error feedback modulator (VM-EFM1) [7]

The second modulator in the hybrid structure is modified MASH 1-1, which has conventional modulo M_2. The cycle length in modified MASH 1-1 structure is ${M_2}^2$, where M_2 is the quantizer modulus in the classical DDSM.

The third modulator in the hybrid structure is multi-modulus MASH 1-1-1, which has conventional modulo M_3. The small positive integer a in the i^{th} stage of HK EFM1 is denoted as a_i. This value will be assumed different for each stage. The values of a_i are selected such that to make $\{M - a_1, M - a_2, \dots, M - a_l\}$ co-prime numbers to maximize the period. A few values of a_i are given in Table I. It is of note that to make the period independent of the input, $M - a_1$ is set as a prime number.

TABLE I

SOME VALUES OF A_I IN THIRD ORDER MASH 1-1-1.

Word Lengths (N)	a_1	a_2	a_3
4,6, 9, 10, 12	3	0	1
3, 5, 7	1	0	3
8	5	0	1
11	9	0	1

If the greatest common divisor of any two numbers is 1, they are co-prime numbers. A prime number is a number that has two divisors.

The fourth modulator in the hybrid proposed structure is dithered MASH 1-1-1-1, which a periodic LFSR dither input with a period N_d added to the third and fourth stages of MASH 1-1-1-1. Fig.8 presents an implementation of the second-order dither hybrid modulator.

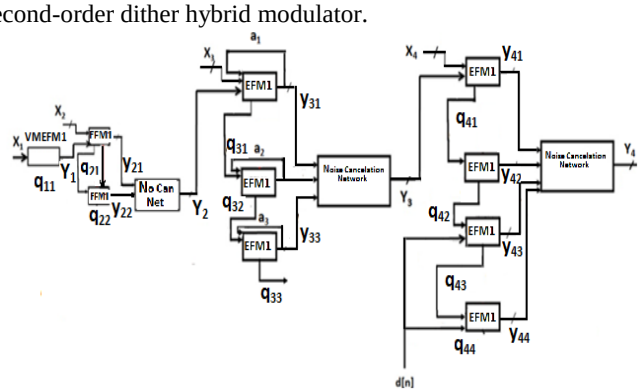


Fig.8: Implementation of the second order dither hybrid DDSM 1-2-3-4 modulator.

The output frequency (f_{out}) in the fractional frequency synthesizer is determined by:

$$f_{out} = (N_0 + \frac{X_4 + \frac{X_3 + \frac{X_2 + \frac{X_1}{M_1}}{M_2}}{M_3}}{M_4}).f_{ref} \quad (6)$$

In this case, the z-transforms y_1, y_2, y_3, y_4, and y_{out} are shown by:

$$Y_{out}(z) = N_0 + Y_4(z) \quad (7)$$

$$Y_4(z) = STF_4(z)(X_4 + Y_3(z)) + NTF_4(z)Q_4(z) \quad (8)$$

$$Y_3(z) = STF_3(z)(X_3 + Y_2(z)) + NTF_3(z)Q_3(z) \quad (9)$$

$$Y_2(z) = STF_2(z)(X_2 + Y_1(z)) + NTF_2(z)Q_2(z) \quad (10)$$

$$Y_1(z) = STF_1(z).X_1 + NTF_1(z)Q_1(z) \quad (11)$$

where STF_1, STF_2, STF_3, STF_4, NTF_1, NTF_2, NTF_3, and NTF_4 are the signal and error transfer functions of first, second, third and fourth stage modulators, respectively, and $Q_1(z)$, $Q_2(z)$, $Q_3(z)$, and $Q_4(z)$ are the quantization

error signals introduced by the first, second, third, and fourth sigma-delta modulators, respectively. X_1, X_2, X_3, and X_4 are the integer inputs of the VM-EFM1, modified MASH 1-1, multi-modulus MASH 1-1-1, and second-order dithered MASH 1-1-1-1in the hybrid architecture, respectively. Hence, the final output y_{out} can be attained by:

$$Y_{out}(z) = N_0 + STF_4(z).X_4 + STF_4(z).STF_3(z).X_3 + STF_4(z).STF_3(z).STF_2(z).X_2 + STF_4(z).STF_3(z).STF_2(z).STF_1(z).X_1 + NTF_4(z)Q_4(z) + STF_4(z).NTF_3(z).Q_3(z) + STF_4(z).STF_3(z).NTF_2(z).Q_2(z) + STF_4(z).STF_3(z).STF_2(z).NTF_1(z).Q_1(z) \quad (12)$$

where,

$STF_4(z) = \frac{1}{M_4}$, $STF_3(z) = \frac{1}{M_3}$, $STF_2(z) = \frac{1}{M_2}$, $STF_1(z) = \frac{1}{M_1}$, $NTF_4(z) = (1-z^{-1})^4$, $NTF_3(z) = (1-z^{-1})^3$, $NTF_2(z) = (1-z^{-1})^2$, and $NTF_1(z) = (1-z^{-1})$.

IV. Design Method

The DDSM quantization error power is distributed over a few tones that are specified by the period, leading to a tone spacing of $df[k] = \frac{f_s}{N}$, where f_s is the sampling frequency and N is the period. When the sequence length and, consequently, the number of tones is large, the Power Spectral Density (PSD) approaches the classical white noise approximation. The PSD of Y_2, Y_3, and Y_4 in the second-order LSB LFSR dither signal in the DDSM2, the multi-modulus DDSM3, and dithered DDSM4 are defined by [13]:

$$P_2(\Omega[k]) = \frac{1}{12}(|1-z^{-1}|)^4{}_{z=e^{j\Omega}} = \frac{1}{12}\left(2\sin\left(\frac{\Omega}{2}\right)\right)^4 \quad (13)$$

$$P_3(\Omega[k]) = \frac{1}{12}(|1-z^{-1}|)^6{}_{z=e^{j\Omega}} = \frac{1}{12}\left(2\sin\left(\frac{\Omega}{2}\right)\right)^6 \quad (14)$$

$$\Omega[k] = \frac{2\pi}{N}.k, \qquad k = 0,1,\dots,\frac{N}{2}$$

$$P_4(\Omega[k]) = \frac{1}{12}(|1-z^{-1}|)^8 + \frac{1}{12}\frac{1}{M_4{}^2}(|1-z^{-1}|)^4{}_{z=e^{j\Omega}} \quad (15)\ (16)$$

where Ω is the angular frequency of the oscillation and P is the density of the power spectrum. Also, at the output of the proposed hybrid modulator, since P_2 and P_3 are second-order and third-order shaped, respectively, while P_4 is fourth-order shaped, if the level of the lowest frequency tone in P_2 and P_3 is below that of P_4, the overall power of P_2 and P_3 should always be below the P_4 envelope. This can be expressed as:

$$P_2 < P_4, f = \frac{f_s.k}{N_2}, k = 1,2,\dots,\frac{N_2}{2} \quad (17)$$

$$P_3 < P_4, f = \frac{f_s.k}{N_3}, k = 1,2,\dots,\frac{N_3}{2} \quad (18)$$

Note that for a DDSM with an output period of *N*, the lowest frequency tone is at $\frac{f_s}{N}$.

Thus, at low frequencies:

$$|1-z^{-1}|^2 = \left|1-e^{\frac{-j2\pi f}{f_s}}\right|^2 = |2\sin\left(\frac{\pi f}{f_s}\right)|^2, \sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s} \text{ for } f \ll f_s \quad (19)$$

We can approximate P_2, P_3, and P_4 at low frequencies by:

$$P_2 = \frac{1}{12}\left(\frac{1}{M_3.M_4}\right)^2 2^4.(\frac{\pi f}{f_s})^4 \quad (20)$$

$$P_3 = \frac{1}{12}\frac{1}{M_4{}^2}2^6.(\frac{\pi f}{f_s})^6 \quad (21)$$

$$P_4 = \frac{1}{12}2^8.(\frac{\pi f}{f_s})^8 + \frac{1}{12}\frac{1}{M_4{}^2}2^4.(\frac{\pi f}{f_s})^4 \quad (22)$$

Substituting Equs. (20)-(22) into the constraints Equs. (17) and (18), we have:

$$\frac{1}{12}2^8.(\frac{\pi f}{f_s})^8 + \frac{1}{12}\frac{1}{M_4{}^2}2^4.(\frac{\pi f}{f_s})^4 \approx \frac{1}{12}2^8(\frac{\pi f}{f_s})^8 \quad (23)$$

$$\left(\frac{1}{M_3.M_4}\right)^2 2^4.(\frac{\pi f}{f_s})^4 < 2^8.(\frac{\pi f}{f_s})^8, f = \frac{f_s}{M_2{}^2} \quad (24)$$

$$2^6.\frac{1}{M_4{}^2}(\frac{\pi f}{f_s})^6 < 2^8.(\frac{\pi f}{f_s})^8, f = \frac{f_s}{(M_3-\alpha)^3} \quad (25)$$

Therefore:

$$\left(\frac{1}{M_4}\right)^2 < \frac{2^2.\pi^2}{M_3{}^6} \quad (26)$$

$$M_3{}^3 < 2\pi.M_4 \rightarrow 2^{3n_3} < 2\pi.2^{n_4} \rightarrow 3n_3 < \log_2(2\pi) + n_4 \rightarrow n_3 < \frac{2.65+n_4}{3} \quad (27)$$

$$\left(\frac{1}{M_3.M_4}\right)^2 < \frac{2^4.\pi^4}{M_2{}^4} \quad (28)$$

$$M_2 < \frac{\sqrt{M_3.M_4}}{2\pi} \quad (29)$$

In the VM-EFM1 accumulator, the output Y_1 will be periodic with a cycle length between two and M_1. In the worst case, the quantization noise power of VM-EFM1 is spread over (M_1-1) tones. The power in the lowest tone, after passing through MASH 1-1, multi-modulus MASH 1-1-1, and dithered MASH 1-1-1-1, is obtained by:

$$P_{tone} = (\frac{1}{M_1.M_2.M_3.M_4})^2 = STF_1{}^2.STF_2{}^2.STF_3{}^2.STF_4{}^2 \quad (30)$$

Consequently, to mask the worst-case tone from VM-EFM1 at the output of dithered DDSM 1-1-1-1, it is required that:

$$\Omega_1[1] = \frac{2\pi}{M_1}, k = 1, N_1 = M_1 \quad (31)$$

$$P_4(\Omega_1[1]) \geq N_f.P_{tone} \quad (32)$$

where N_f is FFT length, which presents the frequencies at which the PSD is estimated.

Substituting Equs. (22) and (30) into the constraint Equ. (32), we obtain:

$$N_f(\frac{1}{M_1.M_2.M_3.M_4})^2 \leq \frac{1}{12}(\frac{2\pi}{M_1})^8 \rightarrow M_1 \leq \sqrt[6]{\frac{(2\pi)^8.M_2{}^2.M_3{}^2.M_4{}^2}{12N_f}} \quad (33)$$

A. Simulation Results

Given three design parameters of the reference frequency f_{ref}, the channel spacing f_s, and the output frequency f_{out}, we need to determine nine integers of $N_0, X_1, X_2, X_3, X_4, M_1, M_2, M_3$, and M_4. First, M_4 is obtained and then M_1, M_2, and M_3 are calculated.

Selecting the variable modulus EFM1, we compute:

$$p_1 = \gcd(f_{ref}, f_{out}, f_s) \quad (34)$$

$$p_2 = \frac{f_{pc}}{p_1} \quad (35)$$

where gcd(a,b,c) denotes the greatest common divisor of a, b, and c. Then, the modulus M_1 is calculated as follows:

$$M_1 = \frac{p_2}{\gcd(p_1,p_2)} \quad (36)$$

M_2 and M_3 obtain from Equs (27) and (29).

Next, the inputs $N_0, X_1, X_2, X_3,$ and X_4 can be determined.

$$I_1 = \frac{f_{out}}{f_{ref}} \quad (37)$$

The integer division number is obtained as:

$$N_0 = \text{floor}(I_1) \quad (38)$$

where floor(x) returns the largest integer less than x.

$$I_4 = M_4.(I_1 - N_0) \quad (39)$$

The input of dithered MASH 1-1-1-1 modulator is determined as:

$$X_4 = \text{floor}(I_4) \quad (40)$$

The input of multi-modulus MASH 1-1-1 modulator is determined as:

$$I_3 = M_3.(I_4 - X_4) \quad (41)$$

$$X_3 = \text{floor}(I_3) \quad (42)$$

The input of modified MASH 1-1 modulator is calculated as:

$$I_2 = M_2.(I_3 - X_3) \quad (43)$$

$$X_2 = \text{floor}(I_2) \quad (44)$$

The input integer number of VM-EFM1 is obtained by choosing:

$$X_1 = M_1.(I_2 - X_2) \quad (45)$$

In GSM 1800, consider the problem of synthesizing an output frequency of 1.800 GHz from a 13 MHz reference clocked. In this example, $f_{ref} = 13$ MHz, $f_s = 200$ KHz, $f_{out} = 1.80$ GHz yielding, $N_0 = 138$, $X_4 = 472, X_3 = 9$, $X_2 = 13$, $X_1 = 7$, $M_1 = 13, M_2 = 2^4, M_3 = 2^4$, and $M_4 = 2^{10}$.

In contrast, in the classical MASH 1-1-1-1, no approximation is implicated in the hybrid modulator. In particular,

$$f_{out} = \left(138 + \frac{472 + \frac{9 + \frac{13 + \frac{7}{13}}{2^4}}{2^4}}{2^{10}}\right).f_{ref} = 1.800\text{GHz} \quad (46)$$

In order to compare classical and hybrid modulators, we demonstrate simulation results. The initial states of the first stage registers are set to odd values to avoid short cycles. The simulated output power spectrum of the classical 23-bit MASH 1-1-1-1 DDSM is shown in Fig.9. The simulated output power spectral density (PSD) of the hybrid DDSM 1-2-3-4 is illustrated in Fig.10. As expected, the hybrid DDSM 1-2-3-4 achieves an almost identical PSD compared to the traditional 23-bit MASH 1-1-1-1.

B. Hardware Complexity

The proposed multi-stage Sigma-Delta modulator circuit has 4-4-4-10 bits, whose power consumption for different transistor models is presented in Table II. The clocked pulse signal frequency of 1 MHz is selected and the number of transistors in this circuit is 2503 complementary transistors. Table III compares the number of transistors and the power consumption of the conventional 1-1-1-1 MASH modulator with the proposed method. The waveform of time domain of the modulator is plotted in Fig.11 after simulation with different transistor models. Continuation of the conventional 1-1-1-1 23-bit multi-stage Sigma-Delta modulator for 3271665 input with initial conditions $e_1[0] = 1$, $e_2[0] = 0$, $e_3[0] = 0$ and $e_4[0] = 0$ with HSPICE software and manufacturing technology 0.18 micrometers are implemented.

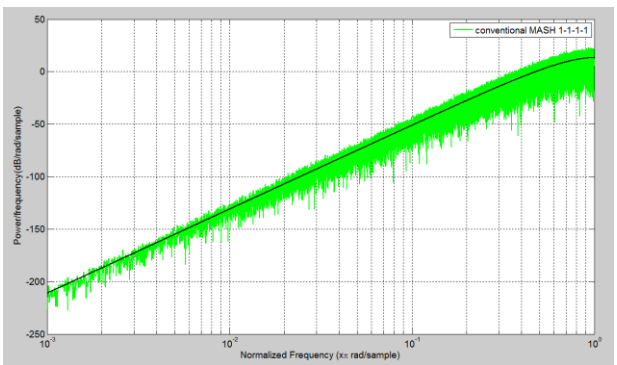


Fig.9: Simulated PSD at the output of a second-order dithered classical MASH 1-1-1-1 DDSM; the input is 3271665, $M = 2^{23}$. The solid black curve shows the PSD of the fourth-order shaped quantization noise of MASH 1-1-1-1 with second-order shaped additive LSB dither.

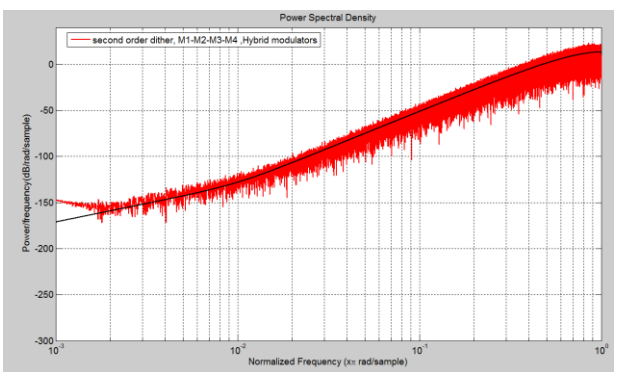


Fig.10: Simulated PSD at the output of a second-order dithered hybrid DDSM 1-2-3-4; the inputs are $X_4 = 472, X_3 = 9$, $X_2 = 13, X_1 = 7$, the modulus are $M_1 = 13$, $M_2 = 2^4, M_3 = 2^4$, and $M_4 = 2^{10}$. The FFT length is $N_f = 2^{18}$. The solid curves assume shaped white quantization noise including second-order shaped additive LSB dither.

TABLE II

COMPARISON OF POWER CONSUMPTION OF MULTI-STAGE MODULATOR STRUCTURE OF THE PROPOSED DESIGN 4-4-4-10 BITS WITH THE MODEL OF DIFFERENT TRANSISTORS N, P.

Transistor Type	Power Consumption
TT	14.06 nW
FF	75.36 nW
FS	71.09 nW
SF	16.75 nW
SS	110 nW

TABLE III
COMPARISON OF THE PROPOSED DESIGN WITH THE CONVENTIONAL 1-1-1-1 MASH SIGMA-DELTA MODULATOR.

Methods	Filip Flaps	Transistor Count	Power Consumption in TT mode
MASH 1-1-1 conventional 25-bit structure [17] (a)	78	2939	297.53 nW
Proposed DDSM4 4-4-4-10 bit (b)	74	2503	14.059 nW
a/b%	94%	85%	47 times

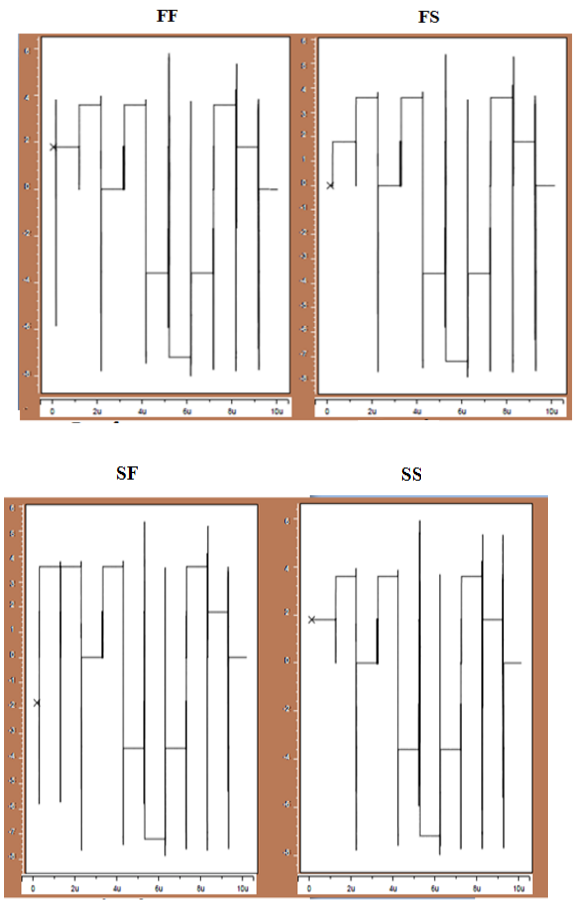


Fig .11. Time waves of the proposed Sigma-Delta modulator with manufacturing technology of 0.18 micrometers per input $X_1 = 7$, $X_2 = 13$, $X_3 = 9$, $X_4 = 472$ and modules $M_1 = 13$, $M_2 = 16$, $M_3 = 16$, $M_4 = 1024$ and the clocked pulse frequency is 1 MHz.

V. THE PROPOSED PLL CIRCUIT

In GSM450 telecommunication system, the synthesizer input frequency is 13 MHz and its output frequency is 450 MHz. In the following, the different parts of this PLL synthesizer circuit are designed.

A. *Phase /Frequency Detector (PFD)*

The PFD circuit is shown in Fig.12. The most important aspect of the phase detector (PD) design is the estimation of the reset path delay. One of the disadvantages of the phase / frequency detector circuit is the presence of a dead zone. In this case, the output pulses become so narrow that they cannot activate the charge pump circuit.

In this figure, four inverting gates are used to delay the reset path. Gates have also been used to connect the Up and Down signals to the charge pump. In this circuit, flip-flops in the Fig.13 are used. This flip-flop has normal and pulse-sensitive reversing gates. In a clocked pulse sensitive inverter gate, if the clocked pulse is equal to one, the gate is activated and if it is zero, the gate does not operate.

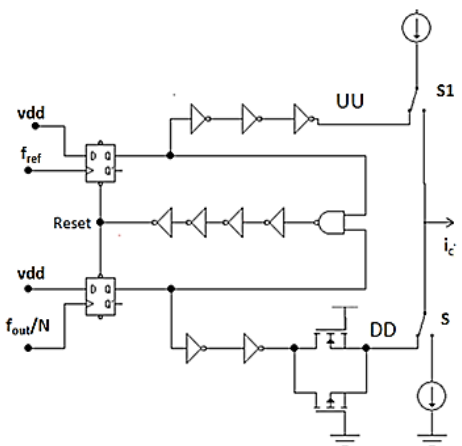


Fig. 12. PFD circuit selected in this synthesizer.

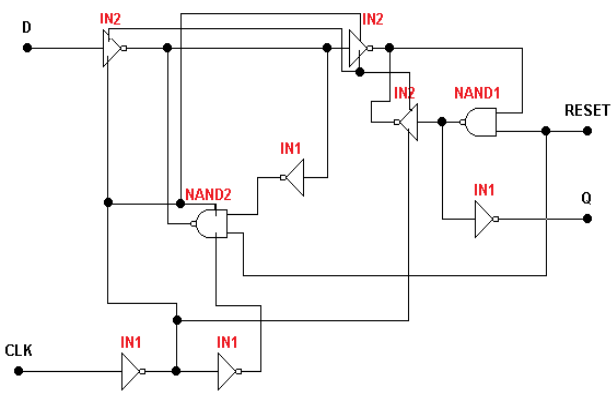


Fig. 13. The D flip-flop circuit with reset base and use of dynamic gates.

B. *Charge Pumping (CP)*

The CP circuit at the transistor level is shown in Fig.14. Transistors M_1, M_2 act as switches to reduce load injection error, undesirable reference tones, and current mismatch. Transistors M_1-M_4 perform the task of switching the charge pump. The rest of the transistors are current mirrors that repeat a certain amount of current at the output. In addition, the

current of the CP circuit is considered equal to 50 microamperes.

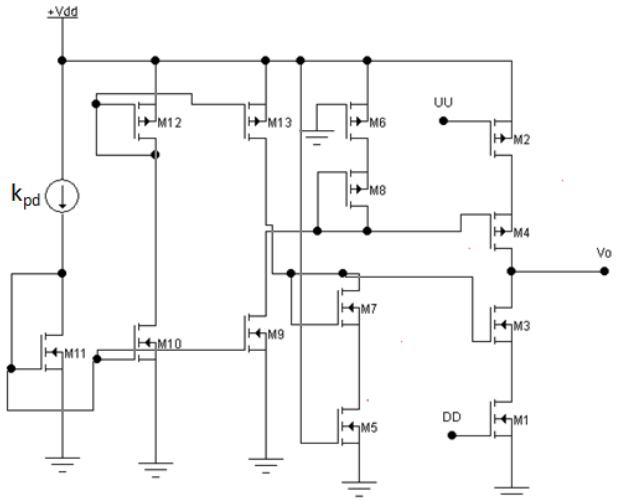


Fig. 14. CP circuit at the transistor level.

C. *Loop filter*

This synthesizer uses a third-order loop filter. This loop filter works in such a way that the response speed is reduced. The narrower the bandwidth of the filter, the lower the cut-off frequency of the filter, and consequently, the slower the loop response time to respond to changes. The circuit of this filter is shown in Fig15. The transfer function of this filter is Equ. (47). The values of the elements of this loop filter are shown in Table IV. Fig.16 shows the time domain waveforms of this PFD / CP / Loop filter.

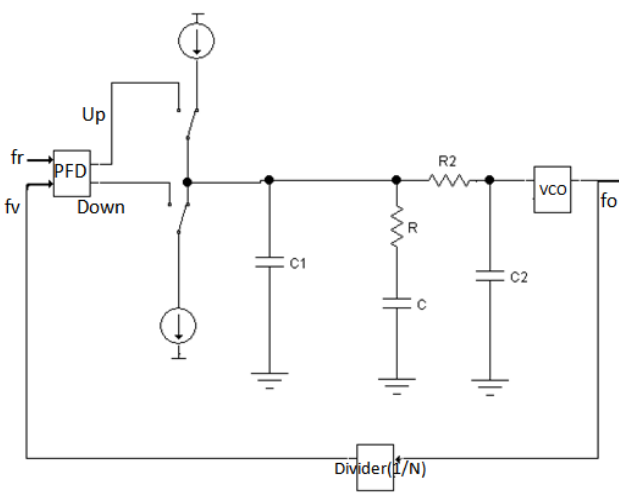


Fig. 15. The proposed CP phase locked loop circuit with a third-order filter.

$$F(s) = \frac{1+RCs}{R.R2.C.C1.C2s^3+\left((C1+C2)RC+R2.C2.(C+C1)\right)s^2+(C+C1+C2)s} \quad (47)$$

D. *Divider into feedback path*

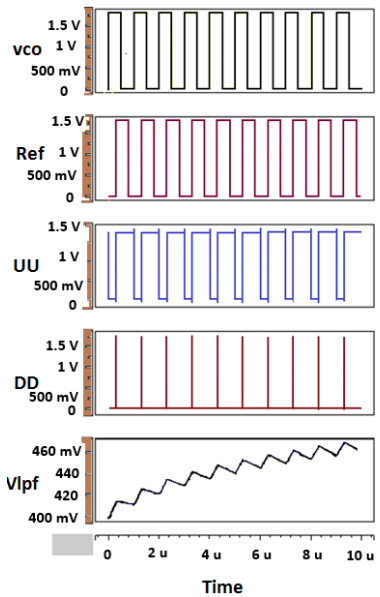


Fig. 16. Waveforms of PFD / CP / loop filter on transistor level.

TABLE IV
VALUES OF LOOP FILTER ELEMENTS IN THIS SYNTHESIZER.

Transistor Type	Power Consumption
N	30-38
f_{ref}	13 MHz
f_{out}	430-450 MHz
K_{pd}	50 µA
C_1	780 pF
C	3.4 nF
C_2	78 pF
R	3.9 KΩ
R_1	306 Ω

will use three counters, as shown in Fig17. In the proposed divider, there is a dual divider P / P + 1 (in this case 5, 6) which divides its input signal by 5, 6 according to the control input. The value of the fractional divider can be programmed as Equ. (48).

$$\mathbf{n_{frac} = 5 \times (6 + N_A) + N_B} \quad (48)$$

where N_A, N_B are the loaded numbers of counter A and B, respectively. These counters are static CMOS in full scale and operate at a frequency of 450 MHz. The time domain waveforms of this divider are shown in Fig.18.

E. *Voltage Control Oscillator (VCO)*

VCO circuits are divided into three categories. NMOS (N metal oxide semiconductor) category, PMOS (P metal oxide semiconductor) category and CMOS (Complementary metal

oxide semiconductor) category. The active circuit of the first type consists of a pair of transistors of type N, which are placed in a cross couple. The advantages of this structure are more simplicity, less noise. One of its disadvantages is its relatively high power consumption. Type P structures are made of PMOS transistors and their power consumption and noise performance are weaker. CMOS structures are made of a pair of N, P type transistors that have lower current consumption, but higher power consumption, noise, jamming capacitance, and complexity. Therefore, in this paper we use the N-type circuit. (Fig.19)

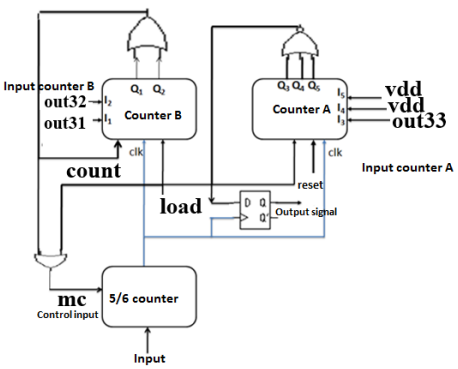


Fig. 17. Multi -module divider structure using 5,6 pre-divider and programmable counter.

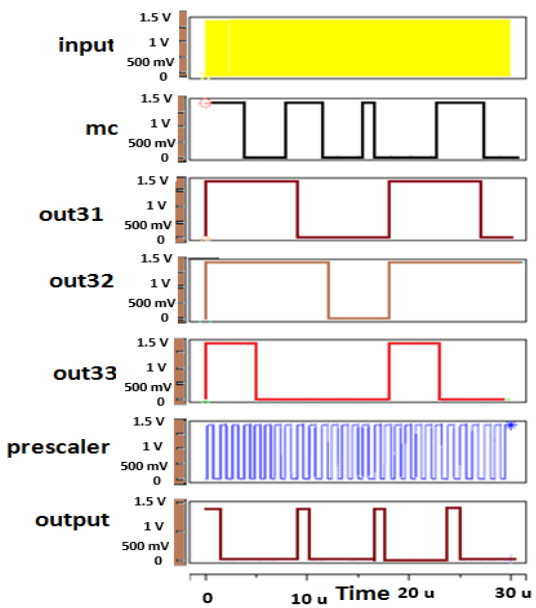


Fig. 18. The waveforms of multi modulus divider with three counters.

In the proposed phase locked loop circuit, the introduced fourth-order Sigma-Delta modulator is used.

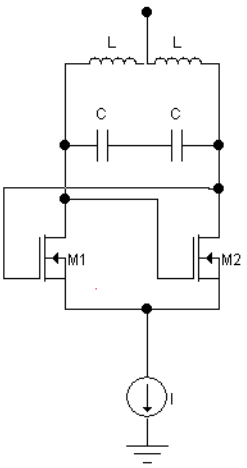


Fig. 19. The NMOS type differential tank circuit in this paper.

Table V compares the proposed method with other methods in terms of power consumption and number of transistors. As this table shows, the number of transistors in this modulator is less than other methods and has lower power consumption.

TABLE V
COMPARISON OF THE PROPOSED DESIGN WITH OTHER METHODS.

Methods	Power Consumption	Transistor Count
[4]	127 nW	2570
[18]	280 nW	2800
[22]	300 nW	2939
[28]	150 nW	2700
Proposed method	100 nW	2503

In this structure, the Carry Skip Adder (CSA) stages have been used as 1-2-3-3-5-3-3-2-1. CMOS transistors are used to make adder circuits. Each logic gate and flip flop is made by CMOS transistors and finally the number of transistors is counted. This configuration has 2939 CMOS transistors. Therefore, in total, the hardware consumption in the proposed method has reached 85% and has decreased by 15%. The total power consumption of a conventional 23-bit fourth-order structure with different transistor models is shown in Table VI, which is much higher than the proposed method.

VI. Conclusions

This paper presents a novel method for digital delta-sigma modulators (DDSMs) that can be used for precision frequency synthesizers. The hybrid DDSM 1-2-3-4 has four stages and the inputs of these stages are fixed numbers. The first stage of this modulator is programmable EFM1 and the module is not power of two. The second stage is a second-order modulator whose modulus of power of 2. The third stage is a third-order modulator with different modules and the fourth stage is a

fourth-order modulator with a dither signal. Optimal input signals are applied to each modulator to provide error masking. In this method, the input with high word length is divided into several optimal and smaller parts and each input is applied to a modulator. The proposed multi-stage Sigma-Delta modulator circuit has 4-4-4-10 bits, whose power consumption for normal transistor models is 14.08 nW. The clocked pulse signal frequency of 1 MHz is selected and the number of transistors in this circuit is 2503 complementary transistors. the conventional 1-1-1-1 MASH Sigma-Delta modulator has 2939 CMOS transistors. Therefore, in total, the hardware consumption in the proposed method has reached 85% and has decreased by 15%. It also simulates corner effects. A PLL circuit was also designed and implemented. In this PLL circuit, a frequency/ phase detector, a charge pump (CP) circuit, a third-order loop filter and a voltage-controlled oscillator (VCO) of the type NMOS are used. Meanwhile, in the feedback path of this PLL, a divider with three counters has been introduced and implemented. The waveforms of this PLL circuit were also plotted in the time domain.

TABLE VI

COMPARISON OF POWER CONSUMPTION OF CONVENTIONAL 1-1-1-1 23-BIT MULTI- STAGE MODULATOR STRUCTURE WITH DIFFERENT N, P TRANSISTOR MODELS.

Type of Transistors	Power Consumption
TT	297.53 µW
FF	355.3 µW
FS	482.3 µW
SF	339.14 µW
SS	248.42 µW

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Leila Jahanpanah received the BSc degree in Electrical Engineering from the Islamic Azad University of Arak Branch in 2005, and the MSc degree in Electrical Engineering from the Islamic Azad University Arak Branch, Iran, in 2010.She is currently a PHD. student in Electrical Engineering at the Mahshahr Branch Islamic Azad University. Her research interests include circuit theory, analog circuit design, Analog to digital modulator.



Seyed Ali Sadatnoori received his Bsc degree in Electrical Engineering from the Islamic Azad University of Dezful Branch and Msc degree in Electrical Engineering from the central Tehran branch Islamic azad university, respectively, in 2001 and 2006. He received PHD degree in Electrical Engineering from the Tehran science and research branch Islamic Azad University, in 2016. He is also an Assistant Professor of Shoushtar Branch Islamic Azad University. His current research interests include mobile ad hoc networks, wireless networks, transmitter and receiver circuits, Analog to digital modulator, integrated circuits, and neural network.



Iman Chaharmahali received the BSc degree in Electrical Engineering from the Islamic Azad University of Borujerd in 2007, and the MSc degree (Hons) in Electronics Engineering from Islamic Azad University, Arak, Iran, in 2010, where he is currently working toward the PHD degree in Electronics Engineering. His research interests include circuit theory, analog circuit design, modelling, and simulation, artificial neural networks and nano electronic.

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