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Design of Low Power Full-Adder Circuit Using Quantum-dot Cellular Automata

Faezeh Motalebi[1] ,and Samira Sayedsalehi[2, †]

[1]Department of Computer and IT Engineering, Qazvin Branch, Islamic Azad University, Qazvin, Iran
[2]Department of Computer Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran

ABSTRACT

Quantum-dot Cellular Automata (QCA) is a new technology for eliminating some of the problems of existing technologies such as CMOS. Some of the key advantages of QCA are an intersection of wires in the same plane, high speed, small area, power consumption, complexity and low cost. Employing a three-input majority gate, a five-input majority gate and three logic gates, this study presents a full-adder circuit in a single layer which for higher efficiency and avoiding much complexity and based on the function of the intended full-adder circuit, the five-input gate is proposed. The proposed full-adder circuit and the proposed ripple adder circuit are compared with previous designs regarding complexity, number of cells, and area and the results are reported. Moreover, proposed circuits' power consumption has been calculated by using QCApro. These results indicate that the proposed full adder design in comparison with previous similar design achieved 36%, 20% and 4.4% reduction in the number of cells, latency and power consumption, respectively.

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Computational circuits, Full adder, Majority gate, Quantum cellular automata.

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I. INTRODUCTION

In recent decades, Metal Oxide Semiconductor (MOS) has been the current technology. The remarkable rise in integration of integrated circuits has raised issues such as an increase in power consumption, limited integration density and limitation in system scaling [1]. As CMOS transistors' size reduced to Nano scale, this technology encountered serious problems and challenges such as high leakage current, reduction in gateway control, high power consumption, high lithography cost, etc. These problems slow the process of reduction of the size and therefore challenge the ability of CMOS technology for creating structures with high density and efficiency in the near future. To overcome this limitation, Quantum cellular automata (QCA), which is one of the solid state Nano-electronic devices and a member of quantum dot, is proposed as an alternative to replace the existing CMOS circuits. The basic element of QCA is a cell which consists of four quantum dots and two electrons. In this technology most of the circuits are produced based on three-input majority gates, five-input majority gates and logic gates [2], [3]. One of the most important circuits which is examined in any technology is adders. So far, many adders have been introduced in QCA [4]-[11]. The most important factor in an efficient design is designing one layer with minimum cells and power level. In this study, by employing a three-input majority gate, a five-input majority gate, and three logic gates a circuit in one layer was proposed; simplicity of design resulted in high efficiency in wider computational circuits. Moreover, after calculating its power consumption, it could be said that the proposed design was more functional and with more favorable outcomes. In section 2, we present a brief description of material, structure, and components of QCA circuits. In section 3, we introduce former QCA full adder circuits. In section 4, we introduce our proposed circuits. In section 5, we simulate the circuits and examine the results. And in the last section the findings are presented.

†**Corresponding Author**: s_sayedsalehi@azad.ac.ir
Tel: +982188830826, Islamic Azad University, South Tehran Branch
Faculty of Electrical and Computer Engineering, Islamic Azad University, South Tehran Branch, Tehran, Iran

II. A REVIEW OF QCA

A. Preliminary materials and devices

Quantum Cellular Automata was first presented by professor Lent at The University of Notre Dame in 1993. The two existing arrangements in Quantum Cellular Automata are one with polarization of P=+1 as logic 1 and one with polarization P=-1 as logic 0. In QCA two wiring methods, standard and inverter, are used (Fig. 1) [12]. The wires cross over each other in several ways such as coplanar-based wiring method, multilayer-based wiring method, and clocking-based method in which two wires can cross each other without affecting each other (Fig. 2) [13].

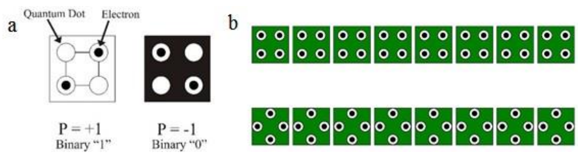

Fig. 1. (a) Basic QCA Cell and Binary encoding; (b) Standard and inverting wiring.

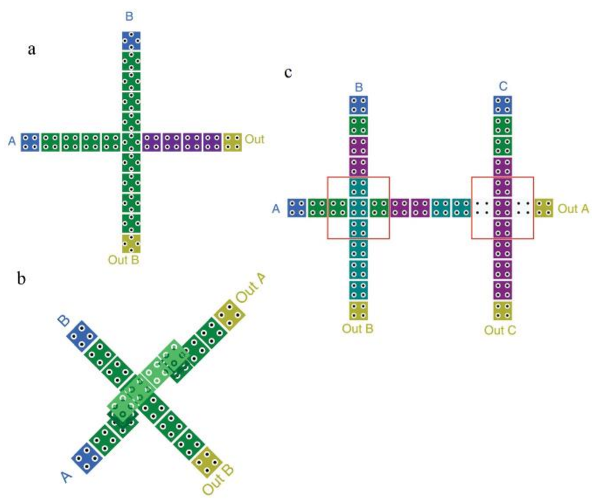

Fig. 2. (a) Crossover based on coplanar-based wiring, (b) Crossover based on multilayer-based, (c) Crossover based on clocking-based wiring [4].

B. Basic elements in QCA

The basic elements in QCA circuits are logic gates, three-input majority gate, and five-input majority gate.

1) Logic Gate: It is the simplest way for placing a cell obliquely next to another cell; other methods are also based on it. Another method is the inverting signal in layers (Fig. 3(a)) [14].

2) Three-input majority gate: A three-input majority gate or majority voting includes three inputs and one output in which the polarization of the output cell is determined by the polarization of input cells (Fig. 3(b)) [15].

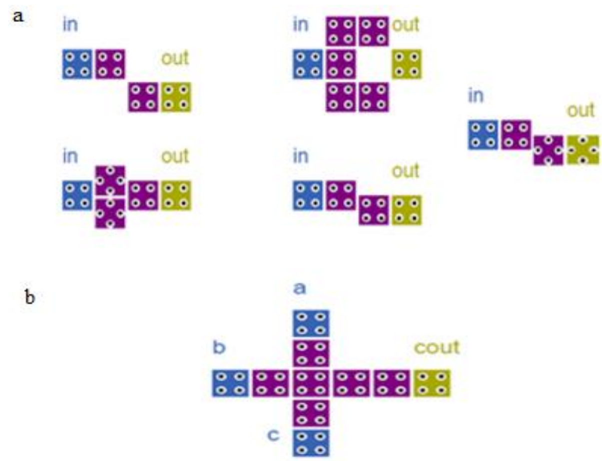

Fig. 3. (a) Some inverting structures, (b) Three-input majority gate.

3) Five-input majority gate: In order to decrease the number of consumption majority gates and to optimize circuits, scientists began to design a five-input majority gate. The first designs were proposed by Navi et al in 2010. In 2011, Akeela and Wagh, and in 2014 Roohi et al proposed their own designs to improve the previous methods. The five-input gate proposed by Sheikhfaal et al, called PM5, was presented in 2015 (Fig. 4).

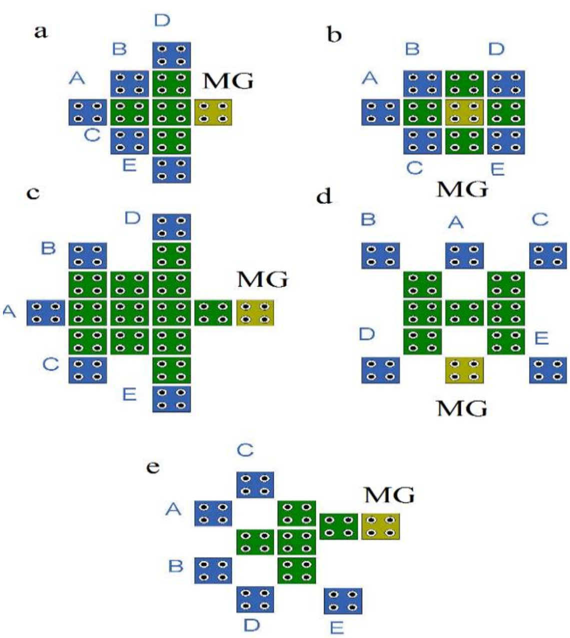

Fig. 4. Four proposed designs for five-input majority gate: (a) The structure proposed by Navi et al [5], (b) The structure proposed by Navi et al [6], (c) The structure proposed by Akeela and Wagh [16], (d) The structure proposed by Roohi et al [17], (e) QCA five-input gate [18].

C. Power Consumption

Since there is no electricity flow in computations of QCA, power consumption is far less than CMOS. The most precise models for calculating power dissipation were proposed by Lent and Timler in 2002. Moreover, Liu et al proposed upper bound power dissipation in 2012. At first, the formula of power was expanded by Lent and Timler, the total power and energy from QCA cells could be calculated by using a Hamiltonian matrix in which for each array of QCA cells, Hartree-Fock approximation is used [19], by taking into account the Coulombic interaction effect among them, a mean square approach, like refer to Equ. (1), is introduced [20], [21]:

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i c_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i c_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}(c_{j-1}+c_{j+1}) & -\gamma \\ -\gamma & \frac{E_k}{2}(c_{j-1}+c_{j+1}) \end{bmatrix} \tag{1}$$

Here, γ is tunneling and c_i is the polarization taken from cell ith, and $f_{i,j}$ is the geometric model that determines the electrostatic interaction between cells (i, j) with regard to geometric distance. With regard to the distance of adjacent cells, the factor $f_{i,j}$ is included in King's energy definition (E_k). This energy, with the energy cost of 2 QCA cells with opposing polarization, is calculated in referring to Equ. (2) [17]:

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n-1}^{4}\sum_{m=1}^{4}\frac{q_{i,n}q_{j,m}}{|r_{i,n}-r_{j,m}|} \tag{2}$$

QCA cell energy in each clock cycle is calculated in referring to Equ. (3):

$$E = \langle H\rangle = \frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda} \tag{3}$$

$\vec{\Gamma}$ is the vector of the energy area from a cell affected by its adjacent cell. ħ is the reduced Planck's constant and $\vec{\gamma}$ indicates coherence. The Hamiltonian vector is presented as corresponding to the Hamiltonian definition (Refer to Equ. (4)):

$$\vec{\Gamma} = \frac{1}{\hbar}[-2\gamma, 0, E_k(c_{j-i}+c_{j+1})] \tag{4}$$

$(c_{j-i} + c_{j+1})$ is the total of adjacent polarizations. As shown in Fig. 5, the power flow of a QCA cell, which has been placed in a binary wire, has been classified into 4 major signal flow [20], [22]. Horizontal signal powers are equal, in which the input power is the signal power taken from the left neighbor and the output signal is the freed signal power to the right-hand cell. During the switch, the gradual increase of inter dot barriers results in transference of the intended amount of the energy to the cell (switch phase) and these barriers decrease in P_{clock}; therefore, the energy returns to a clocking circuit and negligible power dissipation in the clocking circuit is called P_{diss} [21].

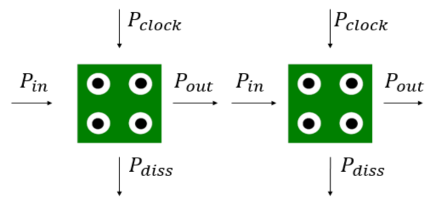

Fig. 5. Power flows in a pair of adjacent cells

The equation for the total power could be calculated this refer to Equ. (5):

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{\vec{\lambda}}{dt}\right] = P_1 + P_2 \tag{5}$$

In Equ. (5), P_1 includes two major components: first, the power increase is the result of the difference between the input signal and the output signal. Second, clocking power transferred to a cell (P_{clock}). P_2 indicates dissipated power, P_{diss} [22]. Power dissipation during a cycle-hour T_{cc}= (-T, T) could be defined as Hamiltonian terms and correlation vectors (refer to Equ. (6)):

$$E_{diss} = \frac{\hbar}{2}\int_{-T}^{T}\vec{\Gamma}.\frac{d\vec{\lambda}}{dt} = \frac{\hbar}{2}\left(\left[\vec{\Gamma}.\vec{\lambda}\right] - \int_{-T}^{T}\vec{\lambda}.\frac{d\vec{\Gamma}}{dt}\right) \tag{6}$$

It is worth mentioning that the highest energy dissipation occurs when the rate of the change of $\vec{\Gamma}$ is at its highest. Therefore, $\vec{\Gamma}$ + is shown as $\vec{\Gamma}$ (+T) and $\vec{\Gamma}$- is shown as $\vec{\Gamma}$(-T). The upper bound of power dissipation can be calculated in referring to Equ. (7):

$$P_{diss} = \frac{E_{diss}}{T_{cc}} < \frac{\hbar}{2T_{cc}}\vec{\Gamma}_{+} \times \left[-\frac{\vec{\Gamma}_{+}}{\left|\vec{\Gamma}_{+}\right|}tanh\left(\frac{\hbar\left|\vec{\Gamma}_{+}\right|}{K_B T}\right) + \frac{\vec{\Gamma}_{-}}{\left|\vec{\Gamma}_{-}\right|}tanh\left(\frac{\hbar\left|\vec{\Gamma}_{-}\right|}{K_B T}\right)\right] \tag{7}$$

K_B is Boltzmann constant and T shows heat. In one array of similar QCA cells, the total power dissipation is the sum of power dissipations of all the cells as shown power dissipation is the same for each QCA cell [21]. Using this information, Srivastava et al in 2011 proposed a power dissipation model for QCA circuits based on dividing the total power into leakage main component and switching. The power dissipated during clock changes (from top to bottom and from bottom to top) brings about power leakage and the power dissipated due to a period of change results in power change. Based on this model an assessment device called QCApro has been designed. This device assesses the maximum, the minimum and the average of power dissipation in QCA structure under a change without deadlock. In addition, this device can be used to investigate the efficiency of the circuit based on Bayesian network analysis [23].

III. Previous Research (Literature Review)

Different quantum cellular automata designs can be compared with each other based on occupation area, consumed cell count in the model's structure, examining the kind of wiring, delay in the release of the model in terms of used clock cycle (the number of clocking zones), and output polarization. Full-adder circuits are from combined circuits which have a variety of functions in digital circuits. In quantum cellular automata technology, there are three major structures for designing full-adder circuits whose differences lie in their elements and the arrangement of their elements. Since 1994, various models have been proposed based on logical gates and three-input majority gates. In 2007, Azghadi designed a full adder using a five-input majority gate for the first time in which most of the structures were designed multi-layers [24]. In 2012 and 2015, Hashemi et al. along with Navi, using Azghadi's model, presented two structures with multi-layer rule and clocking rules for designing [7], [8]. In 2010, Navi et al. presented two five-input majority gates (Fig. 4.(a) and 4.(b)) and proposed their suggested circuits based on them [5], [6]. Moreover, in 2016, Newaz Bahar and Waheed, like other designs, proposed their own design in three levels [11]. In 2011, Sayedsalehi et al. proposed two new implementations for multi-layer design which, be compared with all other designs, had lower cell counts and smaller occupation area [9]. In 2016, Labrado and Thapliyal designed a model in a single layer which in terms of cell count, delay, and environment, compared with other designs, has a better performance [10]. In 2016, Angizi et al. (Fig. 6) proposed a model which has a new quantum cellular automata design based on XOR [4].

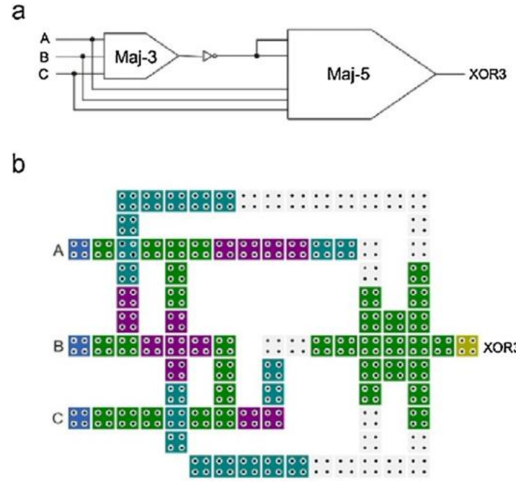

Fig. 6. (a) The logical schema of full adder by, (b) The circuit proposed in [4].

IV. The Proposed Design

The proposed circuit is based on the full-adder circuit of Angizi et al. in tools 2-0-3, QCADesigner; this tool was developed by Walus et al. in ATIPS laboratory for drawing arrangement and simulating quantum cellular automata digital circuits [25] and consists of one five-input majority gate, one three-input majority gate and three logical gates [4]. In Fact, the carry out function of full-adder is output of the three-input majority gate.

A. The Proposed Five-input Majority Gate

Since the five-input majority gate designs that have so far been proposed are not satisfactory, with studies and research we have suggested different changes in the location of inputs which can be observed in Fig. 7. The inputs of the proposed five-input gate are a, b, c, and d in which the input b is somehow considered as two inputs.

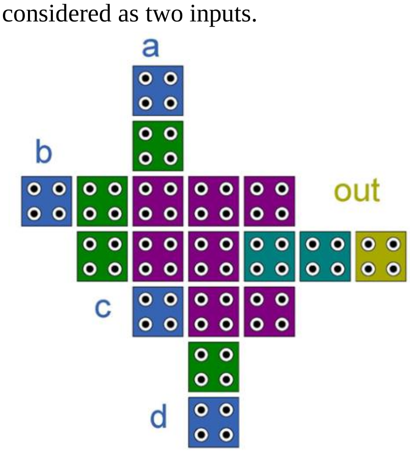

Fig. 7. The proposed five-input gate

B. The proposed full-adder circuit

In this circuit we use three logical gates of which two are simple logical gates and the other is the logical gate shown in Fig. 3 (a). In the next step, for crossing wires we employ clocking rules so that two wires with different hour-phases cross without affecting each other; this is an efficient way for wire-crossing in a single layer (Fig. 2 (c)). In the end, the proposed plan is presented based on the given explanations. At first, three inputs a, b, and c enter the three-input majority gate and generate Cout, then by reversing Cout and by double reversing of wire a, which is used because of adjacency of two input cells of five-input majority gate and because of the attempt to keep the circuit single layer, we produce five-input majority gate and acquire output sum. The results of output sum and Cout after one output are displayed, as shown in Fig. 8. This design includes 59 quantum cells in a space of 0.07 square micrometer, in this design release delay is one cycle-hour which, be compared with Angizi's design, has smaller occupation area and lower delay. One of the reasons for efficiency of this design is its single layer design which reduces the power consumption considerably and results in higher efficiency of wider computational circuits; inputs are at one end and outputs are at the other end of and outside the circuit which accelerates wider computational operations (Fig. 8.). Moreover, because it is a single layer and inputs and outputs are not enclosed, we can easily calculate its power by using QCAPro software. Compared with all other single layer designs which have been presented until now, this design is more efficient in terms of area, delay, and cell count which, in turn, reduces the costs be compared with other single layer designs.

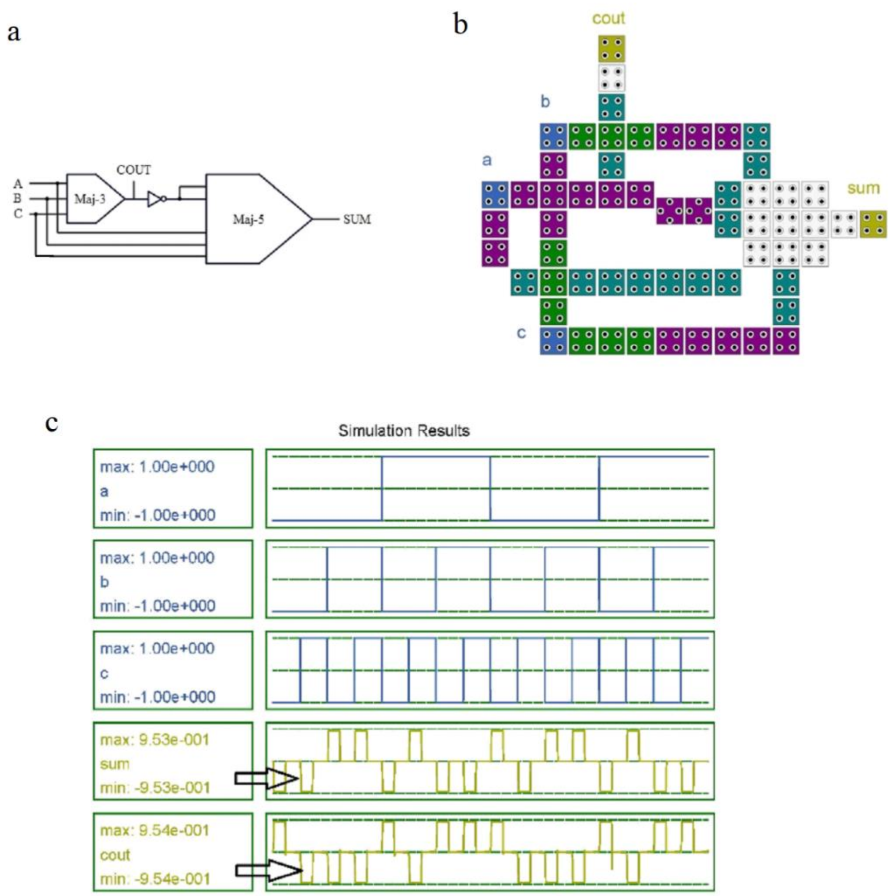

Fig. 8. (a) Schematic design based on Angizi's design, (b) cell layout in the proposed plan, (c) Output result of simulation of the proposed plan.

C. The Proposed Four-bit Ripple Adder Circuit

By placing four adders near each other, we design a four-bit ripple adder in a way that the first adder includes three inputs a_0, b_0, and c_0 and two outputs $Cout_0$ and sum_0 and $Cout_0$ is also the input c1 for the adjacent circuit; this process continues up to the fourth circuit (Fig. 9). Here, the important point is that for the purpose of synchronization it is necessary that outputs and inputs enter the circuit at the same time; it is, therefore, essential that we add to our design some cells with appropriate timing. As can be seen in Fig. 9, in the first full adder the inputs enter without any delay and the output occurs after a 4 cycle-phases delay. In this way, the next full adder, one of whose inputs results from the first circuit's output and enter after one cycle-phases delay and the output is displayed after a three cycle-phases delay; the third cycle, one of whose inputs is from the second circuit's output, enters after a two cycle-phases delay and the output exits after a two cycle-hour delay. Eventually, in the fourth full adder, one of whose inputs like other full adders is from the previous full adder, i.e., the third full adder, the inputs enter after a three cycle-phases delay and the output exit after one cycle-phases delay. This timing in four-bit ripple design brings about synchronization of the inputs and outputs of the proposed four-bit ripple adders.

In order to show the output result of simulation better, we classify the inputs and the outputs into three groups based on the Bus Layout option. Then, in order to show the accuracy of the result of the output of the simulation, we assign values to the inputs, for example, the sum of 1101 and 0011 is 10000 and as can be seen in the Fig. 10, through marking the result of the simulated output occurs like the figure in one column. Our proposed four-bit ripple adder design includes 379 quantum cells in a space of 1 square micrometer; in this design there is a four cycle-phases release delay; it is compared with the previous four-bit ripple adders in the table which is more efficient in terms of area, cell count, delay, and cost.

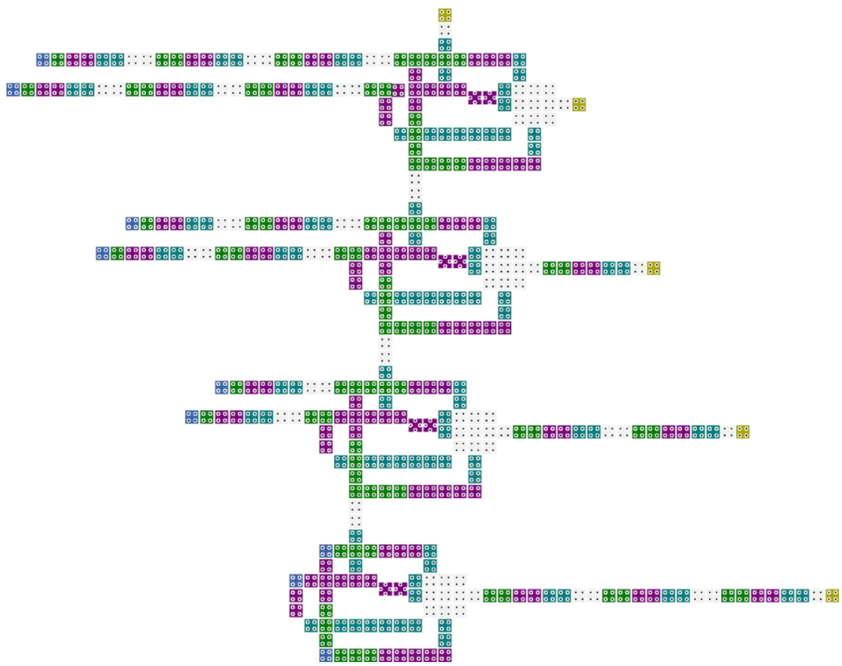

Fig. 9. The layout of four-bit ripple adder circuit

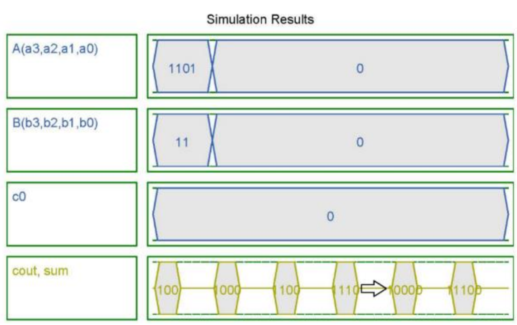

Fig. 10. The simulated output after initialization.

V. Simulation and Comparing the Results

A. *Simulation of Power*

To calculate power, version 1.4-1 of QCApro tools is required which operates through QCADesigner 1.1-4 software using C ++ / C programming language in Linux environment or using Ubuntu in the Windows operating system which is a set of techniques for analysis of configured data based on INUS theory. This simulation can be a quick design for checking the value of the outputs of all the inputs; in single-layer adder circuits if there is an error, it will create the error message, therefore it is a modeling tool for probable error and power dissipation in circuits. QCApro estimates the minimum, the mean, and the maximum of power dissipation [23], [26]. All the input majority gate designs introduced in Fig. 4 are examined through three different tunneling energy levels (0.5 E_k, 1 E_k and 1.5 E_k) in heat of 2K and power dissipation is shown by 0.5 E_k in Fig. 11.

Obviously high power dissipation cells are shown by using heat points with darker colors. It is obvious that in presented designs the mid-cells or voter cells have higher power dissipation than other cells and thus the set position of input cells is like other cells and their effect on the voter cell can be taken as one of the significant functions in increasing power dissipation. Compared with previous designs, the proposed five-input majority gate design includes fewer cells with dark colors (Fig. 12); it is a standard design [18].

Moreover, in the proposed design we observe fewer dark-colored cells be compared with Angizi's design which, as was mentioned earlier, is indicative of the proposed model's standard design in lower level of energy dissipation in a single layer (Fig. 13).

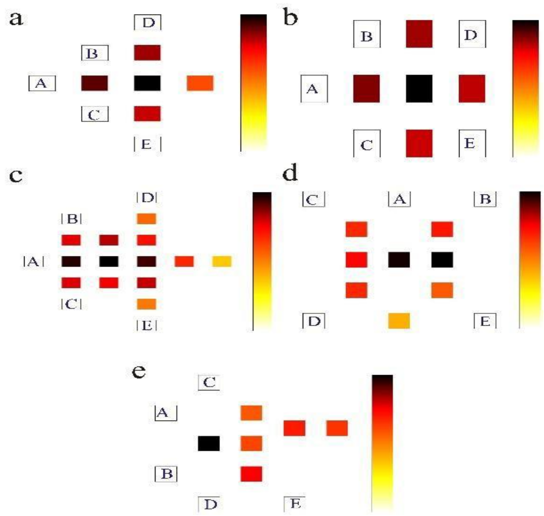

Fig. 11. Power dissipation map for five-input majority gates in heat 2K and with 0.5 E_k, [18] (a) The structure presented by Navi et al., (b) The structure presented by Navi et al., (c) The structure presented by Akeela and Wagh, (d) The structure presented by Roohi et al., (e) The structure presented by Sheikhfaal et al.,

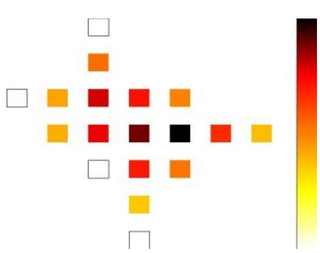

Fig. 12. Power dissipation map for proposed five-input majority gate in heat 2K and 0.5 E_k.

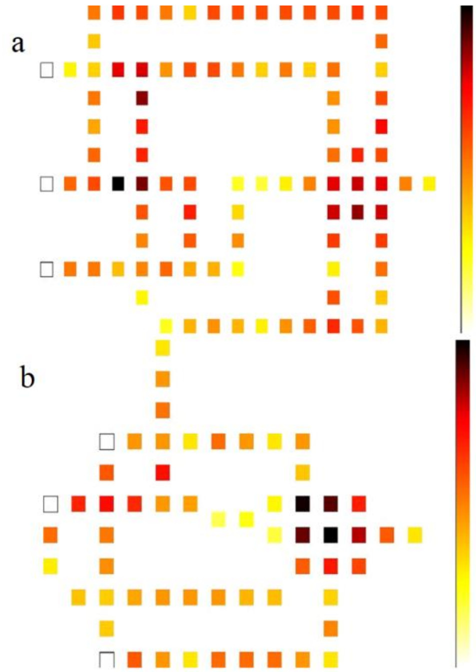

Fig. 13. (a) Power dissipation map for Angizi's full-adder design in heat 2K and with 0.5 E_k, (b) Power dissipation map for the proposed full-adder design in heat 2K and with 0.5 E_k

B. Comparing Circuits' Results

Now, we compare the implementations carried out in research papers. Table I compares the structures proposed for one-bit full-adder circuits and four-bit ripple adder circuits according to occupation area, cell count, and release delay in terms of the cycle-hour and the number of layers.

C. Comparing Power Consumption

All consumption power maps for five-input majority gates are examined through three different tunneling energy levels (0.5 E_k, 1 E_k and 1.5 E_k) in heat 2K. Table II compares the structure proposed for five-input majority gates and average leakage energy dissipation, average switch energy dissipation and total energy consumption at three levels. Since the inputs are applied from one side and with appropriate distance (Fig. 13(b)), cell count in its single-layer direction is more than previous designs too which increases total energy consumption compared with designs with lower cell count. It should be noted that the proposed design includes fewer dark-colored cells compared with other designs which is indicative of standard design of the proposed design at lower level of energy dissipation at one level.

Since the proposed circuit is a single layer, it was examined using QCApro and its power consumption was implemented; examining Table II we observe low power consumption and fewer cells with dark colors. Table III compares leakage energy values, switch energy, and total energy consumption in the proposed full-adder circuit with Angizi's design at three different tunneling energy levels of (0.5 E_k, 1 E_k and 1.5 E_k).

It is clear from Table III that be compared with Angizi's design, the proposed design has lower power consumption at three different tunneling energy levels. This is indicative of an optimal design in comparison with full-adder circuits in one level. These results indicate that the proposed full adder design in comparison with pervious similar design [4] is achieved 36%, 20% and 4.4% reduction in the number of cells, latency and power consumption, respectively.

VI. Conclusion

This study was concerned with designing an efficient full-adder circuit by using quantum cellular automata technology. The cell count and occupation area of a particular design in QCA technology directly affect the cost of building circuits based on this technology. Avoiding the problems of previous circuits, this paper proposed an effective design that enhanced efficiency, simplicity, and regularity of full-adder circuits inquantum cellular automata technology. Due to its occupation area, the proposed circuit was capable of performing in different heats. Another advantage of this design is that the circuit's inputs and outputs were not located in the center of the design in two opposite positions. Therefore, it could be used to build multi-bit adder circuits and wider computational circuits. Since it was a single layer, its consumption power can be calculated. Be Compared with all the other single layer designs, this design was more efficient in terms of area, delay and cell counts which, in turn, help to reduce the costs. Finally, it could be said that this design had a better function, produced more satisfactory results.

TABLE I

COMPARISON BETWEEN THE STRUCTURES PROPOSED FOR ONE-BIT FULL-ADDER CIRCUITS AND FOUR-BIT RIPPLE ADDER CIRCUITS IN QUANTUM CELLULAR AUTOMATA TECHNOLOGY

Circuits	Types of circuits	Cell count	Area (nm^2)	Latency (clock cycle)	Single layer	Circuits	Types of circuits	Cell count	Area (nm^2)	Latency (clock cycle)	Single layer
Design in [7]	FA[1]	79	0.05	1.25	No	Design in [9]	FA	33	0.02	0.75	No
	RA[2]	308	0.29	2	No		RA	-	-	-	-
Design in [8]	FA	71	0.06	1.25	Yes	Design in [4]	FA	93	0.07	1.25	Yes
	RA	442	1	4	Yes		RA	-	-	-	-
Design in [5]	FA	73	0.04	0.75	No	Design in [10]	FA	63	0.05	0.75	Yes
	RA	-	-	-	-		RA	-	-	-	-
Design in [6]	FA	61	0.03	0.75	No	Design in [11]	FA	48	0.03	0.75	No
	RA	-	-	-	-		RA	-	-	-	-
Design in [9]	FA	31	0.02	0.75	No	Propoed Design	FA	59	0.07	1	Yes
	RA	178	0.17	2.4	No		RA	379	1	4	Yes

TABLE II

COMPARING THE PRESENTED STRUCTURE FOR FIVE-INPUT MAJORITY GATES, THE RESULT OF ANALYZING AVERAGE LEAKAGE ENERGY DISSIPATION, SWITCH ENERGY DISSIPATION, AND TOTAL ENERGY CONSUMPTION

circuits	cell count	Area (nm^2)	Single layer	Avg. leakage energy dissipation (mev)			Avg. switching energy dissipation (mev)			Total energy consumption (mev)		
				$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
Design in [5]	10	0.007	NO	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
Design in [6]	10	0.004	NO	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
Design in [16]	18	0.02	YES	3.44	10.67	19.52	32.66	29.89	27.01	36.1	40.56	46.53
Design in [17]	13	0.01	YES	3.38	8.95	15.03	9.23	7.7	6.41	12.61	16.65	21.44
Design in [18]	11	0.01	YES	2.99	7.73	12.35	3.69	2.77	2.15	6.68	10.5	14.5
Proposed design	18	0.02	YES	3.74	11.67	21.38	33.63	30.57	27.04	37.37	42.25	48.78

[1] Full Adder
[2] Ripple Adder

TABLE III
THE RESULT OF ANALYZING AVERAGE LEAKAGE ENERGY, SWITCH ENERGY, AND TOTAL ENERGY CONSUMPTION IN THE PROPOSED FULL-ADDER CIRCUIT

circuits	Avg. leakage energy dissipation (mev)			Avg. switching energy dissipation (mev)			Total energy consumption (mev)		
	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
Design in [4]	26.27	80.93	146.71	160.23	141.55	122.8	186.49	222.49	269.51
Proposed design	24.19	75.21	135.78	154	135.71	117.96	178.19	210.92	253.73

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Faeze Motalebi recieved her bachelor Degree in software computer engineering in 2013 from Islamic Aazad University Malard Branch, and her M.Sc. degree in computer architecture engineering in 2017 from Islamic Azad University Qazvin Branch. Her M.Sc thesis was about Full_Adder Circuit using Quantum-dot Cellular Automata. Her research interests include Quantum-dot Cellular Automata, nanolectronic.

Samira Sayedsalehi received her M.Sc. degree in computer architecture engineering in 2008, and her Ph.D. in computer architecture engineering in 2012 from Science and Research Branch of Islamic Azad University, Tehran, Iran. She is currently Assistant Professor in Faculty of Computer Engineering of South Tehran Branch, Islamic Azad University. Her research interests include Nano electronics with emphasis on Quantum-dot Cellular Automata, CNFET, Computer Architecture, and Computing.