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Development of Quasi Z-Source Inverters Based on Diode-Cells: Analysis and Implementation

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ABSTRACT

This paper proposes two newly developed quasi Z-source inverters (QZSI) based on two new diode-cells. The proposed inverters are called continuous diode assisted quasi Z-source inverter (CDQAZSI) and discontinuous diode assisted quasi Z-source inverter (DDQAZSI). These inverters are thoroughly examined in three modes: two-cell QZSI, three-cell QZSI, and n-cell QZSI that is called developed QZSI. Additionally, the equations of the diodes' voltage and current, capacitors' voltage stress, boost factor, inductor currents, and dc-link current are computed. All equations are given for the proposed generalized topologies. The major advantage of these inverters is the potential of deriving desired boost factor value devoid of extra elements. Furthermore, increasing the number of the diode-cells used in the proposed QZSI reduces the values of dc-link current, inductor current, and diode current. Lastly, to verify the performance of the proposed topologies, the practicality of the proposed QZSI is authenticated by experimental results through a laboratory prototype.

Article Info

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I. INTRODUCTION

Two types of conventional inverters are voltage and current source inverters. The magnitude of input dc voltage in voltage source inverters is less than the magnitude of the effective output voltage, so these inverters function as buck inverters. However, current source inverters function as boost inverters. Individually, these inverters do not function in the buck-boast mode. Furthermore, in voltage source inverters, electromagnetic interference or error gating of power switches will short-circuit the switches of the inverters while an open circuit of the switches will occur when similar conditions occur for current source inverters. These phenomena destroy the inverter [1-4]. Consequently, Z-source inverters (ZSIs) were presented in 2003 by Peng to resolve these limitations [1]. ZSIs are composed of an X-shaped connection of two capacitors and two inductors. ZSIs function in two modes of operation, the shoot-through (ST) and non-shoot-through (non-ST) states. The output voltage magnitude can be controlled, i.e., increased or reduced in the ST state. Therefore, ZSIs have buck-boost functionality. The buck-boost functionality is a major advantage of ZSIs when compared to traditional voltage and current source inverters. Other merits of ZSIs are less distorted output waveform and high reliability [5-6]. Applications of ZSIs are hybrid electric drives, PV systems, motor drives, wind power, distributed generations, and solar cell systems [6-9].

There are different control methods for ZSIs, among which the major ones include the maximum constant boost control method, the maximum boost control method, the simple boost control method, and the maximum boost control method with third-harmonic injection [10-12]. These control methods have their own advantages and disadvantages. This paper focuses on the simple boost control method.

Since the introduction of conventional ZIS topology, various ZSI topologies have been published. Extended boost switched-

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inductor/active-switched-capacitor quasi-Z-source inverters [13], L-Z-source inverters [14], half-bridge Z-source converters [6], gain half-bridge switched-boost inverters [7], switched-coupled-inductor quasi-Z-source inverters [15], quasi-switched boost inverters [16], quasi-Z-source cascaded hybrid five-level inverters [17], and a group of single-phase Z-source AC-AC converters with magnetic coupling and safe-commutation strategy [18], switched boost inverter using a transformer [19], extended switched-inductor quasi-Z-source inverters [20], and new switched-inductor quasi-Z-source inverters [21] are some of the ZSIs presented. Moreover, other quasi-Z-source inverters were presented in [22-24].

The low boost factor is the major disadvantage of these topologies. The boost factor value is increased by increasing the duty cycle of the ST state. Nevertheless, a new drawback of low value for modulation technique is introduced. Applying a dc-dc converter is another strategy for increasing the boost factor value, which also results in increased cost and weight of the inverter.

Two newly developed QZSIs are proposed to solve the disadvantage of the low boost factor and the other disadvantages. These inverters are based on two new diode-cells as basic units. Additionally, the proposed topologies are thoroughly analyzed and the equations of the diode voltage-current stress, capacitor voltage stress, boost factor, inductor currents, and dc-link current are computed in these inverters. The boost factor value is increased when more of the proposed basic units are used, which in turn decreases the diode and inductor current values. These are some merits of the proposed inverter. Lastly, the accurate operation of the proposed QZSI is proven by means of experimental results.

II. PROPOSED TOPOLOGY

The power circuits of the diode-assisted quasi Z-source inverters (DAQZSIs) are illustrated in Figs. 1(a) and (b), respectively [22]. Each inverter is made-up of one diode-cell and one conventional Z-source inverter. Individual diode cells as a new basic unit comprise of two diodes, one inductor, and one capacitor. As shown in Fig. 1, based on the connection of the elements used, there are two different states for the DAQZSI. The current of the input dc source will be continuous if the inductance of the basic unit is series-connected to the input dc source. This inverter is called a continuous diode-assisted quasi Z-source inverter (CDAQZSI) and is shown in Fig. 1(a). Otherwise, the current of the input dc source is discontinuous if the last inductance is not connected series. This inverter is shown in Fig. 1(b) and is called a discontinuous diode-assisted quasi Z-source inverter (DDQAZSI). The modulation strategies of the proposed QZSIs are as same as conventional ZSIs.

This proposes two newly developed DAQZSIs that are thoroughly analyzed. In these inverters, the capacitor and inductor values are deemed equal. The various stages of analysis use a current source and a power switch S to model the single-phase inverter. Additionally, the general equations are calculated for the voltage and current of all elements used, so the boost factor equation is calculated.

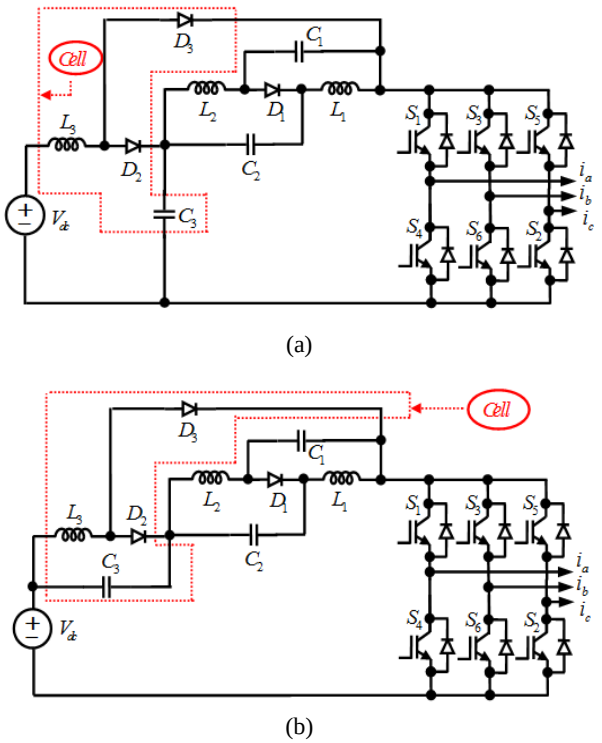


Fig. 1. The power circuit of DAQZSI topologies based on one diode-cell; (a) continuous state; (b) discontinuous state

A. *Proposed CDAQZSI*

This sub-section proposes the new topology for the QZSI based on a diode-assisted basic unit and in the continuous current state. The new topology is analyzed with respect to the use of two basic units, the use of three basic units, and finally, its developed topology. Moreover, the voltage equations of capacitors and diodes and the current equations of inductors, diodes, and dc-link are calculated in addition to the equation of the boost factors for all states.

B. *Proposed CDAQZSI Based on Two Diode-cells*

Fig. 2 illustrates the proposed CDAQZSI power circuit. The proposed topology is derived from incorporating two diode-cells into the traditional ZSI. The proposed topology is composed of four inductors, four capacitors, and five diodes. Two states of operation are possible in the proposed topology, shoot-though and non-shoot-through states. Switch S and diodes D_3 and D_5 conduct while diodes D_1, D_2, and D_4 are turned off during the ST state. During this mode, the input voltage and capacitors charge the inductors. During non-ST state, diodes D_1, D_2, and D_4 conduct while switch S and diodes D_3 and D_5 are turned-off. Therefore, inductors discharge the

stored energy to charge the capacitors.

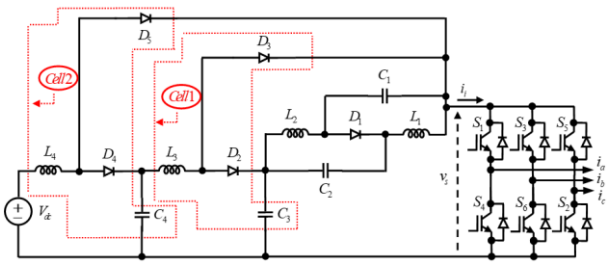


Fig. 2. Two-diode-cell QZSI with continuous current

C. Computation of Boost Factor and Capacitor Voltage Stress

By applying KVL for the ST power circuit, we have:

$$v_{L2}+V_{C1}=v_{L1}+V_{C2} \quad (1)$$

$$V_{C4}+v_{L3}=0 \quad (2)$$

$$v_{L4}-V_{dc}=0 \quad (3)$$

$$V_{C3}+V_{C1}+v_{L2}=0 \quad (4)$$

$$V_{C3}+V_{C2}+v_{L1}=0 \quad (5)$$

Applying KVL to the non-ST power circuit will produce the following equations:

$$V_{C2}=v_{L2} \quad (6)$$

$$V_{C1}=v_{L1} \quad (7)$$

$$v_{L4}-V_{dc}-V_{C4}=0 \quad (8)$$

$$v_{L3}-V_{C3}+V_{C4}=0 \quad (9)$$

where V_{C1} to V_{C4} are the capacitor voltage of C_1 to C_4, respectively, V_{L1} to V_{L4} are the inductor voltage of L_1 to L_4, respectively, and V_{dc} is the dc voltage source.

According to the above equations and based on the point that the average voltage of the inductor is equal to zero, the following expressions are developed:

$$V_{C1}=V_{C2}=\frac{-D_{sh}}{(1-2D_{sh})(1-D_{sh})^2}V_{dc} \quad (10)$$

$$V_{C3}=\frac{-1}{(1-D_{sh})^2}V_{dc} \quad (11)$$

$$V_{C4}=\frac{-1}{1-D_{sh}}V_{dc} \quad (12)$$

Boost factor of the proposed QZSI is computed as:

$$v_{s,\max}=-(V_{C1}+V_{C2}+V_{C3})=\frac{1}{(1-2D_{sh})(1-D_{sh})^2}V_{dc} \quad (13)$$

$$B=\frac{v_{s,\max}}{V_{dc}} \quad (14)$$

where the voltage across switch S is v_S. From the equations above, putting (10) to (12) into (14), the boost factor value is computed as:

$$B=\frac{1}{(1-2D_{sh})(1-D_{sh})^2} \quad (15)$$

By comparing (15) with the traditional ZSI boost factor value, which is equal to $B=1/(1-2D_{sh})$, it is evident that this new topology increases boost factor value. Additionally, by comparing this structure with the one-diode cell QZSI, which is equal to $B=1/(1-2D_{sh})(1-D_{sh})$, it is obvious that the boost factor is increased when one basic unit is added.

D. Computation of Diodes Voltage Stress

Implementing the KVL analysis of Fig. 2 and also factoring capacitors voltage stress value based on (10) to (12) will yield:

$$V_{D1}=V_{C1}+V_{C2}+V_{C3}=\frac{-1}{(1-2D_{sh})(1-D_{sh})^2}V_{dc} \quad (16)$$

$$V_{D2}=V_{C3}=\frac{-1}{(1-D_{sh})^2}V_{dc} \quad (17)$$

$$V_{D3}=V_{C1}+V_{C2}=\frac{-2D_{Sh}}{(1-2D_{Sh})(1-D_{Sh})^2}V_{dc} \quad (18)$$

$$V_{D4}=V_{C4}=\frac{-1}{1-D_{sh}}V_{dc} \quad (19)$$

$$V_{D5}=-V_{C4}+V_{C3}+V_{C1}+V_{C2}=\frac{2D_{sh}^2-3D_{sh}}{(1-2D_{sh})(1-D_{sh})^2}V_{dc} \quad (20)$$

E. Computation of Diodes, Inductors and DC-Link current values

By implementing the KCL analysis of Fig. 2 and given that the average capacitor current value for a period is zero, the following are derived:

$$i_i=(1-D_{sh})(1-2D_{sh})I_{dc} \quad (21)$$

$$I_{L1}=I_{L2}=(1-D_{sh})^2I_{dc} \quad (22)$$

$$I_{L3}=(1-D_{sh})I_{dc} \quad (23)$$

$$I_{L4}=I_{dc} \quad (24)$$

in which I_{dc} and I_{L1} to I_{L4} are the input dc current and current of inductors L_1 to L_4. In addition, i_i is the dc-link current.

By implementing the KCL analysis of Fig. 2 and putting (21) to (24), we derive:

$$I_{D1}=I_{L1}+I_{L2}-i_i=(1-D_{sh})I_{dc} \quad (25)$$

$$I_{D2}=I_{L3}=(1-D_{sh})I_{dc} \quad (26)$$

$$I_{D3}=I_{L3}=(1-D_{sh})I_{dc} \quad (27)$$

$$I_{D4}=I_{L4}=I_{dc} \quad (28)$$

$$I_{D5}=I_{L4}=I_{dc} \quad (29)$$

Contrasting the equations above, it is conspicuous that the added diode current values are equivalent. That is, diodes D_2 and D_3 of the first diode-cell have equivalent current values and the diodes of the second diode-cell D_4 and D_5 also have

equivalent current values. Additionally, by comparing to the traditional ZSI, increasing the quantity of the utilized proposed basic unit while decreasing the diode, inductor and dc-link current values are obtained.

F. Proposed CDAQZSI based on Three Diode-cells

Three diode-cells based on QZSI are proposed in this section. By adding two diodes, one inductor, and one capacitor to the two diode-cells, a three-diode-cell QZSI topology will be produced whose power circuit is illustrated by Fig. 3.

In the ST state, diodes D_3, D_5 and D_7 are turned on and diodes D_1, D_2, D_4 and D_6 are turned off. Therefore, the inductors and capacitors will be charged and discharged, respectively. During the non-ST state, diodes D_1, D_2, D_4 and D_6 are turned on and diodes D_3, D_5 and D_7 are turned off. Therefore, the inductors and capacitors will be discharged and charged, respectively. In this topology, equations of dc-link current, inductor current, capacitor voltage stress, diode voltage stress, and diode current are summarized in Table I.

By implementing the KVL analysis of Fig. 3 at the non-ST state, we derive:

$$v_{s,\max} = -(V_{C1} + V_{C2} + V_{C3}) \tag{30}$$

The boost factor is derived by substituting the capacitors voltage stress from Table I into (30) and changing this equation into (14):

$$B = \frac{v_{s,\max}}{V_{dc}} = \frac{1}{(1-2D_{sh})(1-D_{sh})^3} \tag{31}$$

By comparing (31) with the obtained boost factor in the conventional Z-source inverter that is equal to $B = 1/(1-2D_{sh})$, it results that this new topology increases the value of the boost factor. In addition, by contrasting the equation of the diode current in Table I, the results show that the diode currents of D_1, D_2, D_3 are equivalent. Similarly, the results show that the equation of diodes current of D_4 and D_5 are equivalent. Furthermore, the input dc current value and diodes D_6 and D_7 current values are equivalent. Additionally, the diode current values can be minimized by a factor of (1-D_{sh}) when D_{sh} value is increased. In addition, by increasing the value of D_{sh}, the diodes' current values are decreased by a factor of (1-D_{sh}). This is the same explanation about the inductors' current. When more basic units are used, their values are reduced by a factor of (1-D_{sh}).

G. Proposed Developed CDAQZSI

So, to derive the required boost factor, it is feasible to develop the proposed QZSI with the same number of active elements by adding n diode-cells in a back-to-back state at the end of the inverter. This characteristic, when compared to the traditional ZSI, is the major advantage of the proposed inverter. Fig. 4 shows the power circuit of the proposed inverter. Individual cells of the proposed inverter are composed of two diodes, one inductor, and one capacitor, respectively. The numbers of the power electronic elements in the proposed CDAQZSI are derived from

$$N_L = n + 2 \tag{32}$$

$$N_C = n + 2 \tag{33}$$

$$N_D = 2n + 1 \tag{34}$$

in which n is the number of the diode-cells used.

H. Computation of Boost Factor and Capacitor Voltage Stress

By contrasting the capacitor voltage stress of two and three diode-cells of C_1 and C_2 by (10) and Table 1 equations, it is evident that the capacitor voltage stress is affected by a factor of $1/1-D_{sh}$ when the number of the basic units is increased. The same explanation about the capacitor voltage stress is valid. Furthermore, the voltage stress of the individual diode-cells is affected by the same factor of $1/1-D_{sh}$ when the number of the basic units is increased, i.e. the new capacitor in the existing topology and the capacitor in this new topology are affected by the same factor. For example, the voltage stress of C_3 in the two-diode-cell QZSI is equivalent to the voltage stress of C_4 in the three-diode-cell QZSI.

Moreover, as it is clear from the diode basic unit's topology, by utilizing individual diode-cell, two diodes are included in the proposed ZSI. Additionally, by contrasting (16) and (17) with the same equations in Table I, it is apparent that the voltage stress of the diodes is affected by a factor of $1/1-D_{sh}$ when the number of diode-cells utilized is increased.

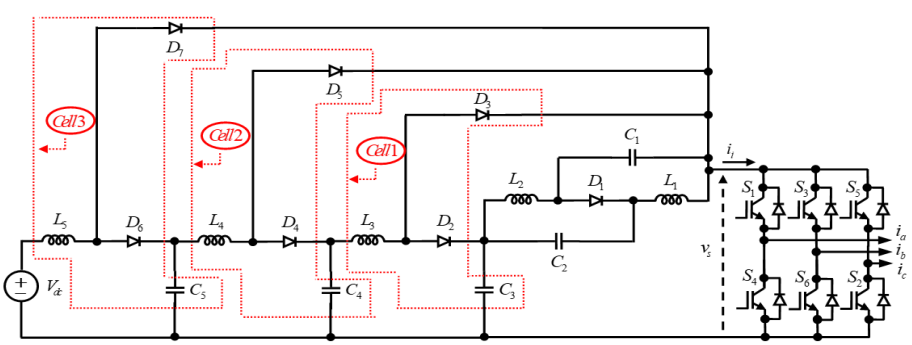


Fig. 3. A three-diode-cell QZSI with the continuous current.

TABLE I

VOLTAGE AND CURRENT EQUATIONS OF ALL ELEMENTS IN THE THREE-CELL CDAQZSI

Capacitors' Voltage Equations	Inductors' Current Equations	Diodes' Voltage Equations	Diodes' Current Equations
$V_{C1}=V_{C2}=\frac{-D_{sh}}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$	$I_{L1}=I_{L2}=(1-D_{sh})^3 I_{dc}$	$V_{D1}=\frac{-1}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$	$i_i=(1-D_{sh})^2(1-2D_{sh})I_{dc}$
$V_{C3}=\frac{-1}{(1-D_{sh})^3}V_{dc}$	$I_{L3}=(1-D_{sh})^2 I_{dc}$	$V_{D2}=\frac{-1}{(1-D_{sh})^3}V_{dc}$	$I_{D1}=I_{D2}=I_{D3}=(1-D_{sh})^2 I_{dc}$
$V_{C4}=\frac{-1}{(1-D_{sh})^2}V_{dc}$	$I_{L4}=(1-D_{sh})I_{dc}$	$V_{D3}=\frac{-2D_{Sh}}{(1-2D_{Sh})(1-D_{Sh})^3}V_{dc}$	$I_{D4}=I_{D5}=(1-D_{sh})I_{dc}$
$V_{C5}=\frac{-1}{1-D_{sh}}V_{dc}$	$I_{L5}=I_{dc}$	$V_{D4}=\frac{-1}{(1-D_{sh})^2}V_{dc}$	$I_{D6}=I_{D7}=I_{dc}$
-	-	$V_{D5}=\frac{2D_{sh}^2-3D_{sh}}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$ $V_{D6}=\frac{-1}{1-D_{sh}}V_{dc}$ $V_{D7}=\frac{-2D_{sh}^3+5D_{sh}^2-4D_{sh}}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$	-

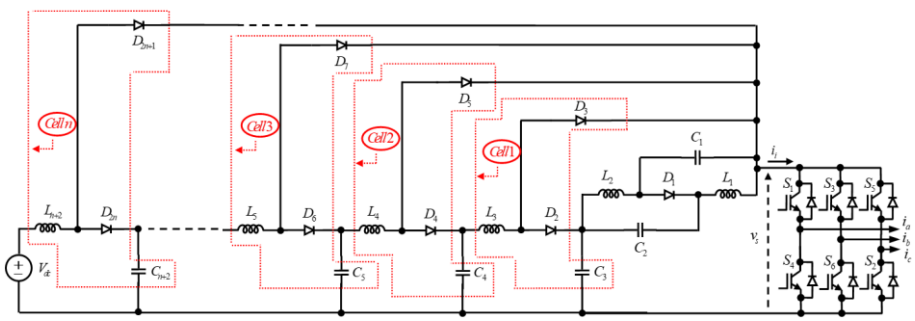


Fig. 4. The proposed developed QZSI topology with the continuous current

This characteristic is applied for series connection of inductor and diodes in individual cells. In addition, by comparing (16), (17), and (19) with the same equation in Table I, it is apparent that in the same diode-cell, the voltage stress of capacitors and series-connected diodes are equivalent. This means that in the same diode-cell, the voltage stress of capacitor C_3 is equivalent to the voltage stress of diode D_2. Moreover, contrasting equations of the inductor current of two-diode-cell-based QZSI (22) to (24) with the same equations in the three-diode-cell QZSI in Table I, it is apparent that the inductor current value is reduced by a factor of (1-D_{sh}) when the number of the diode-cells used is increased. Furthermore, the dc source current value is equivalent to the inductor current value because they are series-connected. In addition, by considering the diodes' current equations from (25) to (29) and the same equations in Table I, it is observed that the diode current value is reduced by a factor of (1-D_{sh}) when more diode-cells are applied. Additionally, the current values of the inductors and diodes in the same cell are equivalent. For example, the current values of inductors L_4 and diodes D_4 and D_5 are equivalent (I_{D4}=I_{D5}=I_{L4}). Therefore, it is feasible to derive current and voltage equations for n-cell CDAQZSI with various utilized elements as indicated in Table II.

The peak input voltage for this topology is expressed by:

$$v_{s,\max}=-(V_{C1}+V_{C2}+V_{C3}) \tag{35}$$

In addition, by substituting the value of voltage capacitors from Table II into (14), the boost factor value is derived by:

$$B=\frac{1}{(1-2D_{Sh})(1-D_{Sh})^n} \tag{36}$$

As it is clear from (36), the value of the boost factor is increased with a factor of $1/1-D_{sh}$ by adding the number of utilized new diode-assisted basic units. This result is also derived without using extra active elements. In addition, the current values of dc-link, diodes, and inductors are also decreased by increasing the number of the basic units.

TABLE II

VOLTAGE AND CURRENT EQUATIONS OF ALL ELEMENTS IN n-CELL CDAQZSI

Capacitors' Voltage Equations	Inductors' Current Equations	Diodes' Voltage Equations	Diodes' Current Equations
$V_{C1}=V_{C2}=\frac{-D_{sh}}{(1-2D_{sh})(1-D_{sh})^{n}}V_{dc}$	$I_{L1}=I_{L2}=\frac{(1-D_{sh})}{(1-2D_{sh})}\mathrm{i}_{i}=(1-D_{sh})^{n}I_{dc}$	$V_{D1}=\frac{-1}{(1-2D_{sh})(1-D_{sh})^{n}}V_{dc}$	$\mathrm{i}_{i}=(1-2D_{sh})(1-D_{sh})^{n-1}I_{dc}$
$V_{C3}=\frac{-1}{(1-D_{sh})^{n}}V_{dc}$	$I_{L\,j+1}=\frac{1}{(1-D_{sh})}I_{L\,j}$ for $j=2,3,4,\cdots,n$	$V_{D2}=\frac{-1}{(1-D_{sh})^{n}}V_{dc}$	$I_{D1}=I_{D2}=I_{D3}=(1-D_{sh})^{n-1}I_{dc}$
$V_{C\,j+2}=(1-D_{sh})^{j-1}V_{C3}$ for $j=1,2,3,\cdots,n$	$I_{L\,n+2}=I_{dc}$	$V_{D3}=\frac{-2D_{sh}}{(1-2D_{sh})(1-D_{sh})^{n}}V_{dc}$	$I_{D\,2j}=I_{D\,2j+1}=\frac{1}{1-D_{sh}}I_{D\,2j-1}$ for $j=2,3,4,\cdots,n$
-	-	$V_{D\,2j+1}=\frac{1}{(1-D_{sh})}-\frac{1}{(1-2D_{sh})(1-D_{sh})^{j}}V_{dc}$ $j=2,3,\cdots,n$ $V_{D2j}=(1-D_{sh})^{j-1}V_{D2}$ for $j=1,2,3,\cdots,n$	-

I. Proposed DDAQZSI

In this sub-section, another new topology is proposed for QZSI based on the diode-assisted basic unit and in the discontinuous current state. This new topology is analyzed based on using two basic units, three basic units, and finally its developed topology. In addition, the related equations for all states of all used elements are calculated, and then the general equation for the boost factor, voltage, and current of the used power electronic devices are proposed.

J. Proposed DDAQZSI Based on Two Diode-cells

The power circuit of the proposed two-cell DDAQZSI is shown in Fig. 5. As illustrated by this figure, one basic unit is composed of two diodes, one inductor, and one diode, which are added to the one-cell DAQZSI. The operating modes of this inverter are segmented into ST and non-ST states. During the ST state, diodes D_1, D_2, D_4 are turned off whiles switch S and diodes D_3 and D_5 are turned on. Therefore, the capacitors and inductors will be discharged and charged accordingly. During the non-ST state, diodes D_1, D_2, D_4 are turned on while switch S and diodes D_3 and D_5 are turned off. Therefore, the capacitors and inductors will be charged and discharged accordingly.

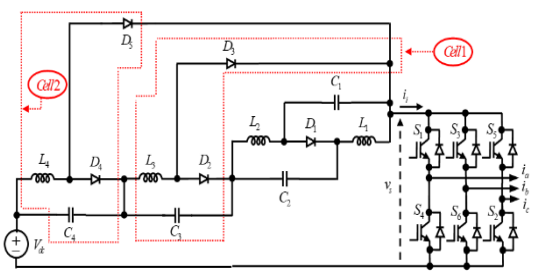


Fig. 5. The two-cell DAQZSI with the discontinuous current.

K. Computation of Boost Factor and Capacitor Voltage Stress

By applying KVL in Fig. 5, we have:

$$v_{L4}-V_{dc}=0 \tag{37}$$

$$v_{L2}+V_{C1}=v_{L1}+V_{C2} \tag{38}$$

$$-V_{dc}+V_{C4}+v_{L3}=0 \tag{39}$$

$$-V_{dc}+V_{C3}+V_{C4}+V_{C1}+v_{L2}=0 \tag{40}$$

$$-V_{dc}+V_{C3}+V_{C4}+V_{C2}+v_{L1}=0 \tag{41}$$

$$V_{C4}=v_{L4} \tag{42}$$

$$v_{L3}=V_{C3} \tag{43}$$

$$V_{C2}=v_{L2} \tag{44}$$

$$V_{C1}=v_{L1} \tag{45}$$

$$v_{L1}=v_{L2} \tag{46}$$

$$V_{C1}=V_{C2} \tag{47}$$

Given that the inductor average voltage is zero, the following results are derived:

$$V_{C1}=V_{C2}=\frac{-D_{sh}}{(1-2D_{sh})(1-D_{sh})^{2}}V_{dc} \tag{48}$$

$$V_{C3}=\frac{-D_{sh}}{(1-D_{sh})^{2}}V_{dc} \tag{49}$$

$$V_{C4}=\frac{-D_{sh}}{1-D_{sh}}V_{dc} \tag{50}$$

In addition, implementing the KVL analysis of Fig. 5 will yield the following:

$$v_{s,\max}=V_{dc}-(V_{C4}+V_{C3}+V_{C2}+V_{C1}) \tag{51}$$

Substituting the values of V_{C1} to V_{C4} from (48) to (50) into

(51), the peak inverter input dc voltage is equivalent to:

$$v_{s,\max} = \frac{1}{(1-2D_{sh})(1-D_{sh})^2} V_{dc} \quad (52)$$

In DDAQZSI, the boost factor is computed by:

$$B = \frac{v_{s,\max}}{V_{dc}} = \frac{1}{(1-2D_{sh})(1-D_{sh})^2} \quad (53)$$

By comparing (53) with the obtained boost factor in the conventional Z-source inverter, which is equal to $B = 1/(1-2D_{sh})$, it results that this new topology increases the value of the boost factor.

L. Computation of Diodes Voltage Stress

Implementing the KVL analysis of Fig. 5 and substituting the voltage values of capacitors C_1 to C_4 from (48) to (50) into the equations of diodes voltage is derived by:

$$V_{D1} = \frac{-1}{(1-2D_{sh})(1-D_{sh})^2} V_{dc} \quad (54)$$

$$V_{D2} = -V_{dc} + V_{C3} + V_{C4} = \frac{-1}{(1-D_{sh})^2} V_{dc} \quad (55)$$

$$V_{D3} = V_{C1} + V_{C2} = \frac{-2D_{Sh}}{(1-2D_{Sh})(1-D_{Sh})^2} V_{dc} \quad (56)$$

$$V_{D4} = V_{C4} - V_{dc} = \frac{-1}{1-D_{sh}} V_{dc} \quad (57)$$

$$V_{D5} = V_{C3} + V_{C1} + V_{C2} = \frac{2D_{sh}^2 - 3D_{sh}}{(1-2D_{sh})(1-D_{sh})^2} V_{dc} \quad (58)$$

M. Computation of Diodes, Inductors, and DC-Link Current Values

By implementing the KCL analysis of Fig. 5 and given that the average capacitor current value for a period is zero, the following are derived:

$$i_i = I_{dc} \quad (59)$$

$$I_{L1} = I_{L2} = \frac{(1-D_{sh})}{(1-2D_{sh})} I_{dc} \quad (60)$$

$$I_{L3} = \frac{1}{1-2D_{sh}} I_{dc} \quad (61)$$

$$I_{L4} = \frac{1}{(1-D_{sh})(1-2D_{sh})} I_{dc} \quad (62)$$

By implementing the KCL analysis of Fig. 5 and putting (59) to (62), we derive

$$I_{D1} = I_{L1} + I_{L2} - i_i = \frac{1}{1-2D_{sh}} I_{dc} \quad (63)$$

$$I_{D2} = I_{D3} = I_{L3} = \frac{1}{1-2D_{sh}} I_{dc} \quad (64)$$

$$I_{D4} = I_{D5} = I_{L4} = \frac{1}{(1-D_{sh})(1-2D_{sh})} I_{dc} \quad (65)$$

N. Proposed Three-cell DDAQZSI

The analysis of the proposed three-cell DDAQZSI is investigated in this section. It is derived by adding two diodes, one inductor, and one capacitor to the two-cell DDAQZSI. Fig. 6 illustrates the three-cell DDAQZSI power circuit. Two states of operation are possible in the proposed topology, shoot-though and non-shoot-through states. Diodes D_3, D_5, and D_7 conducts whiles diodes D_1, D_2, D_4, and D_6 are turned off during the ST state. Therefore, the capacitors and inductors will be discharged and charged accordingly. During the non-ST state, diodes D_1, D_2, D_4, and D_6 are turned on whiles diodes D_3 and D_5 are turned off. Therefore, the capacitors and inductors will be charged and discharged accordingly. Table III shows the equations obtained for all elements in the topology.

The implementation of the KVL analysis of Fig. 6 will yield the following results:

$$v_{s,\max} = V_{dc} - (V_{C5} + V_{C4} + V_{C3} + V_{C2} + V_{C1}) \quad (66)$$

By substituting capacitors voltage stress from Table III into (66) and putting this equation into (53), the boost factor value is derived from:

$$B = \frac{v_{s,\max}}{V_{dc}} = \frac{1}{(1-2D_{sh})(1-D_{sh})^3} \quad (67)$$

By considering (53) and (67), it is evident that the boost factor value is increased by a factor of $1/1-D_{sh}$ when one basic unit is added. Contrasting equations of diodes' current from Table III, it is evident that diodes D_1, D_2, and D_3 have equivalent current values. Likewise, diodes D_4 and D_5 have equivalent current equations. This analysis is valid for diodes D_6 and D_7. Simply put, the diode current equations for individual cells are equivalent when each cell is added.

O. Proposed Developed DDAQZSI

So, to derive the required boost factor, it is feasible to develop the proposed DDAQZSI with the same number of active elements by increasing the number of the basic unit used in a back-to-back state at the end of the inverter. This characteristic, when compared to the traditional ZSI, is the major advantage of the proposed inverter. Fig. 7 shows the power circuit of the proposed inverter. Individual cells of the proposed inverter are composed of two diodes, one inductor, and one capacitor. The number of the power electronic elements used in the proposed DDAQZSI is derived by:

$$N_L = n + 2 \quad (68)$$

$$N_C = n + 2 \quad (69)$$

$$N_D = 2n + 1 \quad (70)$$

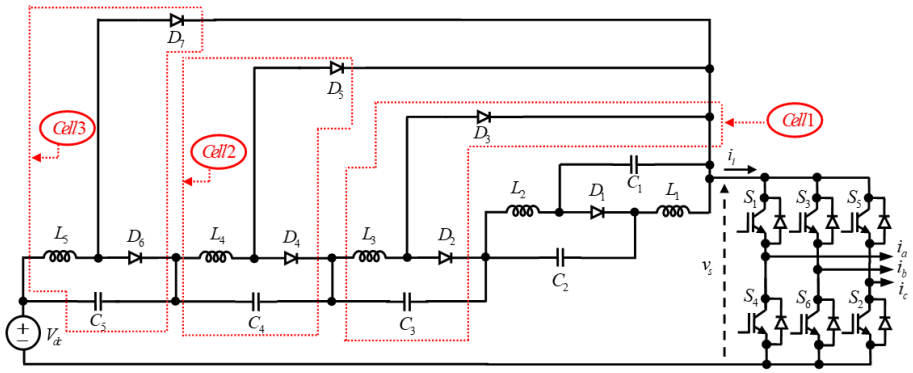


Fig. 6. The three-cell DDAQZSI power circuit with discontinuous current

TABLE III

VOLTAGE AND CURRENT EQUATIONS OF THREE-CELL DDAQZSI

Capacitors' Voltage Equations	Inductors' Current Equations	Diodes' Voltage Equations	Diodes' Current Equations
$V_{C1}=V_{C2}=\frac{-D_{sh}}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$	$I_{L1}=I_{L2}=\frac{1-D_{sh}}{1-2D_{sh}}I_{dc}$	$V_{D1}=\frac{-1}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$	$i_i=I_{dc}$
$V_{C3}=\frac{-D_{sh}}{(1-D_{sh})^3}V_{dc}$	$I_{L3}=\frac{1}{1-2D_{sh}}I_{dc}$	$V_{D2}=\frac{-1}{(1-D_{sh})^3}V_{dc}$	$I_{D1}=I_{D2}=I_{D3}=\frac{1}{1-2D_{sh}}I_{dc}$
$V_{C4}=\frac{-D_{sh}}{(1-D_{sh})^2}V_{dc}$	$I_{L4}=\frac{1}{(1-D_{sh})(1-2D_{sh})}I_{dc}$	$V_{D3}=\frac{-2D_{Sh}}{(1-2D_{Sh})(1-D_{Sh})^3}V_{dc}$	$I_{D4}=I_{D5}=\frac{1}{(1-D_{sh})(1-2D_{sh})}I_{dc}$
$V_{C5}=\frac{-D_{sh}}{1-D_{sh}}V_{dc}$	$I_{L5}=\frac{1}{(1-D_{sh})^2(1-2D_{sh})}I_{dc}$	$V_{D4}=\frac{-1}{(1-D_{sh})^2}V_{dc}$	$I_{D6}=I_{D7}=\frac{1}{(1-D_{sh})^2(1-2D_{sh})}I_{dc}$
-	-	$V_{D5}=\frac{2D_{sh}^2-3D_{sh}}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$ $V_{D6}=\frac{-1}{1-D_{sh}}V_{dc}$ $V_{D7}=\frac{-2D_{sh}^3+5D_{sh}^2-4D_{sh}}{(1-2D_{sh})(1-D_{sh})^3}V_{dc}$	-

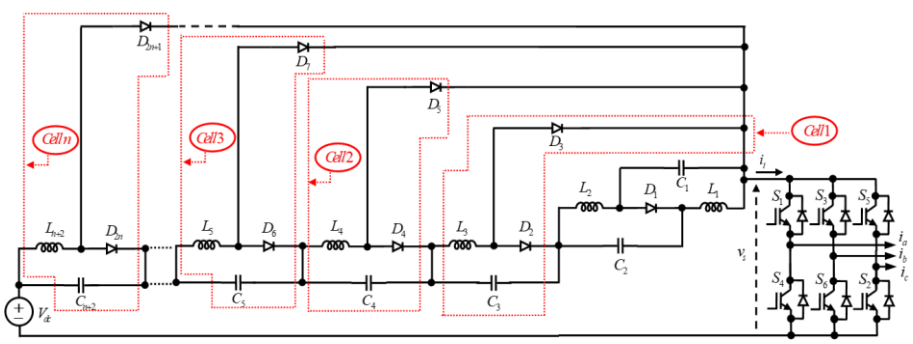


Fig. 7. The developed QZSI power circuit with discontinuous current

P. Computation of Boost Factor and Capacitor Voltage Stress

By contrasting the capacitor voltage stress values from (48) to (50) in the two-cell DDAQZSI with equivalent equations in Table III of the three-cell DDAQZSI, it is drawn that the factor of $1/1-D_{sh}$ affects the capacitor voltage stress equation when the number of the cells used is increased by one. Moreover, the voltage stresses of the capacitors in the previous and new structures are equivalent. That is to say that the voltage stress of capacitor C_3 in the two-cell DDAQZSI is

equivalent to the voltage stress of capacitor C_4 in the three-cell DDAQZSI.

As previously stated, adding two diodes to the basic structure increases the number of the cells used. These diodes are connected in parallel and series. In the main section of the circuit, inductors and one diode are connected in series whiles the remaining diode is parallel-connected. Furthermore, evaluating the diode voltage stress equations of Table III with (54) to (58), it is clear that the series-connected diodes are affected by a factor of $1/1-D_{sh}$.

Moreover, there are the same explanations for the inductors' current. In other words, by contrasting two-diode-cell-based QZSI inductors' current equations from (59) to (62) to three-diode-cell-based QZSI inductors' current equations from Table III, it results that the inductors' current values are affected by a factor of $1/1-D_{sh}$ when the number of the cells used are increased. Additionally, by evaluating diodes' current equations from (63) to (65) and the equivalent equations in Table III, it is drawn that the current equations of diodes D_1, D_2 and D_3 are equivalent and constant when the number of the diode-cells used are increased. Moreover, the current equations of other diodes are affected by a factor of $1/1-D_{sh}$ in comparison to the diode current equation. Finally, Table IV shows the n-cell summarized element equations for current and voltage in DDAQZSI.

Based on Table IV, the current values of diodes in individual cells are the same while the peak dc input voltage is equivalent to:

$$v_{s,\max}=V_{dc}-\sum_{i=1}^{n+2}V_{Ci}=\frac{1}{(1-2D_{Sh})(1-D_{Sh})^{n}}V_{dc}=BV_{dc} \qquad (71)$$

Obviously, it is drawn from (71) that the boost factor value of DDAQZSI is increased by a factor of $1/1-D_{sh}$ when the number of the used cells is also increased. It is obvious that the required value of the boost factor is achievable for this topology by using the equivalent D_{sh} value when juxtaposed to traditional ZSI. This characteristic is the major merit of the proposed developed DDAQZSI.

III. Comparison of the Proposed Topology with the Conventional ZSIs

In this section, to investigate the advantages and disadvantages of the proposed topologies (DDAQZSI and CDAQZSI), these topologies will be compared with several ZSIs. In this comparison, the values of the boost factor based on the number of the elements used are considered. Table I shows this comparison by considering the same value of the ST state duty cycle.

In this table, D shows the value of the ST state duty cycle and n is the number of the units used. As it is clear from the above table, the proposed topologies can obtain a higher value of the boost factor in comparison to other topologies by the same value of D. In addition, it is possible to develop the proposed topologies by increasing only the passive elements that lead to decreasing the losses of the converters in comparison to others. In other words, the value of the boost factor is however increased and the number of the used elements are increased but because of using passive elements, the power losses will not increase while to receive the same value of the boost factor by using other topologies, the power losses will be increased.

IV. Experimental Results

In this section, the correct performance of the proposed CDAQZSI is reconfirmed. To obtain these results, the experimental prototype of the proposed topology with two basic units shown in Fig. 2 is considered. Table V indicates the parameter values utilized for laboratory investigation. Additionally, a simple boost control technique is used and all components are assumed to be ideal.

TABLE VI
EXPERIMENTAL PARAMETERS

$100\,V$	*Input voltage* (V_i)
$5kHz$	*Switching frequency*
150Ω	R_L
6.3 mH	L_f
6 mH	$L_1=L_2=L_3=L_4$
680 μF	$C_1=C_2=C_3=C_4$
0.15	D_{ST}
50 Hz	f_o

Fig. 8 illustrates the experimental waveform of the proposed inverter's input source voltage of which the peak value is 200 V , which is equivalent to 197.6 V derived by computing Eq. (13). The experimental boost factor value is approximately 2, which is equivalent to 1.976 derived by computing Eq. (15). The proposed diode-cells are utilized in the proposed topology to obtain this increase.

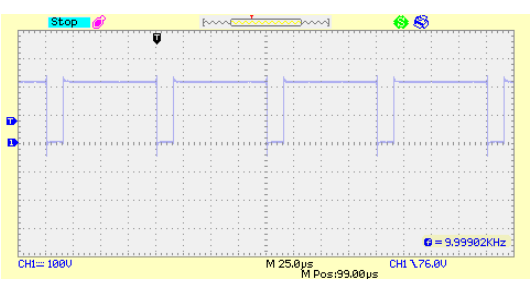


Fig. 8. The input voltage waveform of CDAQZSI

TABLE IV

VOLTAGE AND CURRENT EQUATIONS OF ALL ELEMENTS USED IN n-CELL DDAQZSI

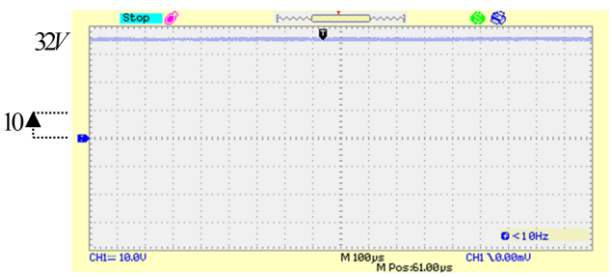
Capacitors' Voltage Equations	Inductors' Current Equations	Diodes' Voltage Equations	Diodes' Current Equations
$V_{C1}=V_{C2}=\frac{-D_{sh}}{(1-2D_{sh})(1-D_{sh})^{n}}V_{dc}$	$I_{L1}=I_{L2}=\frac{1-D_{sh}}{1-2D_{sh}}I_{dc}$	$V_{D1}=\frac{-1}{(1-2D_{sh})(1-D_{sh})^{n}}V_{dc}$	$i_i=I_{dc}$
$V_{C3}=\frac{-D_{sh}}{(1-D_{sh})^{n}}V_{dc}$	$I_{L\,j+2}=\frac{1}{(1-D_{sh})}I_{L\,j+1}$ for $j=1,2,3,4,\cdots,n$	$V_{D2}=\frac{-1}{(1-D_{sh})^{n}}V_{dc}$	$I_{D1}=I_{D2}=I_{D3}=\frac{1}{1-2D_{sh}}I_{dc}$
$V_{C\,j+2}=(1-D_{sh})^{j-1}V_{C3}$ for $j=1,2,3,\cdots,n$	-	$V_{D\,2\,j+1}=\frac{-2D_{sh}}{(1-2D_{sh})(1-D_{sh})^{j}}V_{dc}+\sum_{j=2}^{n}\frac{-D_{sh}}{(1-D_{sh})^{j}}$ for $j=1,2,3,\cdots,n$	$I_{D\,2\,j}=I_{D\,2\,j+1}=\frac{1}{(1-D_{sh})^{j-1}(1-2D_{sh})}I_{dc}$ for $j=2,3,4,\cdots,n$
-		$V_{D\,2\,j}=(1-D_{sh})^{j-1}V_{D2}$ for $j=1,2,3,\cdots,n$	-

TABLE V

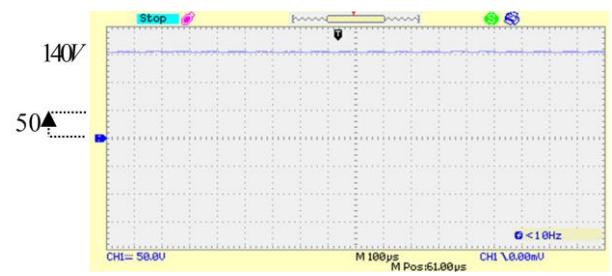
COMPARISON OF NUMBER OF ELEMENTS AND BOOST FACTOR FOR PROPOSED TOPOLOGY WITH CONVENTIONAL ZSIs

No.	Topologies	Value of Boost Factor	No. of Diode	No. of Capacitors	No. of Inductors
1	Proposed (DDAQZSI and CDAQZSI)	$1/(1-2D)(1-D)^{m}$ for $m=1,2,3,\cdots,n$	$N_D=2n+1$	$N_C=n+2$	$N_L=n+2$
2	[25]	$1/(1-2D)$	1	3	2
3	[26]	$(1+D)/(1-3D)$	1	2	4
3	[14]	$(1+D)/(1-D)$	3	0	2
5	[18]	$1/(1-2D)(1-D)$	2	3	3

The experimental capacitors' voltage waveforms are illustrated in Fig. 9. Capacitors C_1 and C_2 have equivalent voltage values, which is $32\,V$ as is depicted in Fig. 9(a). Approximately, this value is equivalent to $29.66\,V$, which is derived by computing Eq. (10). Fig. 9(b) illustrates the waveform of capacitor C_3 's voltage value. The voltage magnitude from this waveform is $140\,V$, which is almost approximately equivalent to $138.4\,V$ obtained from computing Eq. (11). Fig. 10 illustrate the voltage waveform values of diodes D_1 to D_5. The voltage magnitudes of these diodes D_1 to D_5 are equivalent to $200\,V$, $140\,V$, $60\,V$, $120\,V$, and $82\,V$, respectively. These values are almost equivalent to $197.7\,V$, $138.4\,V$, $59.3\,V$, $117.6\,V$, and $80.07\,V$, respectively, derived by computing Eq. (16) to (20).

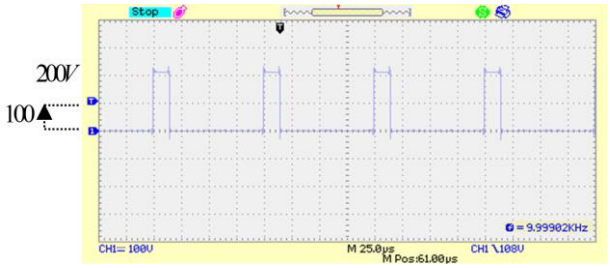


(a)

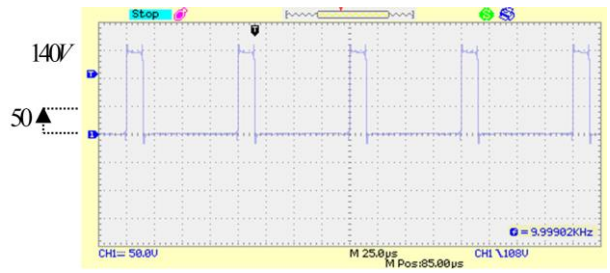


(b)

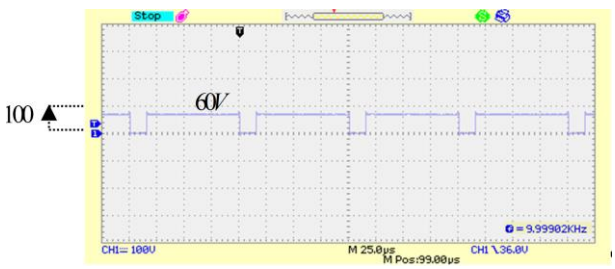
Fig. 9. Capacitors' voltage waveforms; (a) $V_{C1}=V_{C2}$; (b) V_{C3}



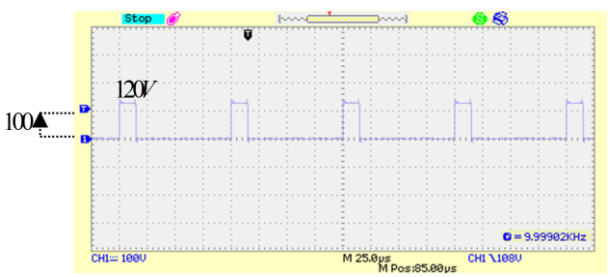
(a)



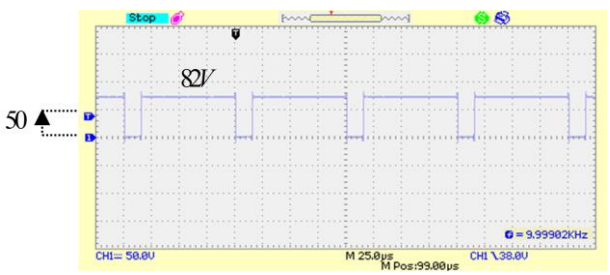
(b)



(c)



(d)



(e)

Fig. 10. Diodes' voltage waveforms; (a) V_{D1} ; (b) V_{D2} ; (c) V_{D3} ; (d) V_{D4} ; (e) V_{D5}

V. Conclusion

Two newly developed QZSIs created on two novel diode-cells are proposed. These topologies, which are called DDAQZSI and CDAQZSI, are capable of increasing the boost factor to the required magnitude without increasing the number of the active elements used. The proposed QZSIs are examined in three conditions: a two-diode-cell QZSI, a three-diode-cell QZSI, and lastly, an -diode-cell developed QZSI. The main difference between these topologies is related to the input dc current, which is continuous in CDAQZSI and is discontinuous in DDAQZSI. These inverters are thoroughly scrutinized in the ST and non-ST states. The current and voltage equations of the used elements, namely capacitors, diodes, and inductors, are computed. According to the acquired equations, the boost factor values are increased by a factor of $1/1-D_{sh}$ when the number of the diode-cells used is increased in the two proposed QZSIs. In addition, in the CDAQZSI, dc-link, diodes, and inductors' current values are reduced by a factor of $1-D_{sh}$ when the same ST duty cycle value (D_{sh}) with more diode-cells are utilized. Moreover, in the DDAQZSI, by increasing the number of basic units, the value of inductors' current will be constant. Lastly, the accuracy operation of the CDAQZSI is reconfirmed through experimental results in the laboratory on two diode-cells.

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