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Optimization of a New Extended Cascaded Multilevel Inverter Topology to Reduce DC Voltage Sources and Power Electronic Components

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ABSTRACT

This work proposes a new multilevel inverter consisting of basic and sub-multilevel units. The basic unit is made up of four isolated dc voltage sources, two bidirectional switches, and ten unidirectional switches. To increase the number of output voltage levels, a cascaded architecture based on a series connection of sub-multilevel is proposed. The proposed inverter utilizes two algorithms to determine the values of dc voltage sources. The number of IGBTs, dc voltage sources, gate driver circuits, variety of dc voltage sources, and peak standing voltage on the switches are calculated and their optimization to produce the maximum number of levels in output voltage is investigated. To examine the advantages of the proposed inverter, the topology is compared with other topologies. The results show the superiority of the proposed topology over most conventional topologies in terms of the number of circuit components. Finally, to confirm the performance of the proposed multilevel inverter, the experimental results of a 25-level inverter prototype are provided.

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I. INTRODUCTION

Multilevel inverters (MLI) have been used as one of the premier alternatives for medium to high power conversion utilizations, such as FACTS devices, renewable energy conversion systems, UPSs (uninterruptible power supply), electric vehicles, and HVDC [1-3]. One of famous topologies is Cascaded H-bridge (CHB) inverters. However, cascaded inverters require a greater quantity of input dc voltage sources and switches, and attempts to minimize the quantity of multi-level inverter circuit components have been one of the main goals of researchers. Based on these constraints, several topologies have been proposed to decrease the quantity of switches in [4-7] and H bridges are used to generate both positive and negative output voltage levels in all these topologies. However, H-bridge switches have a higher standing voltage, which limits their utilization in high-voltage systems. The topologies presented in [6, 7] are composed of diodes and have higher power losses in their asymmetric topologies. These limitations were resolved in [4, 8-9] where the structures can generate both polarities of output voltage levels without using H-bridge. However, they require more isolated dc voltage sources, which is another problem. A new MLI topology presented in [10,11] is a modified H-bridge multilevel inverter that can generate both polarities of output voltage levels using fewer switches. The topologies presented in [12-13] utilize bidirectional

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switches in which the number of gate driver circuits decreases due to the presence of one driver on each bidirectional switch. However, these topologies have a higher standing voltage than the CHB. New MLI topologies disadvantage of this converter is that it has a higher total standing voltage and the quantity of dc voltage sources in [15] is high. The use of a lower number of dc voltage sources in the switched cascaded MLI structure presented in [16] is one of the advantages of this topology. However, requiring a large number of ON switches is an unsolved problem and reduces the efficiency of the inverter. A new MLI topology with asymmetrical configuration was reported in [17], which can produce higher output voltage levels but still suffers from a large number of drivers and isolated sources of dc voltage sources. The MLI topologies introduced in [17, 18] generate both polarities of voltage levels without using an H-bridge. The nature of the bidirectional and unidirectional switches used in these architectures are common emitters where each unidirectional switch comprises of an antiparallel diode and an IGBT, while a bidirectional switch has two IGBTs and antiparallel diodes accordingly both of which require a single gate driver circuit. The basic structure of E-Type MLI in [17] generates 13 levels of output voltage using four asymmetric dc voltage sources and 10 gate driver circuits, but the ST-type topology in [18] requires the same number of dc voltage sources (four asymmetric dc voltage sources) and 12 gate driver circuits to produce 17 levels at the output. A new multilevel inverter topology comprising basic and sub-multilevel units is proposed in this work. This topology is also optimized for different purposes and is then compared with several multilevel inverters to evaluate the benefits of the advantages and disadvantages. Finally, the performance of the proposed 25-level inverter is evaluated by performing different test scenarios on the designed inverter prototype.

II. PROPOSED BASIC UNIT

The basic unit of the proposed multilevel inverter is shown in Fig. 1. The architecture of the proposed topology is a combination of ten unidirectional switches (individual switches are made up of an antiparallel diode and an IGBT), two bidirectional switches with a common-emitter topology (made of two IGBTs and two antiparallel diodes), and four isolated dc voltage sources with magnitudes of (U_1) and (U_2). The switching modes of the proposed 25-level MLI are presented in Table I in which '1' and '0' stand for ON and OFF states of the switches, respectively. The circuit layout of the proposed topology and the selection of the switching paths should be such that the dc voltage sources are never short-circuited by IGBTs or diodes. Clearly, the switches (Z_1, Z_2), $(Z_1, S_Y, S_X), \cdots$ are reported in [14, 15] have reduced the number of switches and used unidirectional switches. The amplitudes of dc voltage sources in these topologies are equal in which case it is named symmetric configuration. However, the main controlled in a complementary way to have a safe performance and to avoid short circuits across the voltage sources. The proposed MLI configurations shown in Fig. 1 can generate the following levels of voltage at the output:

$$0, \pm U_1, \pm 2U_1, \pm(U_2 - 2U_1), \pm(U_2 - U_1), \pm U_2,$$
$$\pm(U_1 + U_2), \pm(2U_1 + U_2), \pm(2U_2 - 2U_1), \pm(2U_2 - U_1),$$
$$2U_2, \pm(U_1 + 2U_2), \pm(2U_1 + 2U_2).$$

Due to the importance and impact of dc voltage source values on the quantity of output voltage levels, the amplitude of the dc voltage sources is chosen to produce maximize the number of output voltage levels as follows:

$$U_1 = U_{dc}, \; U_2 = 2U_{dc}$$

As mentioned before, this topology is capable of generating 25 levels of output voltage: zero output voltage level and 12 output levels for each polarity of voltage without using any voltage polarity generator such as H-bridges. Another issue regarding the proposed basic structure is the design and selection of switches. For this purpose, it is necessary to specify the nominal values of voltage and current of all switches. Table II summarizes the nominal values of voltage and current of all switches. Due to the fact that the switches that are on always have a series connection with the output load, the rated current of all switches will be equal to the maximum load current (I_m).

III. PROPOSED CASCADE MULTILEVEL INVERTER

The extended topology, which is referred to as sub-multilevel, is capable of producing higher levels of output voltage as shown in Fig. 2. The proposed sub-multilevel is made up of n dc voltage sources with magnitude (U_1) and n equal dc voltage sources with magnitude (U_2).

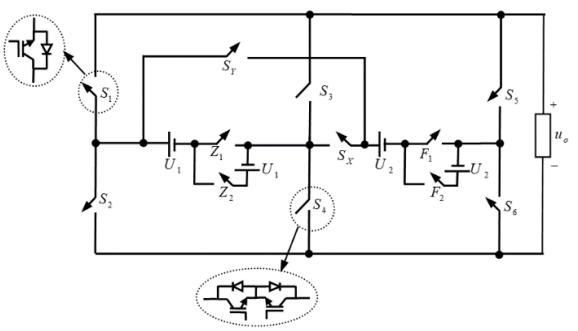


Fig. 1. The proposed basic unit topology.

Table III indicates the switching modes of the proposed sub-multilevel. Deriving expression for the quantity of

power electronic components used in the sub-multilevel topology is the focus of this section. The quantity of dc voltage sources (N_{source}^{sub}), the quantity of IGBTs (N_{IGBT}^{sub}), the quantity of gate driver (N_{drive}^{sub}), and the quantity of a variety of dc voltage sources ($N_{variety}^{sub}$) in the sub-multilevel topology can be calculated using the following equations:

$$N_{source}^{sub} = 2n \quad (1)$$

$$N_{drive}^{sub} = 2n + 8 \quad (2)$$

$$N_{IGBT}^{sub} = 4n + 6 \quad (3)$$

$$N_{variety}^{sub} = 2 \quad (4)$$

The total number of dc voltage sources used in the topology as shown in Fig. 2 is equal to 2n. As per Table III, the maximum output voltage of the proposed sub-multilevel ($U_{o,\max}^{sub}$) and the number of output voltage levels can be derived from the following equations:

$$U_{o,\max}^{sub} = n(U_1 + U_2) \quad (5)$$

$$N_{level}^{sub} = 2n(U_1 + U_2) + 1 \quad (6)$$

TABLE I
SWITCHING STATES OF THE PROPOSED BASIC UNIT

S_1	S_2	S_3	S_4	S_5	S_6	S_X	S_Y	Z_1	Z_2	F_1	F_2	U_o
1	1	0	0	0	0	0	0	0	0	0	0	**0**
1	0	0	1	0	0	0	0	1	0	0	0	U_1
1	0	0	1	0	0	0	0	0	1	0	0	$2U_1$
0	0	1	0	0	1	0	1	0	1	1	0	U_2-$2U_1$
0	0	1	0	0	1	0	1	1	0	1	0	U_2-U_1
1	0	0	0	0	1	0	1	0	0	1	0	U_2
1	0	0	0	0	1	1	0	1	0	1	0	U_1+U_2
1	0	0	0	0	1	1	0	0	1	1	0	$2U_1$+U_2
0	0	1	0	0	1	0	1	0	1	0	1	$2U_2$-$2U_1$
0	0	1	0	0	1	0	1	1	0	0	1	$2U_2$-U_1
1	0	0	0	0	1	0	1	0	0	0	1	$2U_2$
1	0	0	0	0	1	1	0	1	0	0	1	U_1+$2U_2$
1	0	0	0	0	1	1	0	0	1	0	1	$2U_1$+$2U_2$
0	1	1	0	0	0	0	0	1	0	0	0	-U_1
0	1	1	0	0	0	0	0	0	1	0	0	-$2U_1$
0	0	0	1	1	0	0	1	0	1	1	0	-(U_2-$2U_1$)
0	0	0	1	1	0	0	1	1	0	1	0	-(U_2-U_1)
0	1	0	0	1	0	0	1	0	0	1	0	-U_2
0	1	0	0	1	0	1	0	1	0	1	0	-(U_1+U_2)
0	1	0	0	1	0	1	0	0	1	1	0	-($2U_1$+U_2)
0	0	0	1	1	0	0	1	0	1	0	1	-($2U_2$-$2U_1$)
0	0	0	1	1	0	0	1	1	0	0	1	-($2U_2$-U_1)
0	1	0	0	1	0	0	1	0	0	0	1	-$2U_2$
0	1	0	0	1	0	1	0	1	0	0	1	-(U_1+$2U_2$)
0	1	0	0	1	0	1	0	0	1	0	1	-($2U_1$+$2U_2$)

Another key characteristic of multilevel inverters is the total standing voltage on the switches (TSV_{sub}). This criterion is obtained by summing the maximum standing voltage on the switches in their OFF state. TSV_{sub} is calculated as:

$$TSV_{sub} = \sum_{j=1}^{n} U_{Z,j} + \sum_{i=1}^{n} U_{F,j} + \sum_{i=1}^{6} U_{S,j} + U_{S,X} + U_{S,Y} \quad (7)$$

where $U_{Z.j}$, $U_{F.j}$, $U_{S.j}$, $U_{S.X}$, and $U_{S.Y}$ are the values of standing voltages for switches $Z_1, Z_2, Z_3, \cdots, Z_n$, switches $F_1, F_2, F_3, \cdots, F_n$, switches $S_1, S_2, \cdots, S_6$, switch S_X and switch S_Y, respectively. Based on the peak standing voltage values for individual switches, TSV_{sub} can be calculated for each switch as follows:

$$U_{S,1} = U_{S,2} = U_{S,5} = U_{S,6} = n(U_1 + U_2) \quad (8)$$

$$U_{S,3} = U_{S,4} = nU_2 \quad (9)$$

$$U_{S,X} = U_{S,Y} = nU_1 \quad (10)$$

$$\sum_{j=1}^{n} U_{Z,j} = \begin{cases} (\frac{3n^2}{4} - \frac{n}{2})U_1 & ,n = even \\ (\frac{3n^2}{4} - \frac{n}{2} - \frac{1}{4})U_1 & ,n = odd \end{cases} \quad (11)$$

$$\sum_{j=1}^{n} U_{F,j} = \begin{cases} (\frac{3n^2}{4} - \frac{n}{2})U_2 & ,n = even \\ (\frac{3n^2}{4} - \frac{n}{2} - \frac{1}{4})U_2 & ,n = odd \end{cases} \quad (12)$$

$$TSV_{sub} = \begin{cases} (\frac{3n^2}{4} + \frac{11n}{2})(U_1 + U_2) & ,n = even \\ (\frac{3n^2}{4} - \frac{11n}{2} - \frac{1}{4})(U_1 + U_2) & ,n = odd \end{cases} \quad (13)$$

To generate higher levels of output voltage whiles utilizing fewer components, m sub-multilevels can be connected in series as shown in Fig. 3. The output voltage of the proposed cascade multilevel inverter topology (u_o) is obtained by:

$$u_o = u_{o,1} + u_{o,2} + u_{o,3} + \cdots + u_{o,m} \quad (14)$$

According to Table III, the equation of the maximum output voltage of the proposed cascade multilevel inverter is expressed as:

$$u_{o,\max,1} = \left[\frac{(4n+1)^m - 1}{2}\right] U_{dc} = \frac{(N_{level,1} - 1)}{2} U_{dc} \quad (15)$$

Fig. 3 consists of m sub-multilevel units and each sub-multilevel comprises ($n_{j,1} + n_{j,2}$) dc voltage sources in which $n_{j,1}$ and $n_{j,2}$ are the number of voltage sources on the left and right sides of the *j*th sub-multilevel, respectively. To maximize the number of generated voltage levels in the output, with constant device quantity, the number of voltage sources on both sides of each sub-multilevel unit should be equal, and this number must be the same on all sub-multilevel inverters as:

$$n_{j,1} = n_{j,2} = n \quad (16)$$

Using Eq. (16), we have:

$$N_{source} = 2nm \quad (17)$$

$$N_{driver} = m(2n + 8) \quad (18)$$

$$N_{IGBT} = m(4n + 6) \quad (19)$$

TABLE II
NOMINAL VALUES OF VOLTAGE AND CURRENT OF SWITCHES

Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_X	S_Y	Z_1	Z_2	F_1	F_2
Standing voltage	$2(U_1+U_2)$	$2(U_1+U_2)$	$2U_2$	$2U_2$	(U_1+U_2)	$2(U_1+U_2)$	$2U_1$	$2U_1$	U_1	U_1	U_2	U_2
Current rating	I_m	I_m	I_m	I_m	I_m	I_m	I_m	I_m	I_m	I_m	I_m	I_m

The total standing voltage of switches in the proposed MLI (TSV) for $n \geq 2$ is computed using the equations below:

$$TSV = \sum_{u=1}^{m}\left[(\sum_{j=1}^{n} U_{Zk,j} + \sum_{j=1}^{n} U_{Fk,j} + \sum_{j=1}^{6} U_{Sk,j}) + (U_{Sk,X} + U_{Sk,Y})\right] \quad (20)$$

Considering Fig. 3, it is clear that:

$$\sum_{k=1}^{m} U_{Sk,1} = \sum_{k=1}^{m} U_{Sk,2} = \sum_{k=1}^{m} U_{Sk,5} = \sum_{k=1}^{m} U_{Sk,6} = n\sum_{k=1}^{m}(U_{K,1} + U_{K,2}) \quad (21)$$

$$\sum_{k=1}^{m} U_{Sk,3} = \sum_{k=1}^{m} U_{Sk,4} = n\sum_{k=1}^{m} U_{K,2} \quad (22)$$

$$\sum_{k=1}^{m} U_{Sk,X} = \sum_{k=1}^{m} U_{Sk,Y} = n\sum_{k=1}^{m} U_{K,1} \quad (23)$$

$$\sum_{k=1}^{m}\sum_{j=1}^{n} U_{Zk,j} = \begin{cases} (\frac{3n^2}{4} - \frac{n}{2})\sum_{k=1}^{m} U_{k,1} & ,n = even \\ (\frac{3n^2}{4} - \frac{n}{2} - \frac{1}{4})\sum_{k=1}^{m} U_{k,1} & ,n = odd \end{cases} \quad (24)$$

$$\sum_{k=1}^{m}\sum_{j=1}^{n} U_{Fk,j} = \begin{cases} (\frac{3n^2}{4} - \frac{n}{2})\sum_{k=1}^{m} U_{k,2} & ,n = even \\ (\frac{3n^2}{4} - \frac{n}{2} - \frac{1}{4})\sum_{k=1}^{m} U_{k,2} & ,n = odd \end{cases} \quad (25)$$

TSV for $n \geq 2$ is calculated as follows:

$$TSV = \begin{cases} (\frac{3n^2}{4} + \frac{11n}{2})\sum_{k=1}^{m}(U_{k,1} + U_{k,2}) & n = even \\ (\frac{3n^2}{4} - \frac{11n}{2} - \frac{1}{4})\sum_{k=1}^{m}(U_{k,1} + U_{k,2}) & n = odd \end{cases} \quad (26)$$

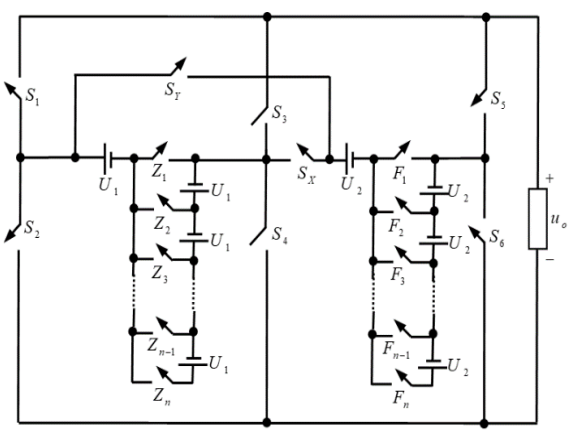


Fig. 2. The proposed sub-multilevel topology.

IV. Determining DC Voltage Source Magnitudes

A. First Algorithm

First sub-multilevel:

$$U_{1,1} = U_{1,2} = U_{dc} \quad (27)$$

The peak output voltage is obtained by:

$$U_{o\max,1} = n(U_{1,1} + U_{1,2}) = 2nU_{dc} \quad (28)$$

Second sub-multilevel:

$$U_{2,1} = U_{2,2} = 2U_{o\max,1} + U_{dc} = (4n+1)U_{dc} \quad (29)$$

The peak output voltage is expressed as:

$$U_{o\max,2} = n(U_{2,1} + U_{2,2}) = 2n(4n+1)\,U_{dc} \quad (30)$$

m^{th} sub-multilevel:

$$U_{m,1} = U_{m,2} = 2\sum_{j=1}^{m-1}(U_{o\max,j}) + U_{dc} = (4n+1)^{m-1}U_{dc} \quad (31)$$

Based on this algorithm, the number of output voltage levels ($N_{level,1}$) is calculated as:

$$N_{level,1} = (4n+1)^m \quad (32)$$

Based on the first algorithm and using Equs. (14), (26), and (32), the maximum generated output voltage ($u_{o,\max,1}$) and the total value of standing voltage on the switches (TSV_1) could be computed by:

$$u_{o,\max,1} = \left[\frac{(4n+1)^m - 1}{2}\right]U_{dc} = \frac{(N_{level,1} - 1)}{2}U_{dc} \quad (33)$$

$$TSV_1 = \begin{cases} (\frac{3n^2}{4} + \frac{11n}{2})\left(\frac{(4n+1)^m - 1}{2n}\right)U_{dc} \\ \quad = \left[\frac{3n^2 + 22n}{8n}\right](N_{level,1} - 1)U_{dc} & n = even \\ (\frac{3n^2}{4} + \frac{11n}{2} - \frac{1}{4})\left(\frac{(4n+1)^m - 1}{2n}\right)U_{dc} \\ \quad = \left[\frac{3n^2 + 22n - 1}{8n}\right](N_{level,1} - 1)U_{dc} & n = odd \end{cases} \quad (34)$$

The number of the variety of dc voltage sources for this algorithm $N_{variety,1}$ is equal to:

$$N_{variety,1} = m \quad (35)$$

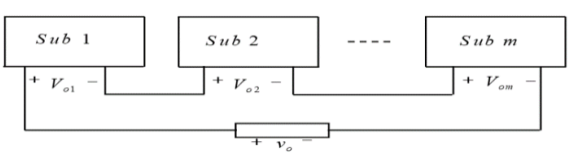


Fig. 3. The topology of the proposed multilevel.

Table III
SWITCHING STATES OF THE PROPOSED SUB-MULTILEVEL.

S_1	S_2	S_3	S_4	S_5	S_6	S_X	S_Y	Z_1	…	Z_{n-1}	Z_n	F_1	…	F_{n-1}	F_n	U_o
1	1	0	0	0	0	0	0	0		0	0	0		0	0	0
1	0	0	1	0	0	0	0	0	…	1	0	0	…	0	0	$(n-1)U_1$
1	0	0	1	0	0	0	0	0		0	1	0		0	0	nU_1
1	0	0	0	0	1	1	0	0		0	1	0		0	1	$n(U_1+U_2)$
							⋮									⋮
0	1	1	0	0	0	0	0	0		1	0	0		0	0	$-(n-1)U_1$
0	1	1	0	0	0	0	0	0		0	1	0		0	0	$-nU_1$
0	1	0	0	1	0	1	0	0		0	1	0		0	1	$-n(U_1+U_2)$

B. Second Algorithm

Unlike the first algorithm, each sub-multilevel has a different dc voltage source magnitude in the second algorithm, as summarized below:

First sub-multilevel unit:

$$U_{1,1} = U_{dc} \tag{36}$$

$$U_{1,2} = (2n+1)U_{1,1} \tag{37}$$

The peak output voltage for the first sub-multilevel is given by:

$$U_{o,\max,1} = n(U_{1,1} + U_{1,2}) = 2n(n+1)U_{dc} \tag{38}$$

Second sub-multilevel:

$$U_{2,1} = 2U_{o,\max,1} + U_{dc} = (2n+1)^2 U_{dc} \tag{39}$$

$$U_{2,2} = (2n+1)U_{2,1} = (2n+1)^3 U_{dc} \tag{40}$$

From Eq. (15), (39), and (40), the peak output voltage for the second sub-multilevel is obtained by:

$$U_{o,\max,2} = n(U_{2,1} + U_{2,2}) = 2n(1+n)(1+2n)^2 U_{dc} \tag{41}$$

*m*th sub-multilevel:

$$U_{m,1} = 2\sum_{j=1}^{m-1}(U_{o\max,j}) + U_{dc} = (2n+1)^{2(m-1)} U_{dc} \tag{42}$$

$$U_{m,2} = (2n+1)\,U_{m,1} = (2n+1)^{2m-1} U_{dc} \tag{43}$$

$$U_{o,\max,2} = n(U_{m,1} + U_{m,2}) = 2n(1+n)(1+2n)^{2(m-1)} U_{dc} \tag{44}$$

Considering the second algorithm, the output voltage levels $(N_{level,2})$ is computed as:

$$N_{level,2} = (2n+1)^{2m} \tag{45}$$

Considering Equs. (14), (26), and (45), the peak output voltage magnitude $(u_{o,\max,2})$ and the total magnitude of the standing voltage on the switches based on the second algorithm (TSV_2) are obtained from the following equations:

$$u_{o,\max,2} = \left(\frac{(2n+1)^{2m}-1}{2}\right)U_{dc} = \frac{(N_{level,2}-1)}{2}U_{dc} \tag{46}$$

$$TSV_2 = \begin{cases} \left(\frac{3n^2}{4}+\frac{11n}{2}\right)\left(\frac{(2n+1)^{2m}-1}{2n}\right)U_{dc} \\ \quad = \left[\frac{3n^2+22n}{8n}\right](N_{level,2}-1)U_{dc}\ ,\ n = even \\ \left(\frac{3n^2}{4}+\frac{11n}{2}-\frac{1}{4}\right)\left(\frac{(2n+1)^{2m}-1}{2n}\right)U_{dc} \\ \quad = \left[\frac{3n^2+22n-1}{8n}\right](N_{level,2}-1)U_{dc}\ ,\ n = odd \end{cases} \tag{47}$$

The variety of the dc voltage sources used $(N_{variety,2})$ is expressed by:

$$N_{variety,2} = 2m \tag{48}$$

V. Optimal Topology

This section analyzes the number of components and standing voltage on the switches, and the minimum number of components and *TSV* are calculated to attain the maximum quantity of the output voltage levels.

A. *Optimal topology for a minimum quantity of IGBTs with constant quantity of output voltage levels*

To identify the configuration that can create a constant number of output voltage levels ($N_{level,1}$) and ($N_{level,2}$) for the minimum quantity of IGBTs, using Eq. (19), (32), and (45), the number of IGBTs are determined as follows:

$$N_{IGBT} = \ln(N_{level,1}) \times \frac{(4n+6)}{\ln(4n+1)} \qquad for\ n \geq 2 \tag{49}$$

$$N_{IGBT} = \ln(N_{level,2}) \times \frac{(4n+6)}{2\ln(2n+1)} \qquad for\ n \geq 2 \tag{50}$$

Fig. 4(a) illustrates the differences of $\frac{(4n+6)}{\ln(4n+1)}$ and $\frac{(4n+6)}{2\ln(2n+1)}$ versus n. According to Fig. 4 (a), it is clear that $n=2$ minimizes the number of IGBTs for $n \geq 2$ for both proposed algorithms to achieve a constant number of output

voltage levels.

B. *Optimal topology for a minimum quantity of gate drivers with a constant quantity of output voltage levels*

Minimizing the number of gate drivers to generate a constant number of output voltage levels ($N_{level,1}$) and ($N_{level,2}$) is the very focus of this section. From (18), (32), and (45), the quantity of gate driver circuits are obtained as follows:

$$N_{driver} = \ln(N_{level,1}) \times \frac{(2n+8)}{\ln(4n+1)} \qquad for\ n \geq 2 \qquad (51)$$

$$N_{driver} = \ln(N_{level,2}) \times \frac{(2n+8)}{2\ln(2n+1)} \qquad for\ n \geq 2 \qquad (52)$$

Fig. 4(b) illustrates the differences of $\frac{(2n+8)}{\ln(4n+1)}$ and $\frac{(2n+8)}{2\ln(2n+1)}$ versus n. From Fig. 4(b), it is clear that the minimum quantity of gate drivers for the first and second proposed algorithms are derived by $n=3$.

C. *Optimal topology for a minimum number of variety of magnitudes of dc voltage sources with a constant number of output voltage levels*

Assuming ($N_{level,1}$) and ($N_{level,2}$) are constant in this section, the focus is to find the best topology that can generate the mentioned number of output voltage levels, using a minimum quantity of variety of dc voltage sources. According to (32) and (35), $N_{variety}$ for the first and second proposed algorithms can be derived as follows, respectively:

$$N_{variety} = \ln(N_{level,1}) \times \frac{1}{\ln(4n+1)} \qquad for\ n \geq 2 \qquad (53)$$

Using (45) and (48), the following equation is calculated:

$$N_{variety} = \ln(N_{level,2}) \times \frac{1}{\ln(2n+1)} \qquad for\ n \geq 2 \qquad (54)$$

Fig. 4(c) illustrates the differences of $\frac{1}{\ln(4n+1)}$ and $\frac{1}{\ln(2n+1)}$ versus n. According to this figure, it is clear that the number of variety of dc voltage sources for a constant $N_{level,1}$ and $N_{level,2}$ will be reduced at the least point of these figures. The least (minimum) points are obtained at $n=\infty$ for the first and second proposed algorithms, which means that the bigger the number of dc sources in series in one sub-multilevel, the less requirement for the variety of dc sources utilized. So, to minimize the variety of dc voltage sources, it is enough to use one sub-multilevel inverter in the optimum topology.

D. *Optimal topology for a minimum number of dc voltage sources with a constant number of output voltage levels*

The main focus of this part is to obtain the value of n to generate maximum $N_{level,1}$ and $N_{level,2}$ with a constant number of dc voltage sources. As it was already indicated in (16), the maximum quantity of voltage levels is generated when the quantity of dc voltage sources in each sub-multilevel is equal. Generally, the quantity of voltage levels is constant, from (17), (32), and (45), N_{source} for the first and second proposed algorithms is expressed accordingly by:

$$N_{source} = \ln(N_{level,1}) \times \frac{2n}{\ln(4n+1)} \qquad for\ n \geq 2 \qquad (55)$$

$$N_{source} = \ln(N_{level,2}) \times \frac{n}{\ln(2n+1)} \qquad for\ n \geq 2 \qquad (56)$$

Fig. 4(d) presents the variations of $\frac{2n}{\ln(4n+1)}$ and $\frac{n}{\ln(2n+1)}$ versus n. Accordingly, the number of dc voltage sources for a constant $N_{level,1}$ and $N_{level,2}$ will be minimized at $n=\infty$ for the initial and second proposed algorithms. So, to minimize the number of dc voltage sources, there will be one sub-multilevel inverter in the optimum topology.

E. *Optimal topology for a maximum number of output voltage levels with a constant number of IGBTs*

In this section, the number of IGBTs is assumed to be constant. Considering (19), (32), and (45), $N_{level,1}$ and $N_{level,2}$ are obtained as follows:

$$N_{level,1} = (4n+1)^{\frac{N_{IGBT}}{(4n+6)}} \qquad for\ n \geq 2 \qquad (57)$$

$$N_{level,2} = (2n+1)^{\frac{2N_{IGBT}}{(4n+6)}} \qquad for\ n \geq 2 \qquad (58)$$

Fig. 4(f) compares $(4n+1)^{\frac{1}{(4n+6)}}$ and $(2n+1)^{\frac{2}{(4n+6)}}$ versus n. It is clear that the maximum number of output voltage levels for the first and second proposed algorithms are generated when $n=2$.

F. *Optimal topology for a maximum number of output voltage levels with a constant number of gate drivers*

In this section, the optimization goal would be to maximize the number of output voltage levels that can be generated using a constant number of gate driver circuits. Considering (18), (32), and (45), $N_{level,1}$ and $N_{level,2}$ can be obtained as follows:

$$N_{level,1} = (4n+1)^{\frac{N_{driver}}{(2n+8)}} \qquad for\ n \geq 2 \qquad (59)$$

$$N_{level,2} = (2n+1)^{\frac{2N_{driver}}{(2n+8)}} \qquad for\ n \geq 2 \qquad (60)$$

In this inverter, the output voltage level count will be maximized when $(4n+1)^{\frac{1}{(2n+8)}}$ and $(2n+1)^{\frac{2}{(2n+8)}}$ reach their maximum value. Fig. 4(g) compares $(4n+1)^{\frac{1}{(2n+8)}}$ and $(2n+1)^{\frac{2}{(2n+8)}}$ versus n according to which the number of output voltage levels will be maximized when $n=3$ for both proposed algorithms.

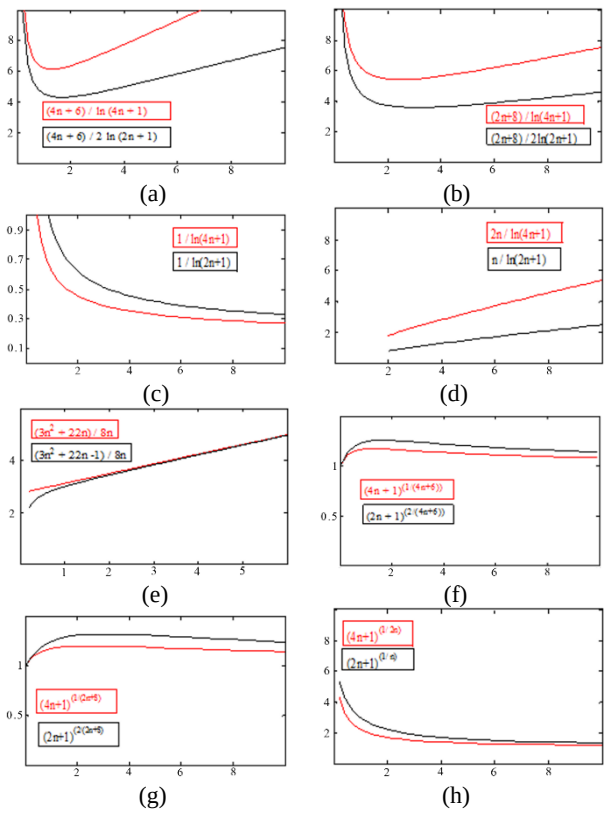


Fig. 4. Variations of different functions versus n.

VI. COMPARISON RESULTS

Fig. 5(a) shows the number of IGBTs versus the number of output voltage levels for the proposed topology with other references. Based on this figure, the proposed topology developed by the second algorithm uses the least amount of IGBT when compared to other structures in [19-30]. The number of the gate drivers required for the proposed topology is compared to other topologies in Fig. 5(b). This comparison indicates that when using the second algorithm for dc voltage source magnitude calculation, the proposed topology needs a minimum number of gate drivers compared to other references. The number of IGBTs, gate driver circuits, dc voltage sources, diodes, and capacitors required to generate at least 69 levels of voltage at the output of 19-30 asymmetric unit structures is summarized in Table IV. According to this table, to generate 69 output voltage levels, the proposed inverter based on the second algorithm requires 16 gate drivers and these numbers are equal to 16, 22, 36, 20, 70, 70, 61, 106, 40, 32, 22, and 21 to produce at least 69 levels in 19-30 topologies, respectively. The number of dc voltage sources is also studied and compared in Fig. 5(c), based on which when using the second algorithm for dc voltage source magnitude calculation, the recommended topology requires fewer dc voltage sources compared to the topologies in [19, 21-29].

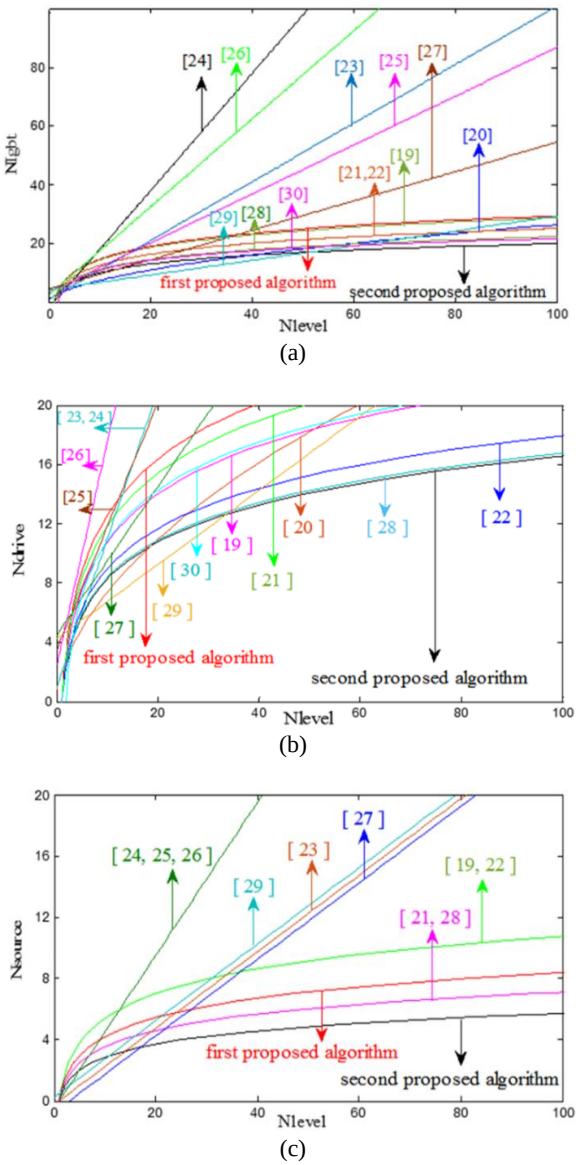


Fig. 5. Variation of (a) N_{IGBT} (b) N_{driver} (c) N_{source} versus N_{level}.

For example, according to Table IV, 69-level inverter based on the second algorithm requires eight dc voltage sources, and this number to produce at least 69 levels is equal to 10, 2, 18, 10, 17, 34, 34, 35, 17, 10, 18, and 1 for the topologies

presented in [19-30], respectively.

Table IV
COMPARISON OF THE PROPOSED INVERTER WITH OTHER STRUCTURES TO PRODUCE AT LEAST 69-LEVEL

Reference	NIGBT	Ndriver	Nsource	Capacitors	Diodes	Standing voltage
19	24	16	10	-	-	**266Vdc**
20	22	22	8	4	8	**9Vdc**
21	36	36	18	-	-	**136Vdc**
22	22	20	10	-	-	**231Vdc**
23	70	70	17	-	-	**138Vdc**
24	136	70	34	-	-	**1802Vdc**
25	61	61	34	-	-	**435Vdc**
26	109	109	35	-	-	-
27	40	40	17	-	16	-
28	32	32	10	-	-	-
29	37	22	18	-	-	**340Vdc**
30	21	21	1	8	4	**524Vdc**
2nd Proposed Algorithm	22	16	8	-	-	**289Vdc**

VII. EXPERIMENTAL RESULTS

This section presents the experimental results for 25 levels of the output voltage (n=2, m=1) based on the second algorithm. As per Fig. 1, this structure consists of four dc voltage sources, 14 IGBTs, and 12 driver circuits. Fig. 6 shows a circuit-built prototype in which values of U_1 and U_2 are selected as 30V and 150V, respectively.

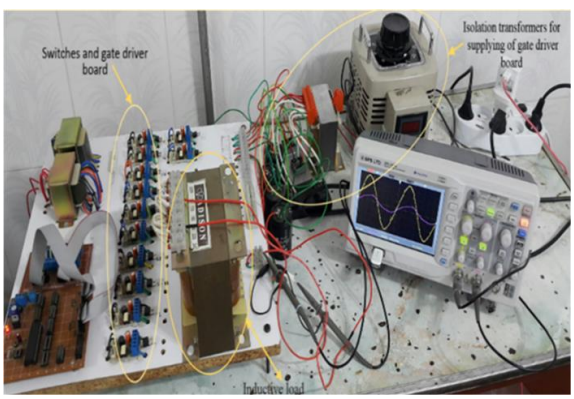


Fig. 6. Laboratory prototype

According to Fig. 7, the maximum output voltage and current are 360V and 4.4A, respectively and an R–L load of $R=85.6\Omega$ and $L=88.6mH$ is utilized to represent the load with an output voltage frequency of 50 Hz. Different control methods can be used to control multi-level inverters. In this paper, the fundamental frequency switching (least error method) is considered the control method. In this control method, switching is done in such a way that according to Fig. 8, the closest step waveform to the desired sinusoidal waveform is created. Fig. 9 shows the voltage on the switches of $S_1,S_2,\cdots,S_6,S_X,S_Y,Z_1,Z_2,F_1,F_2$, which have the maximum voltage of 360, 360, 300, 300, 360, 360, 60, 60, 30, 30, 150, 150 volts, respectively. The total value of standing voltage of the switches for a 25-level inverter (the sum of standing voltage on the switches) is 2520 V, which corresponds to Eq. (26) for $n=2$.

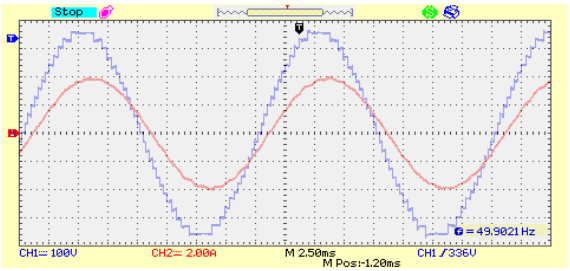


Fig. 7. Experimental results; output 25-level voltage (100V/div), and output 25-level current (2A/div).

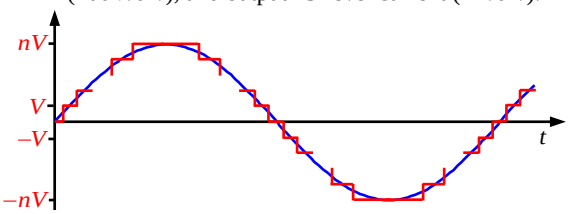


Fig. 8. Fundamental frequency switching control method

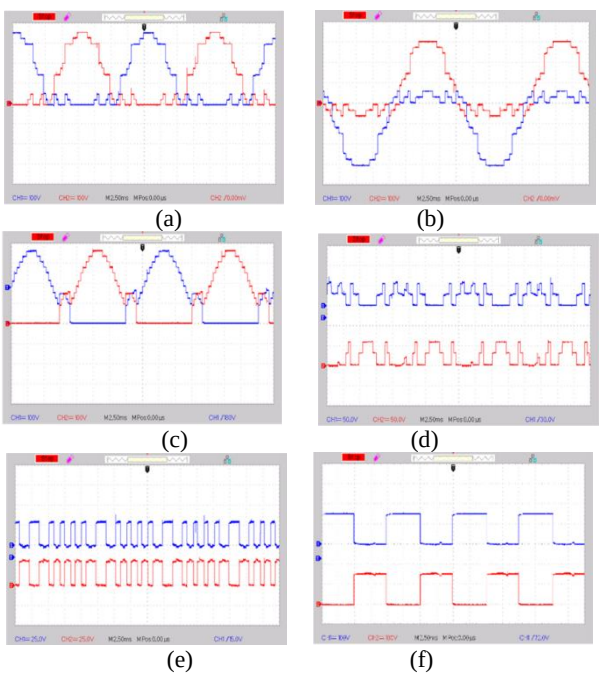


Fig. 9. Voltage waveforms for different switches of the prototype; (a) S1(100 V/div), S2(100 V/div), (b) S3(100 V/div), S4(100 V/div), (c) S5(100 V/div), S6(100 V/div), (d) Sx(50 V/div), Sy(50 V/div), (e) Z1(25 V/div), Z2(25 V/div), (f) F1 (100 V/div), F2 (100 V/div).

VIII. CONCLUSION

A new basic architecture of cascaded multilevel inverter is proposed in this research. The proposed basic unit is comprised of four isolated dc voltage sources and 10

unidirectional and two bidirectional switches with a common-emitter topology. Afterward, the expansion of the basic unit and finally its cascaded variants were examined. To determine the amplitude of dc voltage sources, two algorithms were presented to generate all levels (even and odd) in the output voltage. The optimal extensive topology configuration for different purposes is investigated. For example, it is established that the units with two dc voltage sources and two dc voltage sources are the optimal structure for having a maximum voltage level count at output per specific quantity of IGBTs for both algorithms. The proposed structure was compared with several recently proposed inverter topologies in different aspects. According to the results of the comparison, it is evident that the recommended topology reduced manufacturing cost, volume, and control complexity of the circuit in comparison to the conventional topologies due to having the lowest quantity of IGBTs, gate driver circuits, and dc voltage sources. A 69-level proposed inverter based on the second algorithm requires 22 IGBTs, 16 gate driver circuits, 8 dc voltage sources, no diodes, and no capacitors. To generate the same output voltage level quantity, structures in [23, 26] require 70 and 109 IGBTs, 70 and 109 gate driver circuits, and 17 and 35 dc voltage sources, respectively. The feasibility performance of the proposed structure, for which the dc voltage source magnitudes are calculated with the second algorithm and are controlled with the fundamental frequency control method, is verified through experimental tests performed on a single-phase 25-level prototype.

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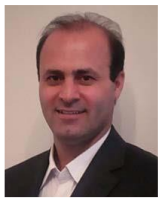
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