

A Controllable Bidirectional Rectifier for EV Home Charging Station with G2H/G2VH/V2H/V2G Functions

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A Finding effective solutions to enhance the process of electric vehicle charging has been the main subject of numerous
B studies. This paper presents a novel bidirectional multiport rectifier that can be used as a wall-box converter that is
S installed in the parking lot of smart buildings and is capable of providing DC-link for local DC loads, such as DC home
T appliances and charge connected EV, simultaneously. The proposed converter is capable of working in
R G2H/G2VH/V2H/V2G modes, enabling the utility grid and costumers to use the EV as a mobile power source and reactive
A power compensator. A control method is also presented that enables the converter to control active and reactive power
C according to the smart grid or customer processed commands. To validate the features of the proposed converter, it
T is simulated in MATLAB/SIMULINK and the results are analyzed. A reduced-scale experimental setup of the proposed
converter is built and tested, and the experimental results confirm the simulation ones.

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I. INTRODUCTION

The use of different types of electric vehicles (EVs) is an effective solution for increasing environmental problems, such as greenhouse emissions, because of its enormous impact on the reduction of massive oil consumption in the transportation sector [1-3]. This has caused a significant rise in EVs usage. The pervasiveness of EVs and their charging needs have caused extensive concerns about their probable effects on the grid [4]. These concerns have led designers and researchers to consider controllable chargers (in terms of power factor (PF)) with low total harmonic distortion (THD) to confirm international standards [5].

Besides all the aforementioned adverse effects of the EVs, the increasing deployment of these cars have opened up

several opportunities for users and smart grids [6-8]. The batteries of EVs have enabled them to work as mobile power sources that can retune their extra stored energy to the grid or suitable load [9-11]. Using appropriate topologies for EV chargers enables them to work in Vehicle-to-Grid (V2G) mode in which active power flows from EV to the grid, in addition to the traditional Grid-to-Vehicle (G2V) mode. A massive number of parked EVs with surplus stored energy provides an opportunity for smart grids to use them for peak shaving purposes. Additionally, EVs can be used as auxiliary power sources to handle AC and DC home appliances to reduce grid energy consumption, or as a backup generator during power outages [12, 13]. EVs can also be used as reactive power compensators that are located near loads and inject reactive power to the power grid [14, 15]. An appropriate topology is, however, required for chargers to allow grasping all these opportunities.

On the other hand, several benefits of a DC power distribution system (DC PDS), such as the absence of reactive

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power and skin effect, which cause a rise in system efficiency and the reduction of the number of AC-DC converters, make that as a predictable future of PDS. Additionally, the flexibility and high efficiency provided by recent advances in power electronics and control methods have made it possible to integrate and merge different DC renewable energy sources efficiently in DC PDSs, primarily residential DC PDSs with undeniable increasing DC load demand due to DC home appliances [16-19]. The operation of EVs' chargers in different modes and applying their capabilities, such as operating as a mobile power source, is more efficient and more accessible in DC PDSs. In these systems, using renewable energies to charge EVs, handling DC home appliances, or returning the battery stored energy to the home or grid can be done quickly and efficiently. A very effective solution for increasing the entire system efficiency is to merge various power converters. AC-DC converters utilized for feeding home DC-Bus and chargers used for EVs are two types of conventional power converters that can be merged.

Although several converters in charging and rectification applications have already been introduced in previous studies, few works have focused on designing an appropriate topology for a converter capable of charging EVs' battery and providing a home DC-Bus simultaneously. The isolated bidirectional AC-DC converter introduced in [19] can be used only as a rectifier to feed the home DC-bus and charging the battery is not considered for that. The bidirectional chargers proposed in [20-22] can charge EV battery and return battery energy to the grid and household loads. Though they have several advantages because of their topologies, they cannot provide any DC-bus, so handling DC loads in V2H mode requires another AC-DC converter which may decrease system efficiency. The multiport converter proposed in [23] is suitable for integrating EVs in smart parking lots, but they can work only as a DC-DC converter and cannot rectify AC grid voltage. All high-performance converters introduced in [5, 24-27] can only charge the connected battery and cannot provide DC-bus for home applications simultaneously. The buck-boost rectifier presented in [28] can provide residential DC-link and cannot charge any EV simultaneously. In [29], a bidirectional rectifier is proposed that can provide two or more outputs. Although it can charge the battery and provide DC-bus simultaneously, the proposed converter cannot work in the V2H mode.

This paper presents a novel bidirectional multiport rectifier that can be installed in the parking lot of smart buildings and is capable of providing DC-bus for DC loads such as lighting systems, air conditioning systems, and charging connected EV batteries simultaneously. As illustrated in Fig. 1(a), the proposed converter can work in four operating modes according to the customer requirements and utility grid conditions. Working as a rectifier to feed DC-bus (G2H; Mode 1), feeding home DC loads and charging connected EV

simultaneously (G2VH; Mode 2), handling DC loads during power outages by the stored energy of battery (V2H; Mode 3), and returning stored energy of batteries to the grid for peak shaving during peak hours (V2G; Mode 4) are the operating modes of the proposed converter. By adopting the control method introduced in this paper, the exchanged active and reactive power between the grid and the converter can be controlled according to the smart grid processed commands or customer requirements, which enables it to be controlled during peak hours and operate as a reactive power compensator that is located very close to the loads. This ability not only causes a reduction in installation and maintenance costs of different reactive power compensators, such as capacitor banks or static synchronous compensators, but it also has no effect on battery performance.

II. ANALYSIS OF THE PROPOSED CONVERTER

A. Configuration

The structure of the presented converter is depicted in Fig.1(b). This two-stage converter consists of an AC-DC stage, as the primary stage, and a DC-DC stage, as the secondary stage. The primary stage includes an AC-DC H-bridge and a DC-link capacitor. Due to the introduced switching pattern, the switches of the left leg (S_{P1} and S_{P2}) have a high-frequency operation and switches of the right leg (S_{P3} and S_{P4}) are OFF or operate with grid frequency depending on the selected operating mode. The secondary stage is a three-port DC-DC converter that has the capability of working in different operating modes according to the status of the relays.

B. Operation Principle and Steady-State Analysis

The operation of each stage of the proposed converter depends upon the converter's operating mode that can be selected by the customer. The primary stage has the same operation in the two first modes (G2H and G2VH). In these modes, the primary stage rectifies the grid voltage with a changeable power factor, thanks to the control strategy introduced in section IV. In the third mode (V2H), the primary stage does not have any function and in the fourth mode (V2G), it works as a single-phase full-bridge inverter and delivers the stored energy of PEV's battery to the grid. The analysis of the converter is presented below in detail.

1- Mode1 (G2H)

- Primary Stage

As already mentioned, rectifying and boosting the grid voltage and controlling active and reactive power depending on the smart grid's commands or the customer's requirements are the tasks of the primary stage during this mode. As shown in Fig. 2, due to the selected high-efficiency switching method [30], in each half cycle of the grid voltage, the

switching cycle is divided into two states. It is worth mentioning that only S_{P1} and S_{P2} have a high-frequency operation and S_{P3} and S_{P4} are OFF.

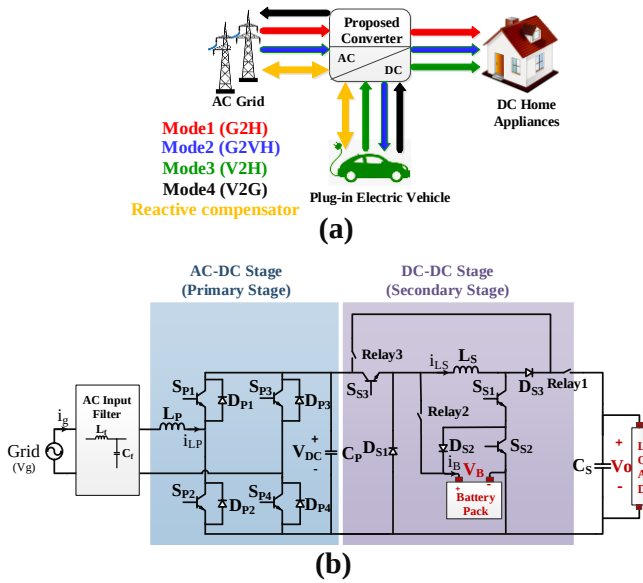


Fig.1. (a) The operating modes and (b) topology of the proposed converter

$V_g > 0$: In the first state ($0 < t < DT_s$), the L_p is magnetized by (V_g) via the path provided by S_{P2} and D_{P4} [Fig. 2(a)]. In the next state ($DT_s < t < T_s$), S_{P2} is turned OFF, so C_p is charged by the energy of L_p and the grid [Fig. 2(b)].

$V_g < 0$: In this condition, as shown in Fig. 2(c)-(d), S_{P1} has a high-frequency operation. First, S_{P1} is ON, so L_p is magnetized by ($-V_g$) via D_{P3} and S_{P1} path [Fig. 2(c)]. Then, S_{P1} is turned OFF, so C_p is charged and L_p is demagnetized [Fig. 2(d)].

The voltage of L_p is obtained in the positive cycle of grid voltage by Eq. (1):

$$\begin{cases} V_{Lp} = V_g & 0 < t < DT_s \\ V_{Lp} = V_g - V_{DC} & DT_s < t < T_s \end{cases} \quad (1)$$

By applying the volt-sec balance law, the voltage gain of the boost rectifier can be achieved by Eq. (2):

$$\frac{V_{DC}}{V_g} = \frac{1}{1-D} \quad (2)$$

• Secondary Stage

In this mode, the DC-DC stage can work as a buck and boost converter and control the V_o voltage according to V_o reference. When the converter is operated in this mode, relay1 is turned ON and relays 2 and 3 are turned OFF.

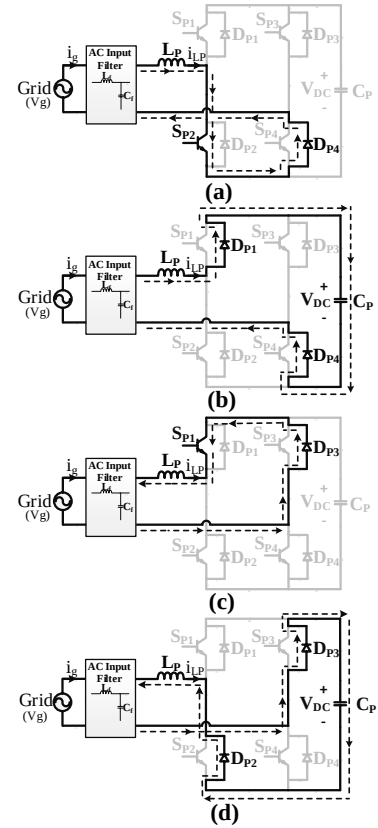


Fig.2. The operation states of the primary stage during mode 1 and mode 2 (a)-(b) $V_g > 0$ (c)-(d) $V_g < 0$

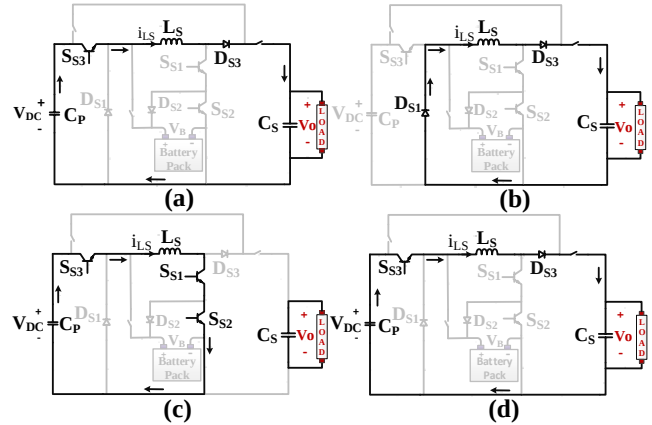


Fig.3. The operation states of the secondary stage during mode 1 (a)-(b) Buck (c)-(d) Boost

A- Buck

S_{S3} , L_s , and D_{S1} are the main components of the secondary stage in the buck condition. The switches S_{S1} and S_{S2} are OFF in this condition.

State 1 ($0 < t < DT_s$): In this state, S_{S3} is ON, so D_{S1} is reversely biased and L_s is magnetized with $(V_{DC} - V_o)$ [Fig.3(a)].

State 2 ($DT_s < t < T_s$): at $t = DT_s$ the S_{S3} is turned OFF, so D_{S1} is directly biased. L_s is demagnetized with $(-V_o)$ and C_s is

charged [Fig. 3(b)].

As depicted in Fig. 3(a)-(b), the voltage and current of L_s and C_s are obtained as follows:

$$\begin{cases} V_{Ls} = V_{DC} - V_o & 0 < t < DT_s \\ V_{Ls} = -V_o & DT_s < t < T_s \end{cases} \quad (3)$$

$$\begin{cases} i_{Cs} = i_{Ls} - \frac{P_o}{V_o} & 0 < t < DT_s \\ i_{Cs} = i_{Ls} - \frac{P_o}{V_o} & DT_s < t < T_s \end{cases} \quad (4)$$

The volt-sec principle can be written as:

$$\frac{1}{T_s} \left[\int_0^{DT_s} (V_{DC} - V_o) dt + \int_{DT_s}^{T_s} (-V_o) dt \right] = 0 \quad (5)$$

So, the voltage gain is obtained by:

$$\frac{V_o}{V_{DC}} = D \quad (6)$$

And the average of L_s current is calculated by:

$$\langle i_{Ls} \rangle = \frac{P_o}{V_o} \quad (7)$$

B- Boost

In the boost condition, S_{S2} and S_{S3} are ON and S_{S1} has a high-frequency operation. As depicted in Fig. 3(c)-(d), the operation of this stage is divided into two states in this mode.

State 1 ($0 < t < DT_s$): In this state, S_{S1} is ON, so D_{S3} is reversely biased and L_s is magnetized with (V_{DC}) [Fig. 3(c)]. Since S_{S2} is ON, the D_{S2} is reversely biased.

State 2 ($DT_s < t < T_s$): at $t = DT_s$, the S_{S1} is turned OFF, so D_{S3} is directly biased. L_s is demagnetized with $(V_{DC} - V_{out})$ and C_s is charged [Fig. 3(d)].

The voltage and current of L_s and C_s are obtained as follows:

$$\begin{cases} V_{Ls} = V_{DC} & 0 < t < DT_s \\ V_{Ls} = V_{DC} - V_o & DT_s < t < T_s \end{cases} \quad (8)$$

$$\begin{cases} i_{Cs} = -\frac{P_o}{V_o} & 0 < t < DT_s \\ i_{Cs} = i_{Ls} - \frac{P_o}{V_o} & DT_s < t < T_s \end{cases} \quad (9)$$

The volt-sec balance can be written as:

$$\frac{1}{T_s} \left[\int_0^{DT_s} (V_{DC}) dt + \int_{DT_s}^{T_s} (V_{DC} - V_o) dt \right] = 0 \quad (10)$$

So, voltage gain can be obtained from:

$$\frac{V_o}{V_{DC}} = \frac{1}{1-D} \quad (11)$$

And the average of L_s current is calculated as:

$$\langle i_{Ls} \rangle = \frac{1}{1-D} \frac{P_o}{V_o} \quad (12)$$

2- Mode 2 (G2VH)

• Primary Stage

The operation of this stage in the second mode is exactly similar to the first mode and rectifies grid voltage [Fig. 2].

• Secondary Stage

In the G2VH mode, the switches of the secondary stage are controlled so as to feed the DC load and charge the connected battery simultaneously. Like the G2H mode, when the converter is operated in the G2VH mode, S_{S3} and relay 1 are turned ON, and relays 2 and 3 are turned OFF. The switching cycle is divided into three states:

State1 ($0 < t < D_1 T_s$): In this time interval, both S_{S1} and S_{S2} are ON, so D_{S2} and D_{S3} are reversely biased. L_s is magnetized with V_{DC} [Fig. 4(a)].

State 2 ($D_1 T_s < t < D_2 T_s$): at $t = D_1 T_s$, S_{S2} is turned OFF and D_{S2} is directly biased and the battery is consequently charged. L_s keeps charging with $(V_{DC} - V_B)$. Until $t = D_2 T_s$, the C_s handles the DC load [Fig. 4(b)].

State 3 ($D_2 T_s < t < T_s$): at the beginning of this time interval, S_{S1} is turned OFF, so D_{S3} is directly biased, and L_s is demagnetized via D_{S3} and C_s path [Fig. 4(c)].

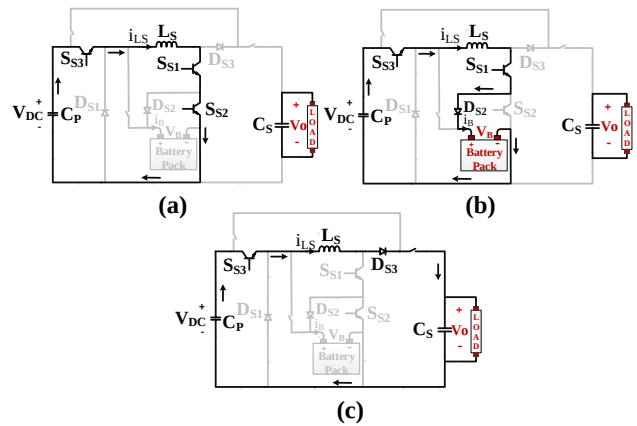


Fig.4. the operation states of the secondary stage during mode2

The voltage and current of L_s and C_s are obtained as follows:

$$\begin{cases} V_{Ls} = V_{DC} & 0 < t < D_1 T_s \\ V_{Ls} = V_{DC} - V_B & D_1 T_s < t < D_2 T_s \\ V_{Ls} = V_{DC} - V_o & D_2 T_s < t < T_s \end{cases} \quad (13)$$

$$\begin{cases} i_{CS} = -\frac{P_o}{V_o} & 0 < t < D_1 T_s \\ i_{CS} = -\frac{P_o}{V_o} & D_1 T_s < t < D_2 T_s \\ i_{CS} = i_{Ls} - \frac{P_o}{V_o} & D_2 T_s < t < T_s \end{cases} \quad (14)$$

The pertinent equation for the volt-sec balance can be written as follows:

$$\frac{1}{T_s} \left[\int_0^{D_1 T_s} (V_{DC}) dt + \int_{D_1 T_s}^{D_2 T_s} (V_{DC} - V_B) dt + \int_{D_2 T_s}^{T_s} (V_{DC} - V_o) dt \right] = 0 \quad (15)$$

The output voltage (V_o) of mode 2 can be calculated using Eq. (16):

$$V_o = \frac{1}{1-D_2} V_{DC} - \frac{D_2 - D_1}{1-D_2} V_B \quad (16)$$

By applying the current-sec principle on C_s , the average current of L_s is obtained as:

$$\langle i_{Ls} \rangle = \frac{1}{1-D_2} \frac{P_o}{V_o} \quad (17)$$

3- Mode 3 (V2H)

Transferring the battery's stored energy to DC load is the task of the proposed converter in this mode. By turning OFF the S_{S3} and relay 3 and also turning ON the relays 1 and 2, the converter receives the power from the battery and is disconnected from the primary stage. So, the primary stage does not have any task in this mode.

• Secondary Stage

In this mode, S_{S2} is ON and only S_{S1} has a high-frequency operation.

State 1 ($0 < t < DT_s$): in this time interval, S_{S1} is ON, so L_s is magnetized with (V_B) [Fig. 5(a)].

State 2 ($DT_s < t < T_s$): at the beginning of this time interval, S_{S1} is turned OFF, so D_{S3} is directly biased, and L_s is demagnetized by ($V_B - V_o$) [Fig. 5(b)].

The voltage across L_s in mode 3 is determined by the following equations:

$$\begin{cases} V_{Ls} = V_B & 0 < t < DT_s \\ V_{Ls} = V_B - V_o & DT_s < t < T_s \end{cases} \quad (18)$$

The L_s volt-sec principle can be written as:

$$\frac{1}{T_s} \left[\int_0^{DT_s} (V_B) dt + \int_{DT_s}^{T_s} (V_B - V_o) dt \right] = 0 \quad (19)$$

So, the voltage gain is obtained by:

$$\frac{V_o}{V_B} = \frac{1}{1-D} \quad (20)$$

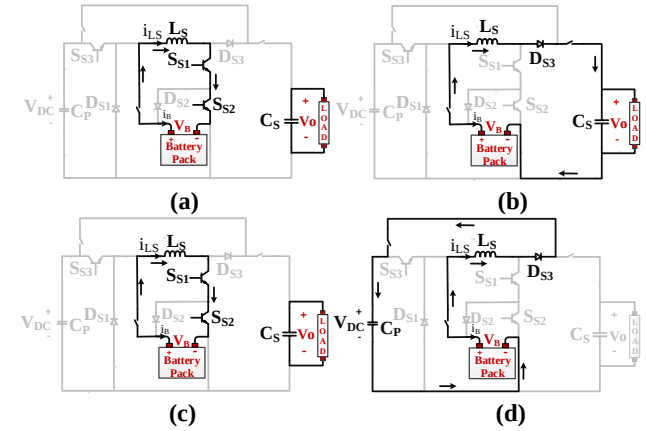


Fig. 5. The operation states of the secondary stage during (a)-(b) mode 3 (c)-(d) mode 4

4- Mode 4 (V2G):

In this mode, the converter delivers the battery's stored energy to the grid with controllable active and reactive power. First, the DC-DC stage regulates the battery voltage according to $V_{DC,ref}$. Then, the AC-DC stage works as a single-phase full-bridge inverter and inverts the DC voltage of DC-link to AC. So, in this part, the DC-DC stage is analyzed before the AC-DC stage.

• Secondary Stage

The operation of the DC-DC stage in this stage is similar to mode 3 with a minor difference. In this mode, relays 2 and 3 are turned ON, and relay 1 is turned OFF, so the secondary stage charges C_p instead of C_s .

State 1 ($0 < t < DT_s$): in this time interval, S_{S1} is ON, so L_s is magnetized by (V_B) [Fig. 5(c)].

State 2 ($DT_s < t < T_s$): at $t=DT_s$, the S_{S1} is turned OFF, so D_{S3} is directly biased, and since $R1$ is ON, L_s is demagnetized by ($V_B - V_{DC}$) [Fig. 5(d)].

The L_s volt-sec balance law can be written as:

$$\frac{1}{T_s} \left[\int_0^{DT_s} (V_B) dt + \int_{DT_s}^{T_s} (V_B - V_{DC}) dt \right] = 0 \quad (21)$$

And voltage gain is obtained by:

$$\frac{V_{DC}}{V_B} = \frac{1}{1-D} \quad (22)$$

• Primary Stage

In this mode, the primary stage works as a single-phase full-bridge inverter that inverts the DC voltage of the DC-link to AC with controllable active and reactive power according to the smart grid commands or customer. Similar to the G2H and G2VH modes, the switching pattern of this stage depends on the grid voltage sign. The switching states and current paths are shown in Fig. 6.

The voltage of LP is obtained by Eq. (23):

$$\begin{cases} V_{LP} = V_{DC} - V_g & 0 < t < DT_s \\ V_{LP} = -V_g & DT_s < t < T_s \end{cases} \quad (23)$$

By applying the volt-sec balance law, the voltage gain of the buck inverter can be estimated by Eq. (24):

$$\frac{V_g}{V_{DC}} = D \quad (24)$$

C. Design Considerations

▪ L_P

The analysis of the L_P 's current ripple during inductor magnetizing time ($kT_s < t < D(k+1)T_s$) is the key to calculating the required inductor value. The L_P 's current ripple can be written as Eq. (25):

$$\Delta i_g = \frac{V_{LP} \times D \times T_s}{L_P} \quad (25)$$

By using KVL during inductor magnetizing time, the inductor voltage is achieved as:

$$V_{LP} = V_g \quad (26)$$

By substituting the voltage gain of boost rectifier (27) into (26), the L_P 's current ripple is obtained as Eq. (28):

$$V_g = (1 - D) \times V_{DC} \quad (27)$$

$$\Delta i_g = \frac{V_{DC} \times D \times (1 - D)}{L_P \times f_s} \quad (28)$$

The worst case in calculating L_P is related to the maximum value of $(D(1-D))$, which is 0.25, so the L_P 's value can be obtained by using Eq. (30):

$$\text{Max}(D(1 - D)) = 0.25 \quad (29)$$

$$L_P = \frac{V_{DC}}{4 \times \Delta i_g \times f_s} \quad (30)$$

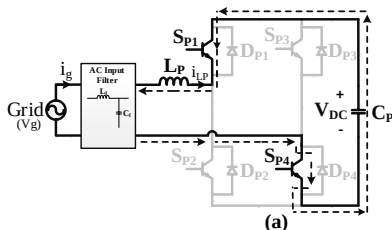


Fig. 6(a)

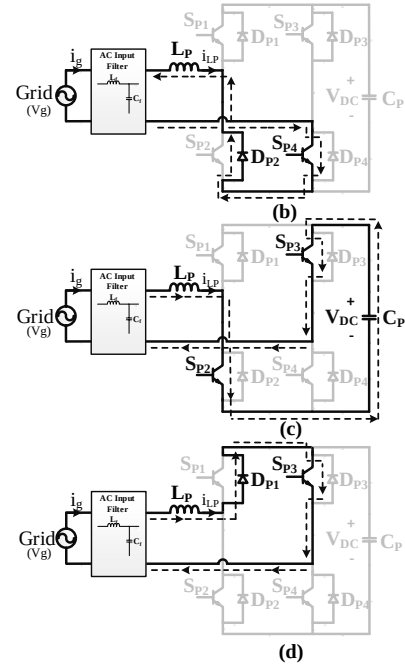


Fig. 6. The operation states of the primary stage during mode4 (a)-(b) $V_g > 0$ (c)-(d) $V_g < 0$

▪ C_{DC}

Handling constant-power loads from a single-phase power grid needs an intermediary device, which is named C_P in this converter. Having appropriate voltage and current in each output ports in terms of ripple depends on the suitable DC-link capacitor (C_P). The DC-link voltage has two terms:

$$V_{DC} = V_{DC} + \Delta V_{DC} \quad (31)$$

where V_{DC} and ΔV_{DC} are the average value and oscillating amplitude of DC-link voltage, respectively. The energy of C_P can be calculated as follows:

$$\frac{1}{2} \cdot C_P \cdot v_{DC}^2 = \int \tilde{p} dt \quad (32)$$

where $\tilde{p}$ is the oscillating value of the instantaneous power:

$$\tilde{p} = 2VI \cos(2\omega t + \varphi) \quad (33)$$

By substituting Eq. (33) into Eq. (32), the required value of C_P is obtained as:

$$C_P = \frac{2V_g I_g}{\omega \Delta V_{DC} V_{DC}} \quad (34)$$

▪ L_S

The DC-DC stage operation in the CCM condition depends on the L_S value, which can be calculated as follows:

$$L_{S \min} = \frac{D_3^2 (V_{DC} - V_o) V_o}{P_{out} f_s} \quad (35)$$

▪ C_f and L_f

To design an effective input filter, the maximum value of the

capacitor of the filter can be obtained as:

$$C_{f \max} = \frac{I_m}{\omega V_m} \tan(\theta) = \frac{\sqrt{2} P_{\max}}{\omega V_m V_g} \tan(\theta) \quad (36)$$

where V_m and I_m are the peak values of the grid voltage and input current, respectively. θ is the displacement angle between the grid voltage and input current, respectively [31]. The required inductive component (L_{req}) can be calculated by using Eq. (37):

$$L_f = L_{\text{req}} + L_g \rightarrow L_{\text{req}} = \frac{1}{4\pi^2 f_c^2 C_f} - 4 \times 10^{-2} \times \left[\frac{1}{\omega L} \right] \times \left[\frac{V_g^2}{P_{\text{out}}} \right] \quad (37)$$

where f_c is the cut-off frequency and L_g is the grid impedance, which is considered 4-5% of the base impedance [32].

D. Efficiency Analysis

To analyze the efficiency of the proposed converter, the parasitic resistance of different components should be considered in addition to the threshold voltage of diodes. R_{Lp} and R_{Ls} are the equivalent series resistance (ESR) of the primary and secondary inductors, respectively. The primary and secondary stage diodes forward resistance are R_{FDpi} and R_{FDsi} , respectively, with V_{FDpi} and V_{FDsi} threshold voltages. Similarly, r_{Dspi} and r_{Dssi} are the primary and secondary switches ON-state resistance. ESR of the capacitors is assumed to be r_{cp} and r_{cs} . It is worth mentioning that the efficiency analysis is done in mode 2, which contains the most parasitic resistance counts.

The conduction losses of inductors can be calculated by using the RMS currents of inductors and their ESR as follows:

$$P_{R_{Ls}} = R_{Ls} I_{\text{rms}, Ls}^2 = R_{Ls} \left(\frac{I_o}{1-D_2} \right)^2 \quad (38)$$

$$P_{R_{Lp}} = R_{Lp} I_{\text{rms}, Lp}^2 = R_{Lp} \left(\frac{I_{\text{ms}, Lp}}{1-D_p} \right)^2 = R_{Lp} \left(\frac{I_o}{(1-D_p)(1-D_2)} \right)^2 \quad (39)$$

where D_p is the duty cycle of the primary stage.

To calculate the conduction losses of the power switches, RMS values switches currents are needed, which can be calculated as:

$$I_{\text{rms}, SP2} = \sqrt{\frac{1}{T_s} \int_0^{D_p T_s} i_{SP2}^2 dt} = \sqrt{\frac{1}{T_s} \int_0^{D_p T_s} i_{Lp}^2 dt} = \sqrt{D_p} i_{Lp} = \frac{\sqrt{D_p}}{(1-D_p)(1-D_2)} I_o \quad (40)$$

$$I_{\text{rms}, S1} = \sqrt{\frac{1}{T_s} \int_0^{D_2 T_s} i_{LS}^2 dt} = \sqrt{D_2} i_{LS} = \frac{\sqrt{D_2}}{(1-D_2)} I_o \quad (41)$$

$$I_{\text{rms}, S2} = \sqrt{\frac{1}{T_s} \int_0^{D_2 T_s} i_{LS}^2 dt} = \frac{\sqrt{D_1}}{(1-D_2)} I_o \quad (42)$$

$$I_{\text{rms}, S3} = \frac{1}{(1-D_2)} I_o \quad (43)$$

So, the conduction losses are calculated as:

$$P_{r_{DSP2}} = r_{DSP2} I_{\text{rms}, SP2}^2 = r_{DSP2} \left(\frac{\sqrt{D_p}}{(1-D_p)(1-D_2)} I_o \right)^2 \quad (44)$$

$$P_{r_{DSS1}} = r_{DSS1} I_{\text{rms}, S1}^2 = r_{DSS1} \left(\frac{\sqrt{D_2}}{1-D_2} I_o \right)^2 \quad (45)$$

$$P_{r_{DSS2}} = r_{DSS2} I_{\text{rms}, S2}^2 = r_{DSS2} \left(\frac{\sqrt{D_1}}{1-D_2} I_o \right)^2 \quad (46)$$

$$P_{r_{DSS3}} = r_{DSS3} I_{\text{rms}, S3}^2 = r_{DSS3} \left(\frac{1}{1-D_2} I_o \right)^2 \quad (47)$$

The switching losses should also be considered that can be calculated by the following equations:

$$P_{SWP2} = f_s C_s V_{P2}^2 = f_s C_s \left(\frac{V_g}{1-D_p} \right)^2 \quad (48)$$

$$P_{SWS1} = f_s C_s V_{S1}^2 = f_s C_s \left(\frac{V_o}{2} \right)^2 \quad (49)$$

$$P_{SWS2} = f_s C_s V_{S2}^2 = f_s C_s \left(\frac{V_o}{2} \right)^2 \quad (50)$$

RMS values of the diodes' currents can be calculated as:

$$I_{\text{rms}, DP1} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{DP1}^2 dt} = \sqrt{\frac{1}{T_s} \int_{D_p T_s}^{T_s} i_{Lp}^2 dt} = \sqrt{1-D_p} i_{Lp} = \frac{\sqrt{1-D_p}}{(1-D_p)(1-D_2)} I_o \quad (51)$$

$$I_{\text{rms}, DP4} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{DP4}^2 dt} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{Lp}^2 dt} = i_{Lp} = \frac{1}{(1-D_p)(1-D_2)} I_o \quad (52)$$

$$I_{\text{rms}, DS2} = \sqrt{\frac{1}{T_s} \int_{D_2 T_s}^{D_2 T_s + D_1 T_s} i_{LS}^2 dt} = \frac{\sqrt{D_2 - D_1}}{1-D_2} I_o \quad (53)$$

$$I_{\text{rms}, DS3} = \sqrt{\frac{1}{T_s} \int_{D_2 T_s}^{T_s} i_{LS}^2 dt} = \frac{1}{\sqrt{1-D_2}} I_o \quad (54)$$

So, the diodes' forward resistance losses can be calculated as:

$$P_{R_{FDP1}} = R_{FDP1} I_{\text{rms}, DP1}^2 = R_{FDP1} \left(\frac{\sqrt{1-D_p}}{(1-D_p)(1-D_2)} I_o \right)^2 \quad (55)$$

$$P_{R_{FDP4}} = R_{FDP4} I_{rms, DP4}^2 = R_{FDP4} \left(\frac{1}{(1-D_p)(1-D_2)} I_o \right)^2 \quad (56)$$

$$P_{R_{FDS2}} = R_{FDS2} I_{rms, DS2}^2 = R_{FDS2} \left(\frac{\sqrt{D_2 - D_1}}{1 - D_2} I_o \right)^2 \quad (57)$$

$$P_{R_{FDS3}} = R_{FDS3} I_{rms, DS3}^2 = R_{FDS3} \left(\frac{1}{\sqrt{1-D_2}} I_o \right)^2 \quad (58)$$

And their forward voltage losses are calculated by Eq. (59)-(62).

$$P_{VF, DP1} = V_{FDP1} I_{DP1} = (V_{FDP1}) \left(\frac{1}{1-D_2} I_o \right) \quad (59)$$

$$P_{VF, DP4} = V_{FDP4} I_{DP4} = (V_{FDP4}) \left(\frac{1}{(1-D_p)(1-D_2)} I_o \right) \quad (60)$$

$$P_{VF, DS2} = V_{FDS2} I_{DS2} = (V_{FDS2}) \left(\frac{D_2 - D_1}{1 - D_2} I_o \right) \quad (61)$$

$$P_{VF, DS3} = V_{FDS3} I_{DS3} = (V_{FDS3}) (I_o) \quad (62)$$

To calculate the capacitors' power losses, their RMS currents are needed, so:

$$I_{rms, CS} = \sqrt{\frac{1}{T_s} \left[\int_0^{D_2 T_s} (-I_o)^2 dt + \int_{D_2 T_s}^{T_s} (i_{LS} - I_o)^2 dt \right]} = \quad (63)$$

$$\sqrt{(D_2 I_o^2) + (1 - D_2)(i_{LS} - I_o)^2} = \sqrt{\frac{D_2}{1 - D_2}} I_o$$

$$I_{rms, Cp} = \sqrt{\frac{1}{T_s} \left[\int_0^{D_p T_s} (i_{LS})^2 dt + \int_{D_p T_s}^{T_s} (i_{LP})^2 dt \right]} = \quad (64)$$

$$\sqrt{\left(\frac{D_p}{(1-D_2)^2} \right) I_o^2 + \left(\frac{D_p^2}{(1-D_p)(1-D_2)} \right) I_o^2} = \sqrt{\frac{D_p}{(1-D_p)(1-D_2)^2}} I_o$$

So, the capacitors' power losses are obtained as follows:

$$P_{r_{CS}} = r_{CS} I_{rms, CS}^2 = r_{CS} \left(\sqrt{\frac{D_2}{1-D_2}} I_o \right)^2 \quad (65)$$

$$P_{r_{Cp}} = r_{Cp} I_{rms, Cp}^2 = r_{Cp} \left(\sqrt{\frac{D_p}{(1-D_p)(1-D_2)^2}} I_o \right)^2 \quad (66)$$

The total power loss is the sum of the calculated losses, which is obtained by:

$$P_{Loss} = \sum P_{RL} + \sum P_{r_{DS}} + \sum P_{sw} + \sum P_{r_{FD}} + \sum P_{v_{FD}} + \sum P_{r_{C}} \quad (67)$$

And finally, the efficiency of the proposed converter in mode2 is calculated by Eq. (68):

$$\eta = \frac{1}{1 + \frac{P_{Loss}}{P_o}} = \frac{1}{1 + \frac{A}{R_o(1-D_2)^2} + \frac{B}{R_o(1-D_p)^2(1-D_2)^2} + \frac{C}{P_o(1-D_p)^2} + \frac{D}{2P_o}} + \frac{1}{\frac{E}{R_o(1-D_2)} + \frac{F}{1-D_2} + \frac{G}{R_o(1-D_p)(1-D_2)^2} + \frac{H}{(1-D_p)(1-D_2)}} \quad (68)$$

where

$$\begin{aligned} A &= R_{LS} + r_{DSS1} D_2 + r_{DSS2} D_1 + r_{DSS3} + R_{FDS2} (D_2 - D_1) \\ B &= R_{LP} + r_{DSP2} D_p + R_{FDP1} (1 - D_p) + R_{FDP4} \\ C &= f_s C_s V_g^2 \\ D &= f_s C_s V_o^2 + 2 V_{FDS3} I_o \\ E &= R_{FDS3} + r_{CS} D_2 \\ F &= V_{FDP1} + V_{FDS2} (D_2 - D_1) \\ G &= r_{Cp} D_p \\ H &= V_{FDP4} I_o \end{aligned} \quad (69)$$

III. COMPARISON STUDY

The presented converter is compared with similar converters introduced in recent years in terms of operating modes that they can work in and the number of high-frequency switches. The results are provided in Table 1.

TABLE I. THE COMPARISON OF THE PROPOSED CONVERTER WITH CONVENTIONAL CONVERTERS

Reference	Operating modes					Number of high-frequency switches
	G2H	G2VH	V2H	V2G	G2V	
[5]	×	×	×	×	✓	1
[19]	✓	×	×	✓	×	12
[20]	×	×	×	✓	✓	6
[21]	×	×	×	✓	✓	6
[22]	×	×	×	✓	✓	8
[23]	×	×	×	✓	✓	3
[24]	×	×	×	×	✓	2
[25]	×	×	×	×	✓	8
[26]	×	×	×	×	✓	3
[27]	×	×	×	×	✓	2
[28]	✓	×	×	×	×	1
[29]	✓	✓	×	✓	✓	6
The proposed converter	✓	✓	✓	✓	✓	7

IV. CONTROL METHOD

Designing an appropriate controller is necessary to control the input current waveform and also active and reactive power flowing between the grid and the proposed converter. Similar to other two-stage converters, the proposed converter needs two interrelated controllers. They can work dependently or independently with one another depending on the system operation. The system condition simulated and implemented in the experimental setup in this paper needs

independent controller subsections, so only the primary stage controller is analyzed and the secondary stage operates open loop.

In this paper, a dual-loop Proportional-Integral (PI) controller is considered for the AC-DC stage. Using a dual-loop PI controller improves the converter performance and also input current and output voltage in terms of THD and ripple, respectively. The first loop controls the active and reactive power according to the utility grid commands or customer requirements by calculating input current reference. It is possible to control the DC-link voltage directly by setting $V_{DC,ref}$ manually. In this case, the controller is allowed to control only reactive power. The second loop generates gate pulses by calculating the difference between reference and measured input current.

As illustrated in Fig. 7, the quadrature signals of grid voltage and input current are first driven by using delay blocks. Then, the single-phase active and reactive power is computed by using the instantaneous pq theory introduced in [33]. After that, there are P-loop and Q-loop controllers. In the P-loop, a PI controller is first used to modify $V_{DC,ref}$ in order to track active power command (P_C). Afterward, another PI controller is used to track the calculated $V_{DC,ref}$. Similarly, in the Q-loop, a PI controller is used to track reactive power command (Q_C). In this step, there are two options: (1) controlling the DC-link voltage directly by setting $V_{DC,ref}$ and controlling reactive power; and (2) controlling active and reactive power simultaneously according to the processed commands from the utility grid or customer. In the first case (the method simulated and tested in this paper), the two stages' controllers

can work independently, but in the second case, they have to work dependently. The computed active and reactive power is used to calculate input current reference via Eq. (70)-(72):

$$\theta = \tan^{-1} \left(\frac{Q_{ref}}{P_{ref}} \right) \quad (70)$$

$$I_{ref} = \frac{P_{ref}}{V_g \cos(\theta)} \quad (71)$$

$$i_{ref}^* = \sqrt{2} I_{ref} \sin(\omega t - \theta) \quad (72)$$

In the second loop, the calculated reference and measured currents are used to obtain the error signal that is fed to the PI controller. The output of the PI controller is compared with a 30kHz triangle waveform and finally, the gate pulses are generated using logic blocks as shown in Fig. 7.

The dynamic of this converter is nonlinear. If the dynamic of the system is linearized, a linear controller can be used. With attention to the system dynamic, it can be linearized around its set point, and then a linear cascade controller via the bode diagram technique in frequency space can be designed. Fig. 8 shows the bode plot of the DC-link voltage in open loop, open loop via a controller, and closed-loop via controller conditions with properties provided in Table 2. As shown in Fig. 8, the AC-DC stage can be controlled by using a properly designed PI controller with PI parameters calculated according to Fig. 8 and Table.2.

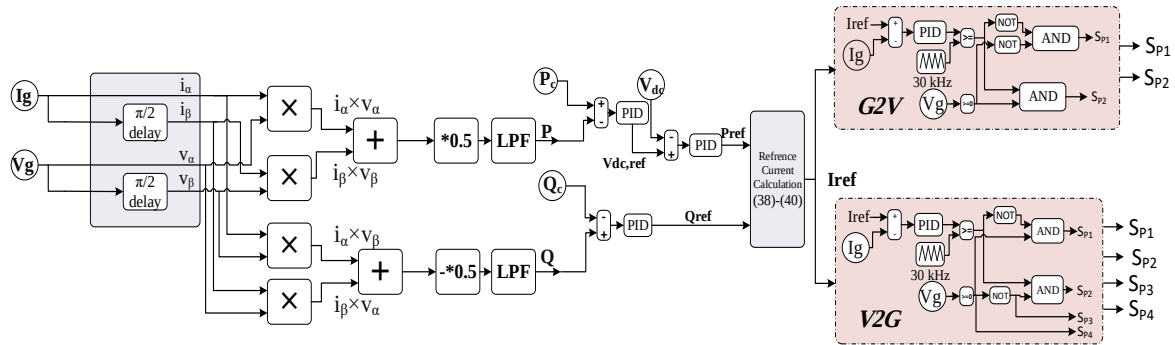


Fig. 7. The proposed control method

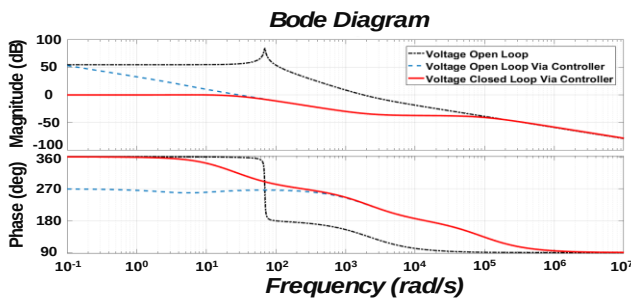


Fig. 8. The bode plot of the DC-link voltage

TABLE II. THE BODE PLOT PROPERTIES

Closed-loop via controller	
Bandwidth	31.9 rad/S
Open-loop	
Gain Margin	-54.5 dB
Phase Margin	-40.1 deg
Open-loop via Controller	
Gain Margin	37.3 dB
Phase Margin	85.1 deg
Closed-loop	
Gain Margin	37.2 dB
Phase Margin	161 deg

V. SIMULATION RESULTS

The presented converter has been simulated in different modes in the MATLAB/SIMULINK software to validate system analysis. The converter specifications are tabulated in Table 3. It is assumed that the converter is connected to the grid (220 V_{rms}), and the battery pack voltage is considered 320V. The home DC link is 400V with a 5kW DC load.

The proposed converter is simulated in unity power condition in mode 1 and results are presented in Fig. 9 through Fig. 15. Fig. 9 shows the grid voltage (V_g) and input current (I_g) in the UPF condition. The FFT analysis in three cycles of the input current is shown in Fig. 10, which illustrates the THD value as 3.47% with acceptable harmonic orders. Figs. 11 and 12 are related to the control unit operation in either mode1 or mode 2. Fig. 11 shows the current loop PID output which is compared with a 30 kHz triangular wave. The S_{P1} and S_{P2} gate pulses are depicted in Fig. 12. As already mentioned, S_{P1} and S_{P2} have a high-frequency operation in the negative and positive half cycle of the grid voltage, respectively.

TABLE III. THE PROPOSED CONVERTER'S SPECIFICATIONS

	Simulation	Experimental
Input voltage (V_g)	220 V(RMS)	30 V(RMS)
Output voltage (V_o)	400 V	160 V
DC-link voltage (V_{DC})	340 V	110 V
Output Power	5 kW	200 W
Battery Voltage	320 V	70 V
L_p	4.4 mH	4 mH
L_s	1.5 mH	1.5 mH
C_p	9 mF	6 mF
C_s	680 μ F	470 μ F
Maximum input current THD	4.24%	-
AC Input Frequency	50 Hz	50 Hz
Switching Frequency	30kHz	30 kHz
Maximum Output Voltage Ripple	2%	-
Power Factor	0.99	0.99
Controller	-	ARMSTM32F103RET
Mosfet	-	KF13N60
Current Sensor	-	ACS712

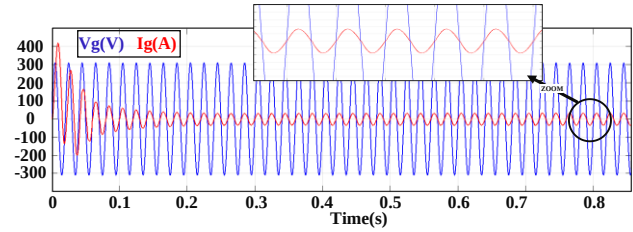


Fig. 9. The grid voltage and input current in mode 1

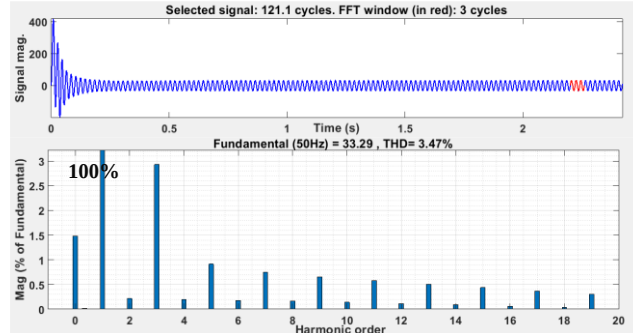


Fig. 10. The FFT analysis of input current in mode 1

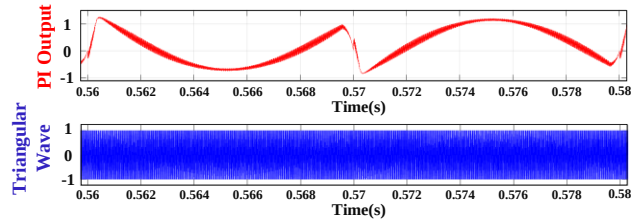


Fig. 11. The current loop PID output and triangular wave

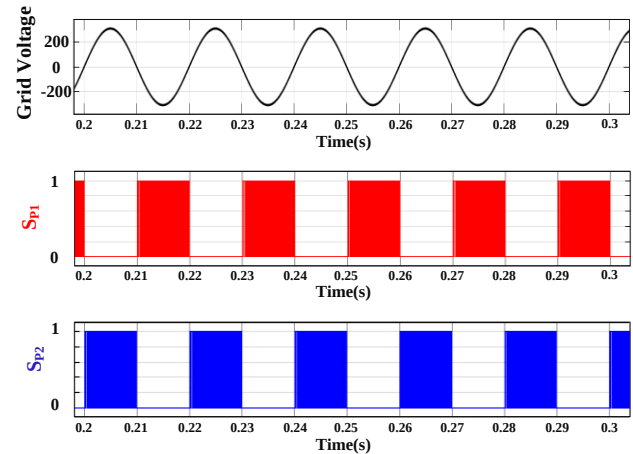


Fig. 12. The gate pulses of S_{P1} and S_{P2} in mode 1

Fig.13 illustrates the reference and measured input current, which shows the perfect capability of the converter to track the current reference generated by the controller. The desired DC-link and output voltages are tracked with a good transient, as shown in Fig. 14. Fig. 15 displays the voltage and current of L_s in mode 1.

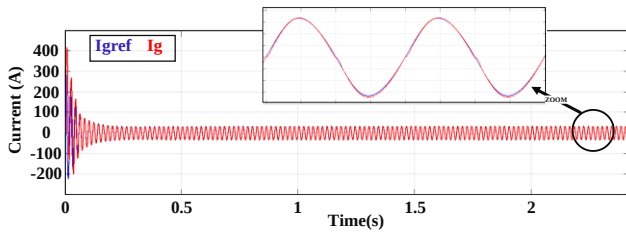


Fig. 13. The measured and reference input current in mode 1

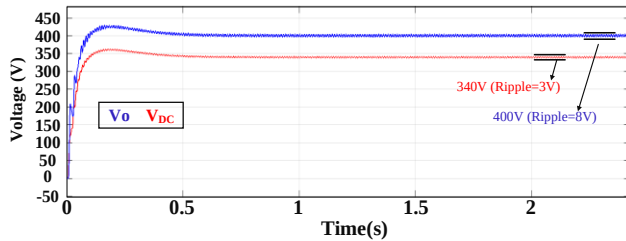


Fig. 14. The DC-link voltage and output voltage in mode 1

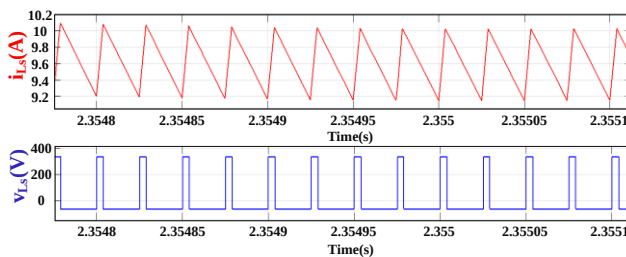


Fig. 15. The voltage and current of L_s in mode 1

The converter's behavior during load changing in mode 1 is illustrated in Figs. 16 and 17. The output power is increased in three steps (1kW, 2kW, and 5kW) at $t=1$ and 2s. The current rise due to load increase is shown in Fig. 16(a). As shown in Fig. 16(b), at all loads, the PF is more than 0.99 with the sinusoidal input current.

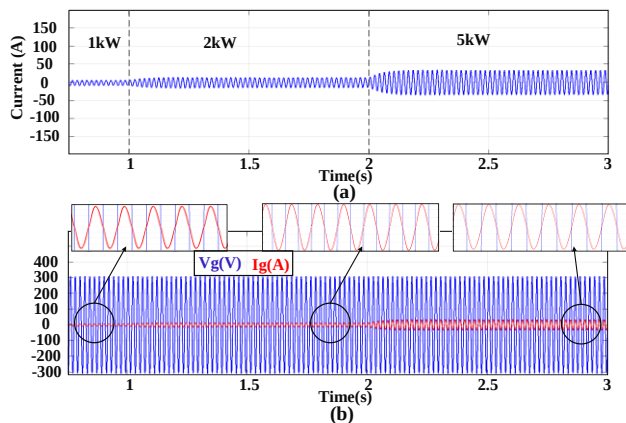


Fig. 16. (a) The input current and (b) grid voltage and input current during load changing in mode1

Transient and steady-state of DC-link voltage and output voltage are shown in Fig. 17. The steady-state of DC-link and output voltages are fixed on their set point (340V and 400V,

respectively), which shows the robustness of the adopted control method.

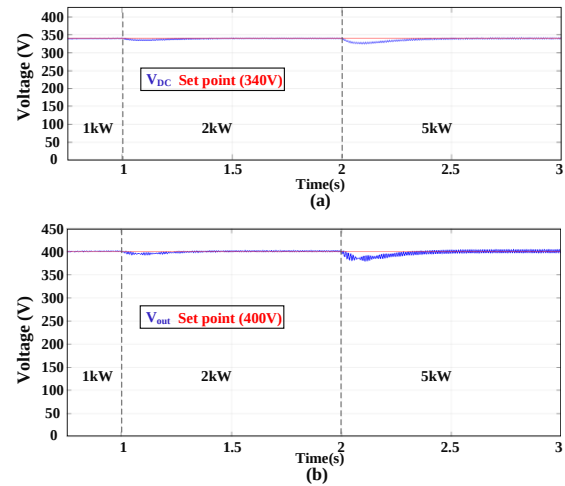


Fig. 17. (a) DC-link and (b) output voltages during load changing in mode1

The second operating mode (G2VH) is also simulated, and the results are provided. Fig. 18 displays the grid voltage and input current of the converter in mode 2 and also the converter's capability of correcting the power factor. As illustrated in Fig. 19, the THD of the input current is 4.09%. The operation of the converter in this mode is divided into three states. The voltage and current of L_s in different states are shown in Fig. 20. The transient and steady-state of V_{DC} and V_o are depicted in Fig. 21. The output voltage ripple is less than 1.5%.

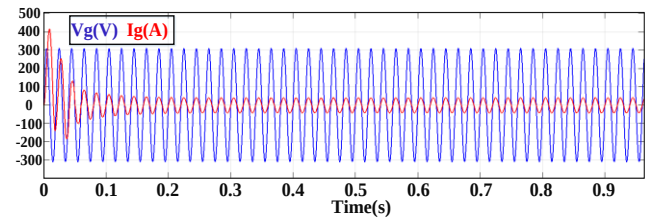


Fig. 18. The grid voltage and input current in mode 2

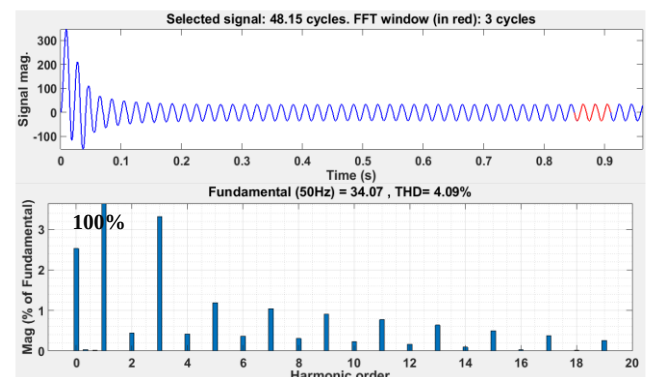


Fig. 19. The FFT analysis of the input current in mode 2

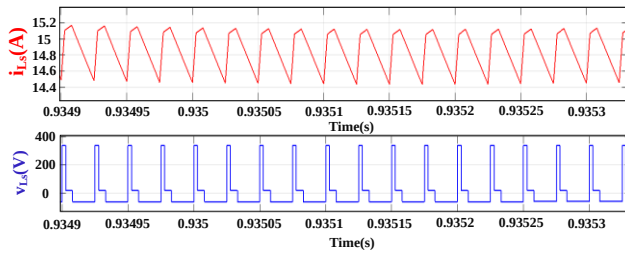


Fig. 20. The voltage and current of L_s in mode 2

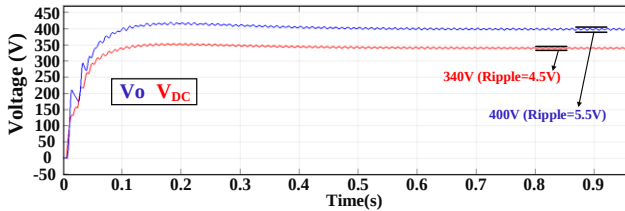


Fig. 21. The DC-link voltage and output voltage in mode 2

The behavior of the converter during load changing in mode2 is also analyzed and results are shown in Fig. 22.

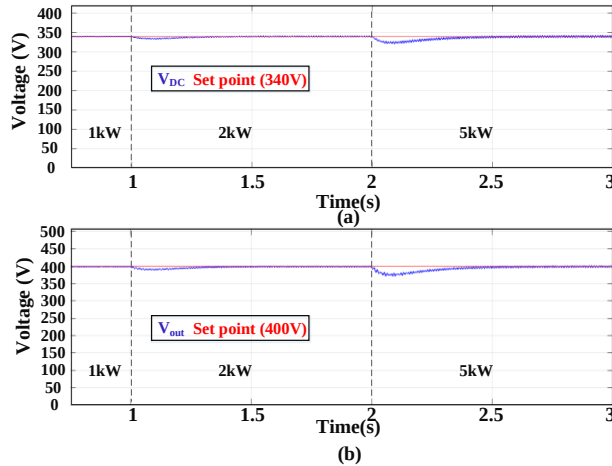


Fig. 22. The DC-link and output voltages during load changing in mode 2

The proposed converter is simulated with real components (considering ON-state resistance and forward voltages for diodes and switches and resistance for inductor) during mode2 and its efficiency is measured as illustrated in Fig. 23.

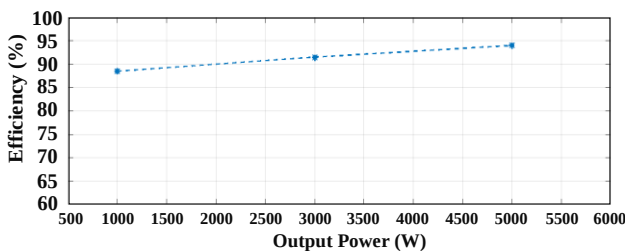


Fig. 23. The converter efficiency in mode 2

The primary stage does not have any task in mode 3. In this mode, the battery provides the energy needed by the DC load. Fig. 24 shows the output voltage in mode 3. As can be seen, the output voltage has an acceptable ripple.

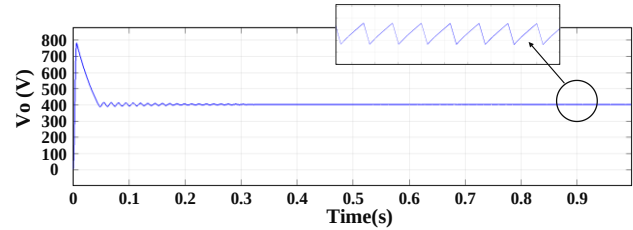


Fig. 24. The output voltage in mode 3

The results of the mode 4 simulation are provided in Figs. 25-27. Fig. 25 shows the switching pattern of $S_{P1} \sim S_{P4}$. S_{P1} and S_{P2} have a high-frequency operation, and S_{P3} and S_{P4} operate with grid frequency. Figs. 26 and 27 illustrate the input current waveform and its FFT analysis, respectively.

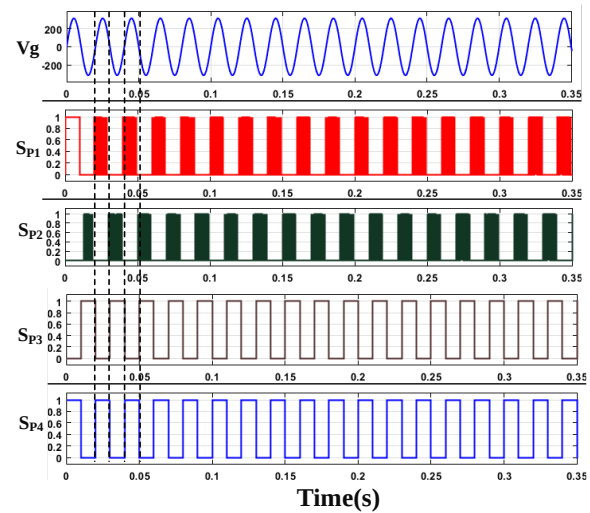


Fig. 25. The gate pulses of $S_{P1} \sim S_{P4}$ in mode 4

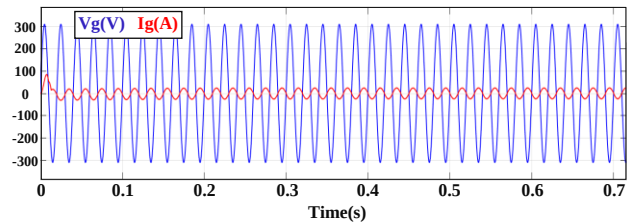


Fig. 26. The grid voltage and input current in mode 4

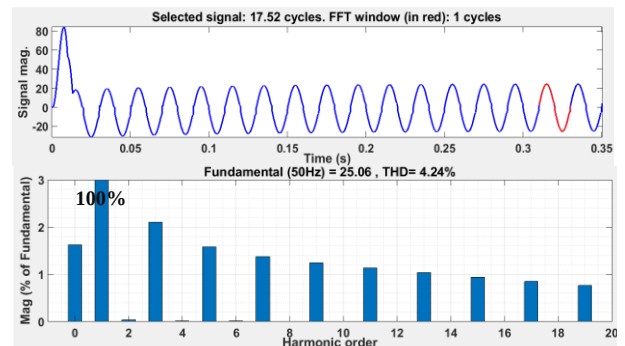


Fig. 27. The FFT analysis of input current in mode 4

VI. EXPERIMENTAL VERIFICATION

To confirm the simulation results, an experimental prototype has been built and tested. The reduced-scale experimental setup is shown in Fig. 28 and its specifications are tabulated in Table 3.

The grid voltage and input current are shown in Fig. 29(a) in the unity PF condition. The gate pulses of the primary stage switches (S_{P1} and S_{P2}) generated with the controller (STM32F103RET) are depicted in Fig. 29(b)-(c). The converter is tested in mode 1 under buck and boost conditions and the DC-link and output voltages are shown in Figs. 29(d) and 29(e), respectively. Fig. 29(f) shows the voltage across L_S in mode 1 boost condition.

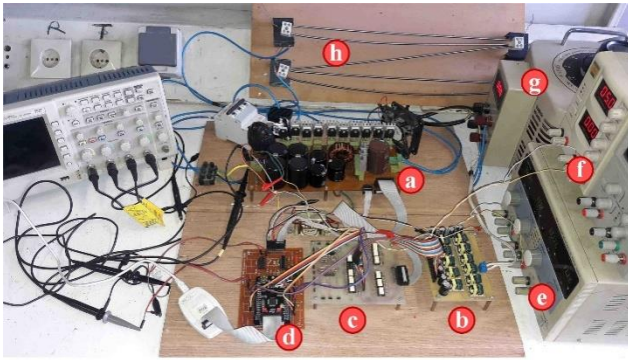


Fig. 28. The implemented overall system composed of (a) power circuit, (b) isolated gate drive supply, (c) gate drive board, (d) controller board, (e) supply of op-amps, (f) supply of ACS712, (g) autotransformer, and (h) load

The proposed converter is simulated in the unity power condition in mode 1. The results are presented in Figs. 9-15. Fig. 9 shows the grid voltage (V_g) and input current (I_g) in the UPF condition. The FFT analysis in three cycles of the input current is shown in Fig. 10, which illustrates the THD value as 3.47% with acceptable harmonic orders. Figs. 11 and 12 are related to the control unit operation in either mode 1 or mode 2. Fig. 11 shows the current loop PID output compared with a 30 kHz triangular wave. The S_{P1} and S_{P2} gate pulses are depicted in Fig. 12. As aforementioned, S_{P1} and S_{P2} have a high-frequency operation in a negative and positive half cycle of the grid voltage, respectively.

The converter is tested in mode 2 and the DC-link, battery port, and output voltages are depicted in Fig. 30(a). Fig. 30(b) shows the voltage of L_S in this mode.

Fig. 31(a) shows the battery port and output voltages in mode3. The converter is also tested in mode 4, and the grid voltage and input current of the converter are shown in Fig.31(b).

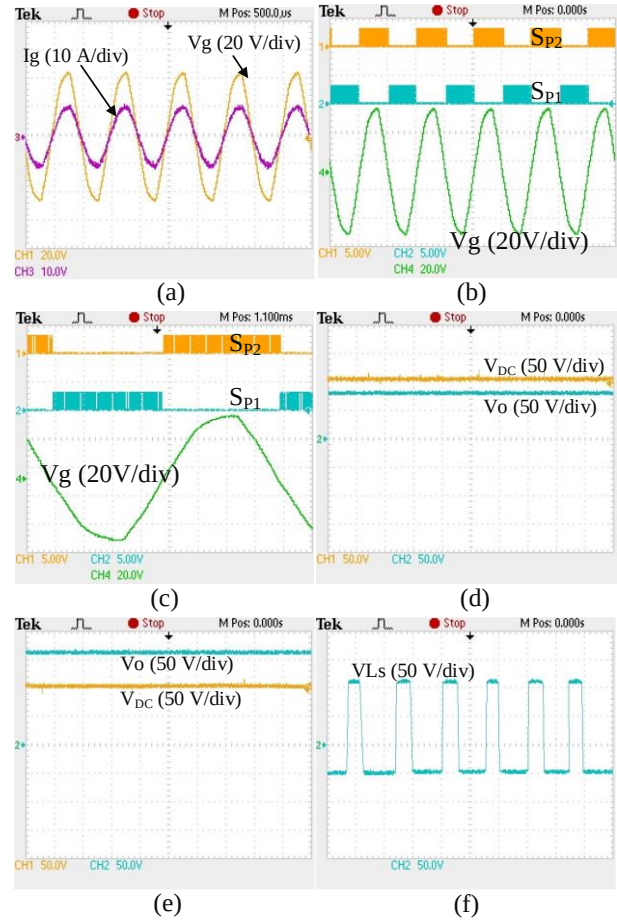


Fig.29. Experimental results of mode1

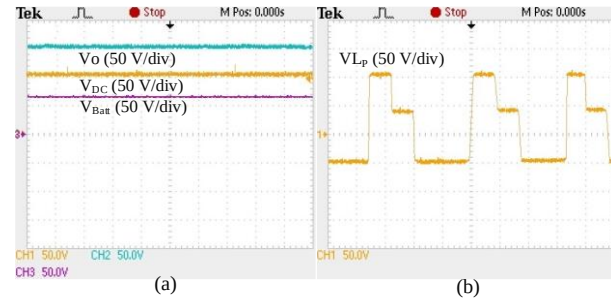


Fig. 30. The experimental results for mode 2

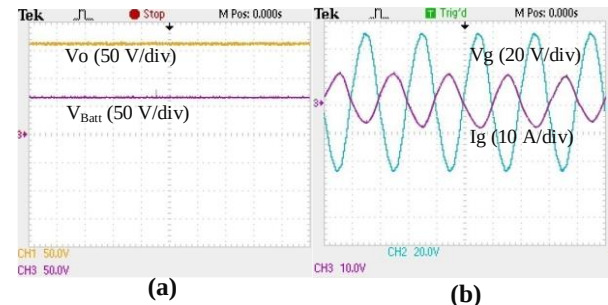


Fig. 31. (a) Battery voltage and output voltage in mode 3, and (b) grid voltage and input current in mode4

VII. CONCLUSION

A novel bidirectional multiport rectifier has been presented in this paper. The proposed converter can be used as a wall-box converter that can be installed in the parking lot of smart buildings and can provide DC-link for local DC loads, such as DC home appliances and charge the connected EV, simultaneously. The ability to work in four operating modes (G2H, G2VH, V2H, and V2G) is the main feature of this converter. A control method is also explained that enables the proposed converter to control active and reactive power according to the processed smart grid or customer commands. The operation of the presented converter is explained and analyzed during all operating modes, and simulation is done to validate system analysis. A reduced-scale experimental setup has been built, and the performance of this converter has been assessed through an experimental test. The results confirm the simulation ones.

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