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A new mismatch cancelation for quadrature delta-sigma modulators

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ABSTRACT

This paper proposes a new mismatch cancelation technique for quadrature delta-sigma modulators (QDSM). In this approach, a high speed and simple structure dynamic element matching (DEM) based on homogenization and time-division (HTD) is designed. In addition, I and Q digital-to-analog converters (DACs) are merged into one complex DAC (C_DAC) for quadrature mismatch cancelation which leads to near-perfect I/Q balance. A third-order multi-bit continuous-time (CT) QDSM for a WCDMA LOW-IF receiver is designed and implemented in 180 nm CMOS technology to investigate the effects of the proposed DEM. The proposed DEM method and DWA algorithm are applied to the QDSM with 2% mismatch errors in DAC cells and compared two outputs PSD effects. Simulation results show that the modulator achieves a signal-to-noise ratio (SNR) of 74 dB and 74.2 dB for the proposed method and DWA, respectively, while the proposed method is simpler and faster than the data weighted averaging (DWA) algorithm.

Article Info

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I. INTRODUCTION

Delta-sigma converters have been promoted to use in radio receivers due to quantization noise shaping and higher accuracy than other types of converters [1, 2]. At a medium data rate, the QDSM is a suitable candidate to implement an analog-to-digital converter (ADC) for a LOW-IF receiver [3, 4]. To increase the SNR and reduce the Jitter sensitivity, a multi-bit quantizer is employed in modulators. The main drawbacks of multi-bit modulators are mismatching error DAC cells and mismatch error between I and Q DACs in the modulator feedback. These errors are affected by the signal back (Feedback) and directly added to the input signal and cause non-linear effects on the total modulator output. This process reduces the SNR, SFDR and other quality characteristics of the modulator. As shown in Figure 1, the most popular method to reduce the effects of these mismatches is to use DEM methods [5, 6].

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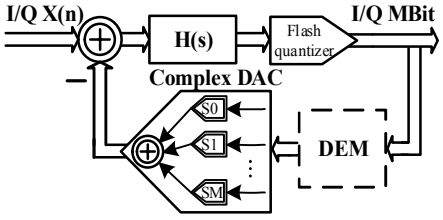

Fig.1. A CT_QDSM structure with DEM.

Various mismatch shaping techniques have been presented in the literature, some of which are reviewed here [7-9].
A low-complexity and efficient digital control for implementing the data weighted averaging (DWA) algorithm is proposed in [8] and a low-complexity, high-speed implementation for the DWA algorithm is proposed in [9]. The effects of non-linear error in the delta-sigma modulator DAC output and a shortened-TDEM (tree-structure DEM) algorithm were presented in [10]. The merging of the first and second layers in tree-structure, hardware-efficiency has resulted in even better than the conventional TDEM. A second-order multi-bit QDSM with a quadrature mismatch scrambler (QMS) is designed in [4]. In this DEM algorithm, two techniques were combined, i.e. incremental data weighted averaging (IDWA) in the first layer and data-directed scrambler (DDS) in the

second layer. A higher-order band-pass (BP) DWA algorithm based on simple pointer calculations which minimize the delay caused by mismatch calibration in the loop has been suggested in [9]. This algorithm and DAC have required a 3x higher clock frequency compared to the modulator. In [11], a DWA algorithm has been implemented in a new method and its pointer has been randomly added. The SNR and SFDR have been grown and the tones have been eased.

The DEM algorithms are implemented by digital circuits. These circuits are usually complex and impose a delay to the modulator loop (due to low speed), decreasing the modulator stability [8, 12-14].

The stability of modulators has been decreased in previous works because of delays and complexities of DEM structures. This paper presents a new method with high speed and simple structure to mismatch error cancelation. In this method, the quantizer output is homogenized by the first swapper layer. Then, every bit is divided into four parts timeshare in parallel slice with ¼ delay period at time-division part. Finally, each quadruple slice group is applied to four complex DAC cells. To evaluate the effectiveness of the proposed DEM, this method is compared with a DWA algorithm that is one of the popular DEM methods [15]. The effectiveness of the high-speed and simple-structure proposed method is comparable with the DWA algorithm. This article is organized as follows: mismatch error analyses are presented in Section 2 and the proposed DEM method is described in Section 3. The DWA algorithm has been implemented in Section 4. The modulator structure and implementation are described in Section 5. Simulation results with 2% mismatch error for DWA and HTD DEM are presented in Section 6 and finally, conclusions are given in Section 7.

II. Mismatch Error Analyses

The effects of nonlinear error in the M bit delta-sigma modulator DAC output can be written as Eq. (1) [10].

$$DAC_{error} = \frac{\pi^2}{3*OSR^3} \cdot \frac{\sigma_\alpha^2 \left(1-\frac{1}{M}\right)^2 M}{12} \qquad (1)$$

where σ^2_α is the variance of mismatch error. In general, non-ideal errors in the DAC are of two types: static and dynamic errors. A real model of DAC cell is shown in Figure2.

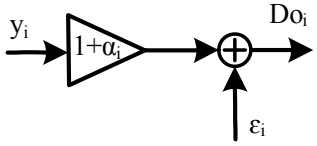

Fig. 2. A real DAC cell model.

The conversion function for each cell can be applied to as Eq. (2).

$$Do_i(n) = [1+\alpha_i]SV_i(n) + \varepsilon_i \qquad (2)$$
$$\alpha_i = eh_i - el_i \quad and \quad \varepsilon_i = el_i$$

where SVi and Doi are the input and output of ith DAC cell, respectively, and ehi and eli are the mismatch error pulses caused by the component mismatches for two different DAC states (on and off). Similarly, for a DAC with M cells, it is calculated as follows:

$$Do_i = Y(n) + e(n) + \varepsilon$$
$$e(n) = \sum_{i=0}^{M} \alpha_i SV_i(n) \quad and \quad \varepsilon = \sum_{i=0}^{M} \varepsilon_i \qquad (3)$$

As specified by Eq. (3), the output of each cell is equal to the amount of input, mismatch error (e (n)), and offset error (ε). The offset error is not important in most cases and cannot be corrected by using DEM. But, the main limitation of the multi-bit modulator DAC cells is the error of mismatch directly added by the input signal and non-linear effects in output and reduces SNR and SFDR and other quality factors of the modulator [16].

III. Proposed DEM Method (Quadrature Mismatch Cancelation)

The DEM algorithms are useful to mismatch error cancelation, but they are only applied to single I and Q DAC paths [17]. In [18], with I/Q paths and DACs multiplexing technique, the aliasing of image interference and DAC mismatch are canceled. But, it only operates in discrete-time (DT) quadrature modulators. The proposed complex DEM is shaped both of DAC mismatches error cells and mismatch between I and Q DACs. This approach is done in two steps; the first step is the homogeneous section with a time-division DEM (HTD_DEM) to cancel DAC mismatch cells and the second is complex DAC designed to cancel mismatch error between I and Q paths.

A. The HTD_DEM structure

The quantizer output comes in the so-called thermometric code. Like a mercury thermometer, a certain comparator can only output a high bit if all comparators below are high, too. In this regard, the probabilities of lower (first) bits being one are more than the higher bits, as shown in Fig 3.

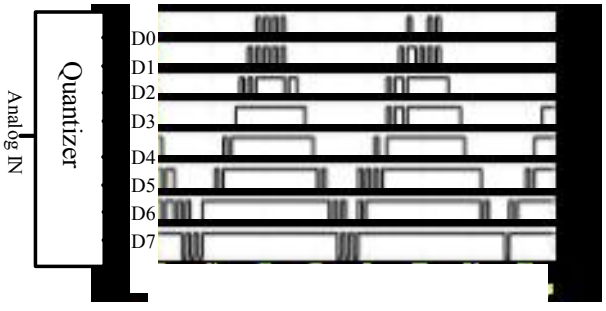

Fig. 3. One and zero distribution at quantizer's outputs.

Like any other DAC, the problem in this DAC architecture

combined with the thermometric quantizer output is that a mismatch in the cells leads to a systematic error of the D/A conversion.

To solve this problem, a new DEM method is proposed. In this method, each top and down pair of bits is applied to the one swapper in swapper block 1 (homogenization) and is replaced in the decussate period, according to Fig. 4. Then, the outputs of the homogeneous swapper are distributed between two time-division (TD) parts in the second layer.

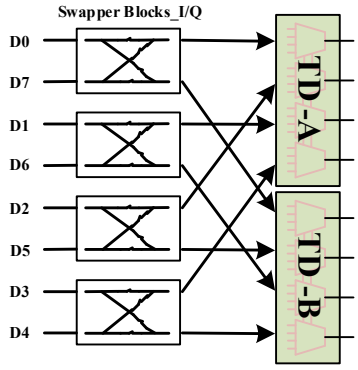

Fig. 4. Homogeneous section (swapper block1) with TD blocks.

The distribution of ones and zeros at the output of swapper block 1 are shown in Fig. 5. This output is applied to the TD block.

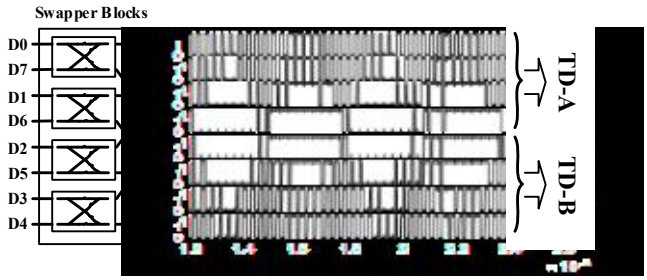

Fig. 5. One and zero distribution at swapper's (homogenization) outputs.

The TD block and an example of bit's TD are shown in Fig. 6. The outputs of the homogenization section in quadruple groups are applied to the TD block. Four multiplexers (in each TD block) are used to divide the time for each quadruple group of data (in the proposed modulator, this task is done by eight multiplexers (2x4)). At this stage, every bit is divided into four slices by timeshared so that each slice will be given to output in quarter cycles. Thus, each quadruple group of the binary input bits is converted into four parallel slices in that each slice has a ¼ cycle delay relative to previous quarter cycle. Finally, the TD block output is applied to a complex DAC (C_DAC).

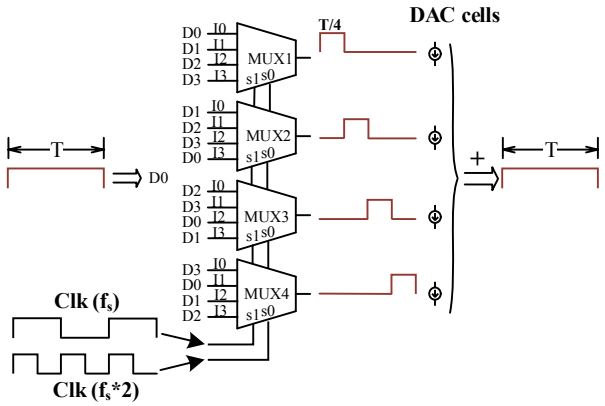

Fig. 6. TD-A (TD-B) block diagram with an example (D0) of bit's time division.

B. Implementation of complex DAC and swapper cells

The proposed HTD_DEM architecture with C_DAC is shown in Fig 7. The I/Q DAC mismatch error cells are canceled with HTD_DEM, as described in the previous section. The mismatch errors between I and Q are alleviated by C_DAC. This block consists of two sections; swapper block 2 and complex DAC cells [4, 14]. This block adopts out of the gain error averaged between I and Q feedback DACs.

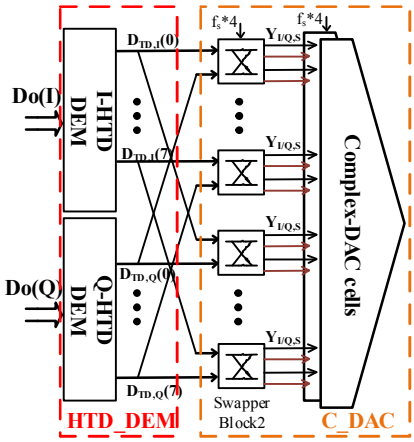

Fig. 7. The proposed HTD_DEM architecture with C_DAC.

The I/Q C_DAC unit selection signals are generated by the selection rule defined in (4). When ($Y_{I,TD}, Y_{Q,TD}$) = (0,0) or (1,1), I-DAC current will be diverted to the Q-path, and Q-DAC current flows to the integrators in I-path. When ($Y_{I,TD}, Y_{Q,TD}$) = (1,0) or (0,1), I-DAC and Q-DAC remain at their original I-path and Q-path.

$$Y_{I/Q,C\_DAC}\begin{cases} If\,(Y_{I,TD,n}[n]+jY_{Q,TD,n}[n])=(0+j0)\Rightarrow Y_{I,S}=Y_{Q,TD}\ and\ Y_{Q,S}=Y_{I,TD} \\ If\,(Y_{I,TD,n}[n]+jY_{Q,TD,n}[n])=(1+j0)\Rightarrow Y_{I,S}=Y_{I,TD}\ and\ Y_{Q,S}=Y_{Q,TD} \\ If\,(Y_{I,TD,n}[n]+jY_{Q,TD,n}[n])=(0+j1)\Rightarrow Y_{I,S}=Y_{I,TD}\ and\ Y_{Q,S}=Y_{Q,TD} \\ If\,(Y_{I,TD,n}[n]+jY_{Q,TD,n}[n])=(1+j1)\Rightarrow Y_{I,S}=Y_{Q,TD}\ and\ Y_{Q,S}=Y_{I,TD} \end{cases} \quad (4)$$

The C_DAC is of NRZ type consisting of 16 DAC units and

realized with the current-steering topology. Fig. 8 depicts a simplified schematic of each C_DAC unit and swapper cell. A swapper cell consists of four AND gates and flip flops. Each C_DAC cell is composed of four switches and a current tail. Each cell is switched according to the input values (DTD_I /D TD_Q) and determines the direction of the current tail based on Table 1. Therefore, the mismatch error between I and Q DACs is swapped dynamically. As a result, the mismatch error between I and Q DACs are greatly reduced and then SNR is considerably better.

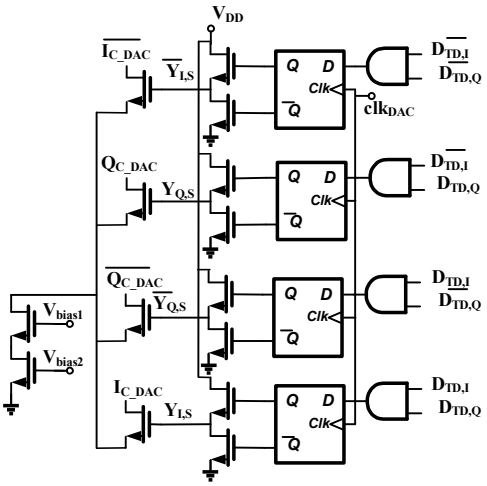

Fig. 8. The current steering C_DAC unit with a swapper cell.

TABLE I.
THE DIRECTION OF THE CURRENT TAIL

D_I	D_Q	Y_{I,C_DAC}	Y_{Q,C_DAC}
0	0	$\overline{Y_I}$	$\overline{Y_Q}$
0	1	$\overline{Y_I}$	Y_Q
1	1	Y_I	Y_Q
1	0	Y_I	$\overline{Y_Q}$

The interface of the complex I/Q DAC (which consists of 16 DAC units) and the integration input are depicted in Fig. 9. The output of HTD_DEM is rotated in complex DAC cells.

IV. IMPLEMENTATION OF DWA STRUCTURE

To clarify the effect of the proposed DEM (HTD_DEM), this method is compared with a DWA algorithm. The DWA algorithm is one of the most widely used methods and displays the best performance with respect to other first-order mismatch error shaping DEM methods[8]. This algorithm eliminates the DAC cells mismatch errors as well as a high-pass filter [19].

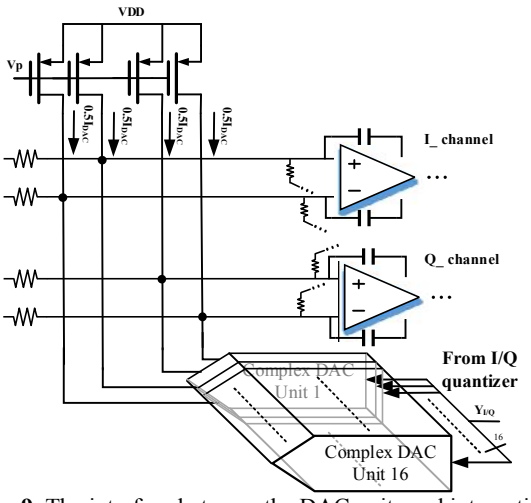

Fig. 9. The interface between the DAC units and integration input.

This algorithm uses a pointer (ptr (n)) to specify the starting point of a period with respect to the previous period and increases the amount of input code with each clock. How to select the elements depends on the amount of input so that the input of DAC is selected for a successive round (consecutive). The block diagram of the DWA logic is shown in Figure 10. The outputs of an eight-bit thermometer quantizer are applied to the DWA logic. The thermometer code is converted to binary, then a 3-bit adder and a 3-bit register produce two indexes which are converted into two sets of 8-bit thermometer codes by two binary-to-thermometer decoders. When the carry signal of the adder is low, the output control signals are the mutual XOR of the two 8-bit thermometer codes. When the carry signal is high, the control signals are the mutual XNOR of the two 8-bit codes. The DWA algorithm selects DAC cells cyclically one by one. No cell is reselected before all the others are selected. The DWA algorithm converts the quantizer output code to eight control signals for the element selection of the 8-cell DAC.

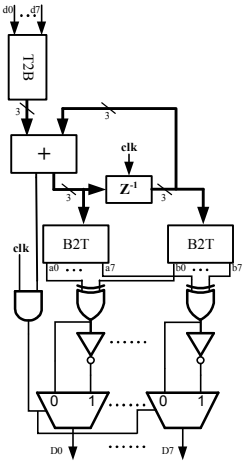

Fig. 10. The block diagram for the DWA realization.

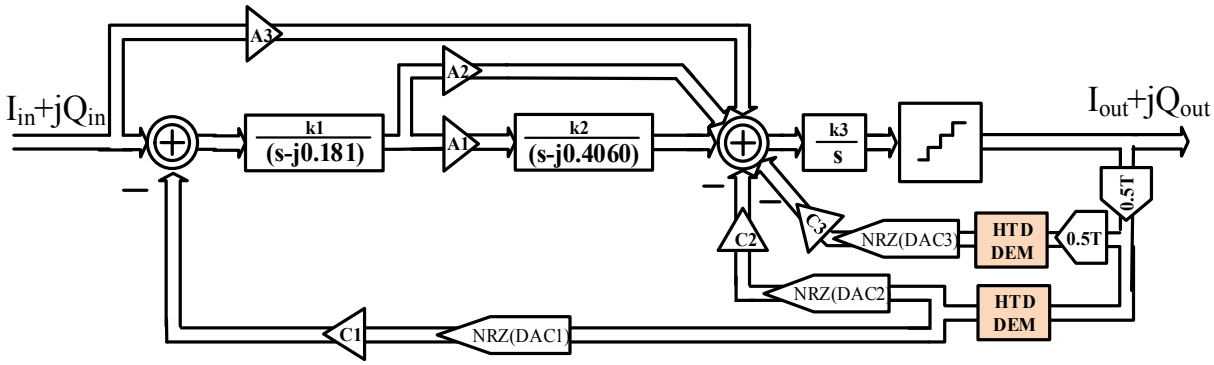

Fig. 11. System level block diagram of the QDSM

V. MODULATOR STRUCTURE

The proposed modulator is designed in feed-forward (FF) topology. The major advantage of the FF topology is that the integrator outputs do not contain a significant part of the input signal as compared with the feedback architecture. Thus, the necessity for scaling and also the requirements on integrator dynamics are much more relaxed [20]. In the FF structures, the signal amplitude is small at the integrator output and the modulator sensitivity to the non-linearity of the integrator is decreased [21]. In the proposed modulator, the adders are eliminated to optimize power consumption [22]. The loop filter transfer function (H(s)) of the modulator is shown as Eq. (5).

$$H(s)=\frac{0.4576+(1.3958+j0.1786)(s-j0.183)+2.0537s(s-j0.183)}{s(s-j0.087)(s-j0.183)} \quad (5)$$
$$+0.862$$

The block diagram of the proposed modulator is shown in Fig. 11. The adders of the modulator are removed to compensate for the excess loop delay. The excess loop delay is set to half of the sampling period of quantizer [23]. In the modulator structure, in addition to the main DAC1, two other DACs (DAC2, DAC3) are added to the modulator to compensate for the delay loop and eliminated adders. The quadrature modulator structure with three bit quantizer and DAC cells is implemented for WCDMA standard with the specifications of OSR 32, sampling frequency 64MHz and bandwidth 2MHz. The modulator integrators are implemented with active RC due to the high linearity. The circuit of the proposed modulator is shown in Fig. 12.

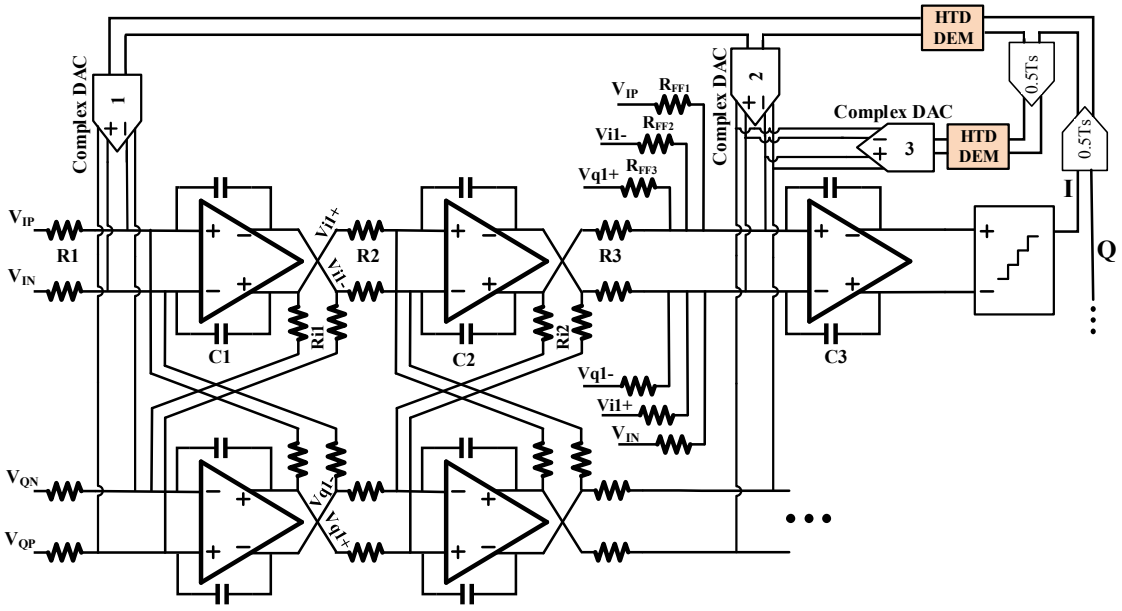

Fig. 12. A simplified circuit of the proposed modulator.

The first-stage integrator is a telescopic op-amp that has low power and large bandwidth. The swing problem of this op-amp

has solved by the use of high swing current mirror as a load [24]. A folded cascade op-amp whose input and output common mode range can be adjusted independently from each other [25, 26] is used in the second stage. The most important feature of this op-amp is on the third stage which serves as a collector for feed-forward paths. The telescopic op-amp has been used again because of its low power advantages. The I/Q path has three NRZ DACs that are implemented using the current string method. A 3-bit flash quantizer consisting of eight comparators is implemented in the modulator [27].
The modulator output PSD is shown in Fig. 13 with the SNR of 75.9 dB.

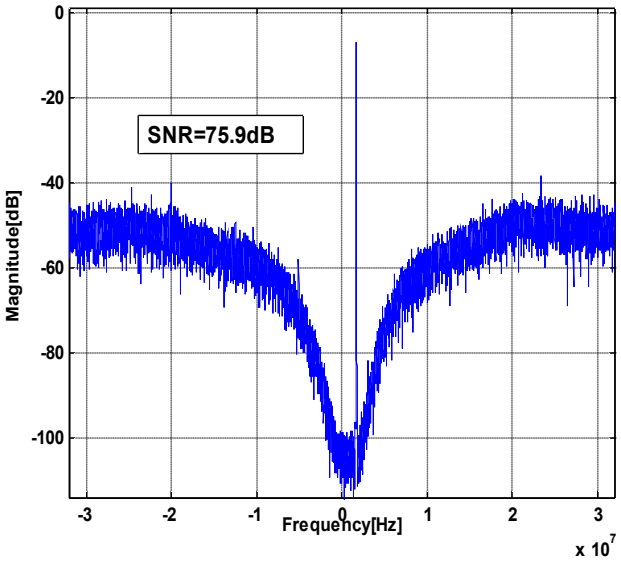

Fig. 13. The output PSD of the proposed modulator with an ideal DAC without DEM.

X. Simulation Results

The proposed DEM method (HTD_DEM) and DWA algorithm are applied to the modulator and the output PSD effects are compared. The output PSD of the QDSM at four states of ideal, 2% mismatch error, HTD_DEM ON and DWA on are shown in Figs. 14-17. The SNR of ideal is about 12dB more than the 2% mismatch errors condition. The SNR of HTD_DEM is almost as great as the DWA algorithm and 2 dB less than the ideal DACs.

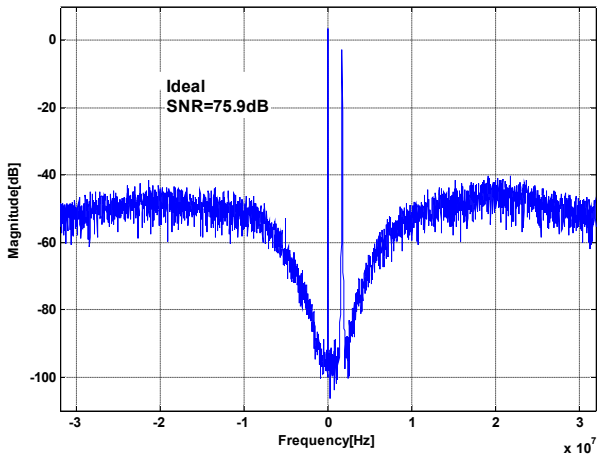

Fig. 14. The simulated output spectra of the modulator with ideal DAC cells.

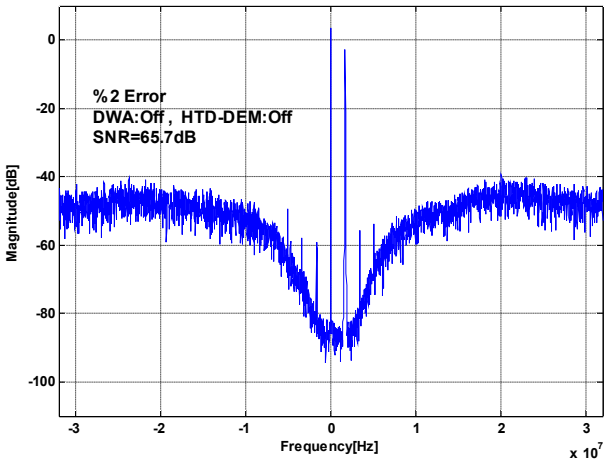

Fig. 15. The simulated output spectra of the modulator with 2% mismatch in DAC cells and DEM blocks are off.

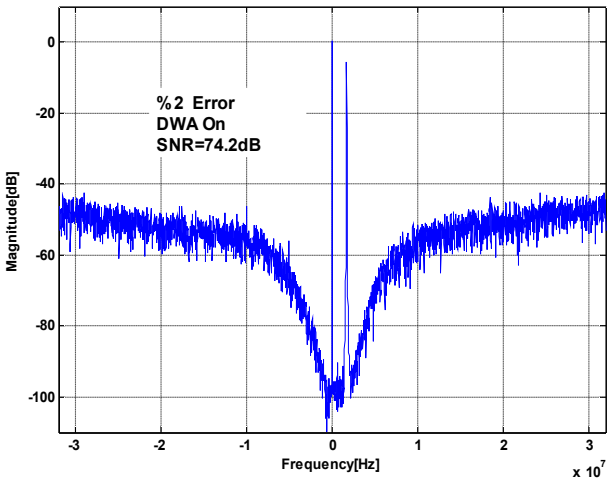

Fig. 16. The simulated output spectra of the modulator with 2% mismatch DAC cells; DWA block is on.

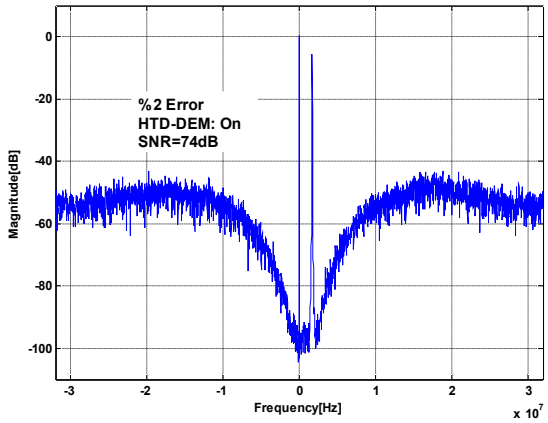

Fig. 17. The simulated output spectra of the modulator with 2% mismatch DAC cells; HTD_DEM block is on.

The comparison of SNR and DAC errors under four conditions of the modulator is shown in Fig. 18. This figure plots the simulated SNR versus the input amplitude under 2 MHz signal bandwidth. The efficiency of the mismatch coefficient of the DAC cells in different DEM algorithms is indicated in these curves.

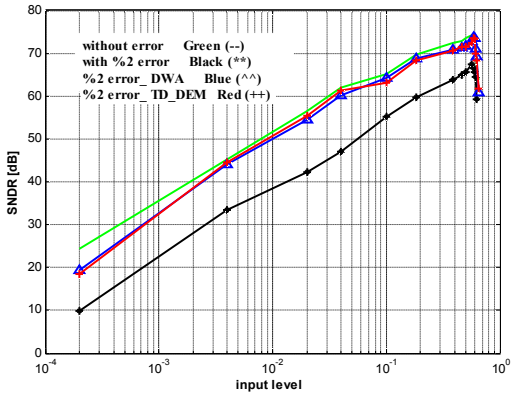

Fig. 18. The comparison of the simulated SNR versus input.amplitude by DAC errors under four conditions of the modulator.

The simulated performance of the modulator in various states of DAC (ideal, 2% mismatches) and DEM (DWA-DEM on, HTD-DEM on) is summarized in Table 2. These results confirm the favorable performance of the proposed structure HTD-DEM so that they are comparable to the DWA-DEM system. The performance comparisons with other literatures are shown in Table 3. The FOM of this work is best compared with other references except [22]. This difference is related to the fact that this work has DEM block with 2% mismatch error in DACs while [22] has an ideal DAC without DEM block.

TABLE II.
A SUMMARY OF THE SIMULATED SNR IN VARIOUS STATES OF DAC.

DAC condition	Max SNR (dB)
ideal	75.9
2% mismatch	65.7
DWA-DEM ON	74.2
HTD-DEM ON	74

XI. CONCLUSIONS

A new complex mismatch error cancelation for the implementation in QDSM is proposed in this paper. This structure includes two sections: HTD-DEM to I and Q DACs cells mismatch error cancelation and C_DAC to complex mismatch error cancelation. A third-order multi-bit QDSM with 2 MHz bandwidth is designed for WCDMA standard to investigate the effects of the proposed DEM. The proposed method (HTD-DEM) and DWA algorithm are applied to the designed modulator with 2% mismatch error in DAC cells and then it is compared to two output PSD effects. The effectiveness in mismatch error correction of the proposed method with the high speed and simple structure is in the range of popular DWA technique mismatch error correction.

TABLE III.
PERFORMANCE COMPARISON WITH OTHER LITERATURES.

Parameter	type	SNR (dB)	Bandwidth (MHz)	OSR	Power (mW)	FOM [28] (pj/conv)*	Technology (μm)
[28]	QFF3/CT	58.6	1	32	1.7	1.22	0.13
[29]	QFF3/CT	50.4	1.5	24	2	1.6	0.13
[30]	QFF3/CT	65.2	0.5	192	2.3	1.58	0.13
[22]	QFF3/CT	75.9	2	32	6.91	0.339	0.18
[31]	QFF3/CT	74.2	2	32	8.3	0.495	0.18
This work	QFF3/CT	74	2	32	7.15	0.436	0.18

$$* \quad \text{FOM} = \frac{\text{power}}{2*\text{BW}*2^{((\text{SNDR}-1.76)/6.02)}}$$

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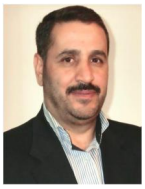

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