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A New Multilevel Inverter Topology with Component Count Reduction

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ABSTRACT

As a major component of electrical systems, multilevel inverters have been discussed extensively over the past decade. Nowadays, the improvement of their performance is one of the important challenges that has brought about many studies on their topology and control system. This paper proposes a new topology of symmetrical multi-level inverters that is able to feed inductive, resistive and capacitive loads. The proposed topology has fewer power elements including IGBTs, driver circuits, diodes, and DC voltage sources. To increase the number of output voltage levels, several basic topologies can be used in a cascaded structure. The comparison of the proposed converter with some previous topologies shows its better conditions in terms of the used semiconductor count, switching and conduction losses, and total blocking voltage. The operation and performance of the proposed multi-level inverter are ascertained by simulations and are verified experimentally for a 9-level inverter, showing the capability of the proposed converter in smooth sinusoidal output voltage generation with a minimum total harmonic distortion.

Article Info

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I. Introduction

DC to AC converters, that called inverters, are one of the key components of electrical systems that have many applications, such as reactive power compensators, adjustable speed drives, uninterruptible power supplies, High voltage DC transmissions and electric vehicles [1-11]. Conventional inverters produce square-wave output with two positive and negative voltage levels [12, 13]. The switching voltages across power switches, and dv/dt stresses of the mentioned topologies are considerable. In order to overcome the mentioned problems of conventional converters, multi-level inverters with more than three levels at the output voltage have been introduced. Multilevel inverters have many benefits such as high power quality, lower harmonics, better electromagnetic characteristics and lower switching losses [14-17]. Classical multi-level inverters are divided into three topologies: Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascade H-bridge (CHB) [18-22].

The quality of a multi-level inverter specifies by its number of output levels. Although increasing the number of output levels leads to an increase in the number of semiconductor devices and increases the complexity of controlling and operating of the inverters, therefore, the number of semiconductor devices must be reduced [23-25].

Multi-level cascaded inverters are made up of a series connection of multiple single-phase inverters [26]. The Cascaded multilevel inverters are divided into two types: If the value of all dc voltage sources is equal, they will be symmetrical inverters and otherwise they called asymmetrical inverters. Many topologies are based on the CHB inverters. Some of them used symmetrical voltage sources and some other used asymmetrical voltage sources to reduce the number of switches [27, 28].

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In this paper, a new topology of the symmetrical multi-level inverters is proposed. To increase the number of output levels, several basic units can be connected in series. The comparison between the proposed converter and some previous topologies shows that it has better conditions with respect to the used semiconductor count, switching and conduction losses, and total blocking voltage. The operation and performance of the proposed multi-level converter have been ascertained through simulations and verified experimentally for a 9-level inverter which shows the proposed converter's ability in smooth sinusoidal output voltage generation with minimum total harmonic distortion.

II. The proposed topology

A. Basic unit

The basic unit of the proposed topology is shown in Fig. 1. This basic structure consists of four switches with higher switching frequency (S1- S4) and four switches with lower-switching frequency (T1-T4) and four symmetrical dc voltage sources. Also, the basic structure consists of two parts: The level generation part and H-bridge part. The desired voltage level is generating by level generation part and the H-bridge changes it to negative or positive one.

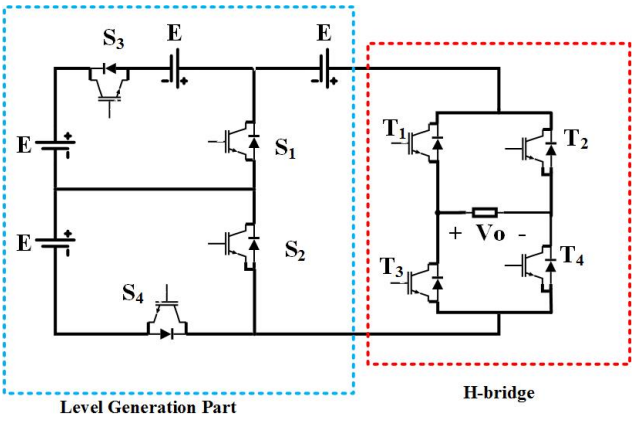

Fig. 1: Basic unit of the proposed topology

Table 1: The output voltage of the basic structure for different switching patterns

State	Switches On	V_O
1	S_3, S_4, T_1, T_4	$4E$
2	S_3, S_2, T_1, T_4	$3E$
3	S_1, S_4, T_1, T_4	$2E$
4	S_1, S_2, T_1, T_4	E
5	T_3, T_4	0
6	S_1, S_2, T_2, T_3	$-E$
7	S_1, S_4, T_2, T_3	$-2E$
8	S_3, S_2, T_2, T_3	$-3E$
9	S_3, S_4, T_2, T_3	$-4E$

Table 1 shows the output voltage of the basic unit for different switching patterns of inverter. As shown in Table 1, this topology is able to produce nine level in output. Also different operating modes of the proposed inverter and current path of each voltage level are shown in Fig.2

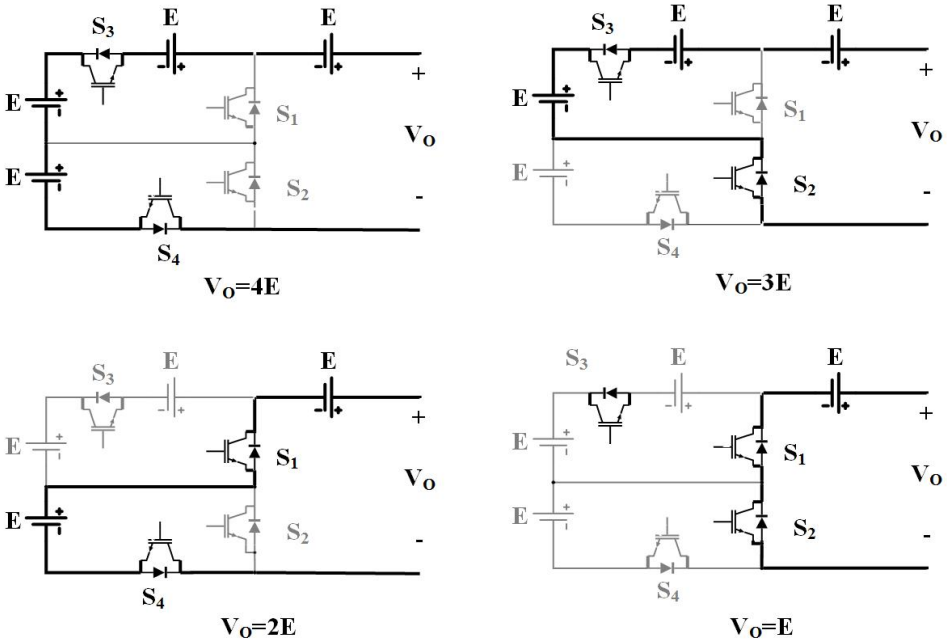

Fig. 2: Different operating modes of proposed inverter

B. *The proposed cascaded topology*

A new cascaded multilevel inverter is obtained from series connection of n number of basic units. The structure of the proposed cascaded multi-level inverter is shown in Fig. 3. According to Fig. 3, the total output voltage of the inverter is obtained from summation of the output voltage of different units, as follows:

$V_{O\_LGP} = V_{o1} + V_{o2} + \cdots + V_{on}$ (1)

Which V_{O_LGP}, V_{oi} are level generation part output voltage and *i-th* cascaded unit output voltage in cascaded topology (see Fig.3). The output voltage of the proposed topology with different switching patterns is given in Table 2. In the proposed cascaded multilevel structure, the number of output levels (N_{level}), the number of IGBTs (N_{IGBT}) and the number of dc voltage sources (N_{source})are obtained from the following equations:

$N_{level} = 6n + 3$ (2)

$N_{IGBT} = 4n + 4$ (3)

$N_{source} = 3n + 1$ (4)

Where n is the number of cascaded stages. Another important parameter in the inverters is the maximum amount of blocked voltage on the switches. By using of the presented methods in [28] for the proposed topology, the value of this parameter for different switches of each stage is obtained from the following equation:

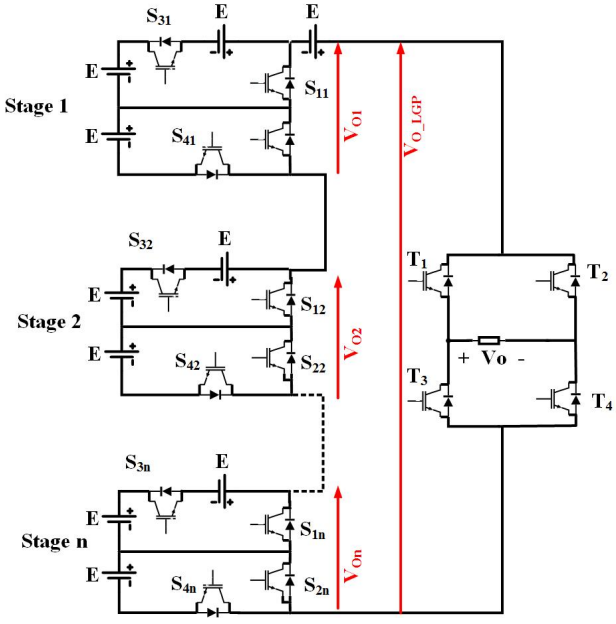

Fig. 3: The proposed cascaded inverter

Table II: The output voltage of the cascaded structure for different switching patterns

Switches On				H-bridge	V_O
Stage1	Stage2	…	Stage n		
S_{31}, S_{41}	S_{32}, S_{42}	…	S_{3n}, S_{4n}	T_1, T_4	$(3n+1)E$
S_{31}, S_{41}	S_{32}, S_{42}	…	S_{3n}, S_{2n}	T_1, T_4	$3nE$
⋮	⋮	⋮	⋮	⋮	⋮
S_{31}, S_{41}	S_{32}, S_{42}	…	S_{1n}, S_{2n}	T_1, T_4	$7E$
S_{31}, S_{41}	S_{32}, S_{22}	…	S_{1n}, S_{2n}	T_1, T_4	$6E$
S_{31}, S_{41}	S_{12}, S_{42}	…	S_{1n}, S_{2n}	T_1, T_4	$5E$
S_{31}, S_{41}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_1, T_4	4E
S_{31}, S_{21}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_1, T_4	$3E$
S_{11}, S_{41}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_1, T_4	$2E$
S_{11}, S_{21}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_1, T_4	E
–	–	…	–	T_3, T_4	0
S_{11}, S_{21}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_2, T_3	$-E$
S_{11}, S_{41}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_2, T_3	$-2E$
S_{31}, S_{21}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_2, T_3	$-3E$
S_{31}, S_{41}	S_{12}, S_{22}	…	S_{1n}, S_{2n}	T_2, T_3	$-4E$
S_{31}, S_{41}	S_{12}, S_{42}	…	S_{1n}, S_{2n}	T_2, T_3	$-5E$
S_{31}, S_{41}	S_{32}, S_{22}	…	S_{1n}, S_{2n}	T_2, T_3	$-6E$
S_{31}, S_{41}	S_{32}, S_{42}	…	S_{1n}, S_{2n}	T_2, T_3	$-7E$
⋮	⋮	⋮	⋮	⋮	⋮
S_{31}, S_{41}	S_{32}, S_{42}	…	S_{3n}, S_{2n}	T_2, T_3	$-3nE$
S_{31}, S_{41}	S_{32}, S_{42}	…	S_{3n}, S_{4n}	T_2, T_3	$-(3n+1)E$

$V_{block_{S_{1i}}} = V_{block_{S_{3i}}} = 2V_{block_{S_{2i}}} = 2V_{block_{S_{4i}}} = 2E$ (5)

There for the blocked voltage of each stage is as follows:

$V_{block_i} = V_{block_{S_{1i}}} + V_{block_{S_{3i}}} + V_{block_{S_{2i}}} + V_{block_{S_{4i}}} = 6E$ (6)

The total amount of blocked voltage in level generation part can calculated by this equation:

$$V_{block_{LGP}} = \sum_{i=1}^{n} V_{block_i} = 6nE \quad (7)$$

Similarly, the blocked voltage on the switches of H-bridge unit calculated as follows:

$V_{block_{T_1}} = V_{block_{T_2}} = V_{block_{T_3}} = V_{block_{T_4}} = V_{O_{max}}$ (8)

Similarly the total amount of blocked voltage in H-bridge can calculated by this equation:

$V_{block_{HB}} = \sum_{j=1}^{4} V_{block_{T_j}} = 4V_{O_{max}} = (12n + 4)E$ (9) .

Therefore, the maximum value of total blocked voltage on the switches in cascaded multi-level inverter is obtained as follows:

$V_{block} = V_{block_{HB}} + V_{block_{LGP}} = (18n + 5)E$ (10)

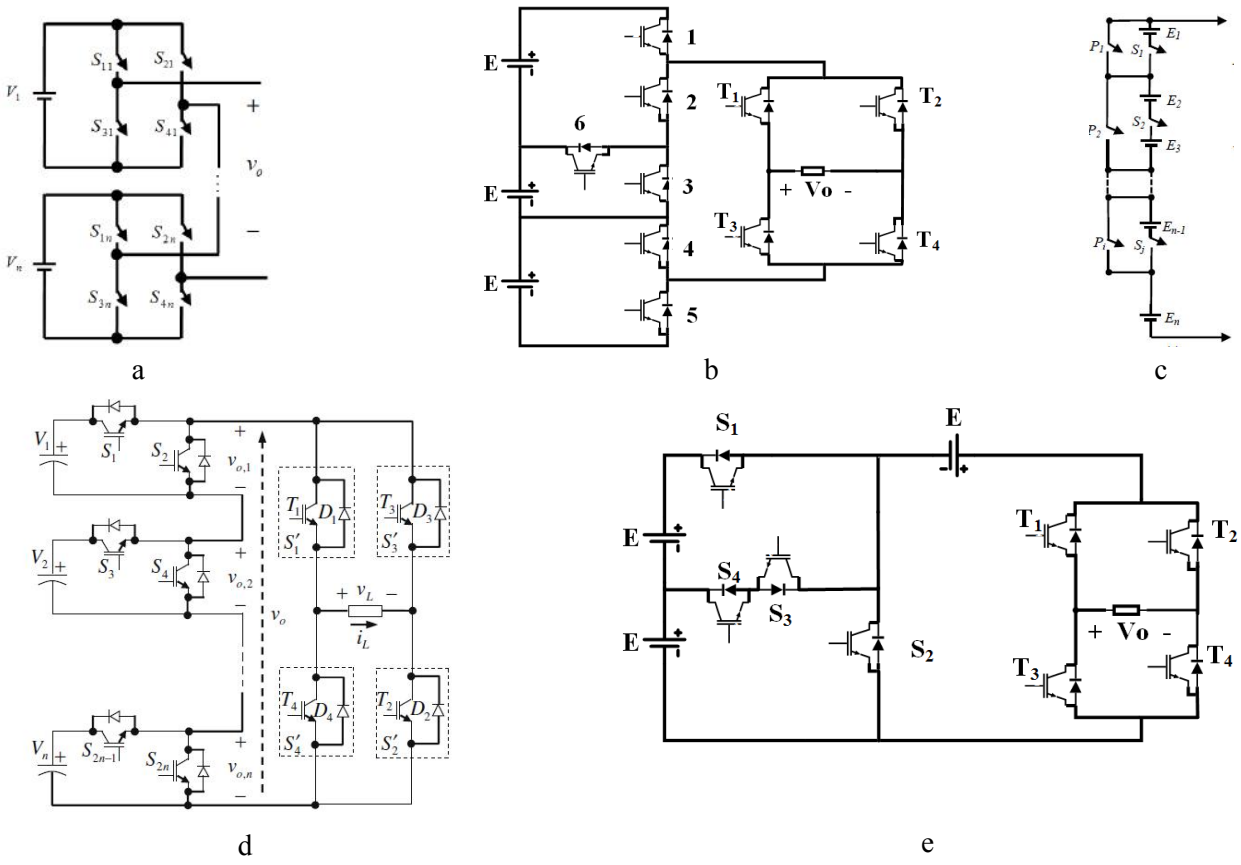

Fig. 4: Symmetrical cascaded multilevel inverters; a) proposed inverter in [29] - (R_1- CHB); b) proposed topology in [30] - (R_2); c) presented topology in [31] - (R_3); d) suggested structure in [32] - (R_4); e) proposed topology in [10]- (R_5)

III. Comparison Of proposed Topology with Conventional Topologies

The main goal of presenting a new inverter topology is to increase the number of output levels by decreasing the number of used elements. To verify the performance of the proposed topology, it is compared with several conventional symmetrical topologies from different points of view, such as the number of IGBTs, the number of dc voltage sources and the amount of the blocked voltage on switches. The topologies that used for this comparison are named by (R_1-R_5). This symmetrical topologies are shown in Fig.4.

Fig.5 compares the number of used voltage sources in each topology. According to this figure, the required dc voltage sources in proposed topology is equal to CHB, R_2, R_4 and R_5 and is less than R_3 to generate same levels in output.

The number of IGBTs and its anti-parallel diodes are the main components of an inverter, which affects the price, size and the complexity of inverter. In Fig. 6, the number of IGBTs for different topologies are compared. As it is clear, the proposed topology requires fewer IGBTs. Therefore has better performance and is cheaper and required more simple switches control circuits. It should be noted that all these topologies are symmetrical.

As above-mentioned, the other important parameter in the inverters is the maximum amount of blocked voltage on the switches. This parameter defines the rating of switches, as this amount goes up, the rating of switches also goes up and the inverter price will increase. According to Fig.7 the blocking voltage in proposed topology is less than others and his topology can be cheaper rather than other topologies.

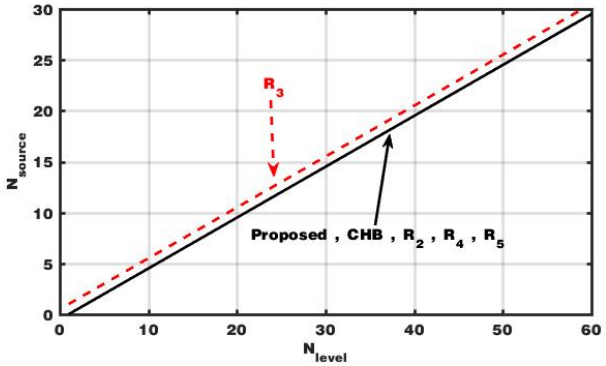

Fig. 5: Comparison of N_{source} in different topologies

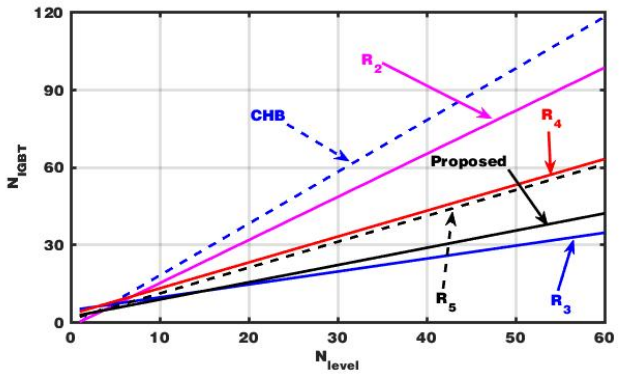

Fig. 6: Comparison of N_{IGBT} in different topologies

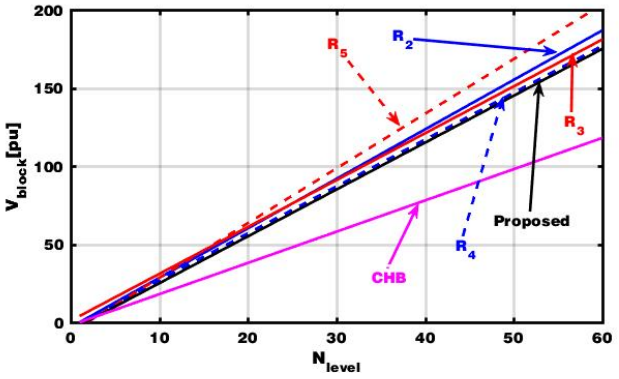

Fig. 7: Comparison of V_{block} in different topologies

IV. Calculation of losses in the proposed topology

In this section, the losses of power electronic switches are calculated. Generally, the switches have two types of losses (i.e. Conduction losses and switching losses) [33].

A. Conduction loss calculation

Since the switches include transistors and diodes, the losses of a transistor and a diode are calculated as follows:

$$p_{cond,T}(t) = \left[V_T + R_T.i^{\beta}(t)\right]i(t) \quad (11)$$

$$p_{cond,D}(t) = [V_D + R_D.i(t)]i(t) \quad (12)$$

Where, V_T and V_D are the threshold voltages of power devices. R_T and R_D are the equivalent resistance of the transistor and diode, respectively. In the proposed basic unit, there are 4 switches in current path in every operating modes of inverter. Also, in each half cycle, the transistor and its anti-parallel diode are conduct for (π-φ) radian and (φ) radian, respectively. Where φ is the power factor angle. The total conduction losses of the switches are calculated as follows:

$$P_{cond} = \frac{4}{\pi}\int_0^{\varphi} p_{cond,D}\,d\omega t + \frac{4}{\pi}\int_{\varphi}^{\pi} p_{cond,T}\,d\omega t$$

$$= \frac{4V_T I_P}{\pi}(1+\cos\varphi) + \frac{4R_T I_P^{\beta+1}}{\pi}\int_{\varphi}^{\pi}\sin^{\beta+1}(\omega t)\,d\omega t$$

$$+\frac{4V_D I_P}{\pi}(1-\cos\varphi) + \frac{4R_D I_P^2}{4\pi}(2\varphi - \sin(2\varphi)) \quad (13)$$

Where, I_P is the peak value of the output current. Also, β is a constant related to the specification of the transistor.

B. Calculation of the switching losses

The switching losses are calculated based on the calculation of energy losses. Switching losses occur during turn-off and turn-on period. For simplicity of calculation, it is assumed that the voltage and current of the switches changes linearly during the switching period [31]. Based on the above assumptions, the following relationships can be written for a switch:

$$E_{on,k} = \int_0^{t_{on}} v(t).i(t)dt$$

$$= \int_0^{t_{on}}\left[\left(\frac{V_{IGBT,k}}{t_{on}}t\right).\left(-\frac{I}{t_{on}}(t-t_{on})\right)\right]dt$$

$$= \frac{V_{IGBT,k}.I.t_{on}}{6} \quad (14)$$

$$E_{off,k} = \int_0^{t_{off}} v(t).i(t)dt$$

$$= \int_0^{t_{off}}\left[\left(\frac{V_{IGBT,k}}{t_{off}}t\right).\left(-\frac{I}{t_{off}}(t-t_{off})\right)\right]dt$$

$$= \frac{V_{IGBT,k}.I.t_{off}}{6} \quad (15)$$

Where, $E_{on,k}$ and $E_{off,k}$ are the turn on and turn off energy losses of the k-th switch. Also, t_{on} and t_{off} are turn on and turn off time of the switch, respectively. The proposed topology has 8 switches in each basic unit. So the energy losses in m-th unit is obtained as follows:

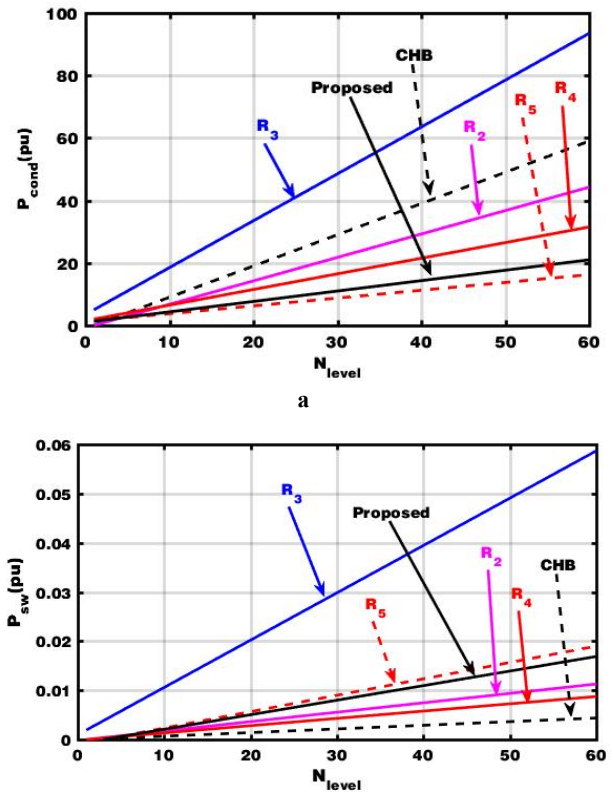

Fig. 8: Comparison of the losses in different topologies; a) The conduction losses; b) The switching losses

$$E_{sw} = \sum_{k=1}^{8} N_{on,k}.E_{on,k} + N_{off,k}.E_{off,k}$$
$$= \frac{I}{6}\sum_{k=1}^{8}\left(N_{on,k}.t_{on} + N_{off,k}.t_{off}\right).V_{IGBT,k} \quad (16)$$

Where $N_{on,k}$ and $N_{off,k}$ and $V_{IGBT,k}$are the number of turning on and turning off and the revers voltage on the k-th switch during a period of output voltage, respectively. I is the current through the switches before turning off or is the current through the switches after turning on. The total power loss for the proposed topology is obtained as follows:

$$P_{sw} = \sum_{m=1}^{n} f_m.E_{sw,m}$$
$$= \frac{I}{6}\sum_{m=1}^{n}\left[\sum_{k=1}^{8}\left(N_{on,k}.t_{on} + N_{off,k}.t_{off}\right).V_{IGBT,k,m}\right] \quad (17)$$

Where n is the number of the series units in the cascaded topology. Also $E_{sw,m}$ and f_m are the total energy losses and the frequency of the output voltage related to m-th unit in cascaded inverter, respectively. In Fig. 8, the losses of the proposed topology are compared with the losses in other topologies. As it is clear from the figure, the proposed topology has fewer conduction losses than others and has fewer switching losses than some of other topologies.

V. Simulation and Experimental results

A. *Simulation results*

To examine the proposed topologies and to generate the desired output voltage level waveforms, 9-Level proposed symmetric multilevel inverter is simulated using the computer simulation tool MATLAB / Simulink. The simulated output voltage and current is shown in Fig. 9 and Fig. 10.

In the simulation, each dc source magnitude is 50V with load value **R=50Ω** and **L=50mH.** The nearest voltage level modulation techniques is implied as a modulation method which is preferable for a higher number of voltage steps [34].

Fig. 11 and Fig.12 show the gating signals of level generation part switches and the voltage across the level generation part switches. As shown in Fig. 12, the blocking voltage on the S_1, $S_3$and S_2, S_4switches are 100V and 50V, respectively.

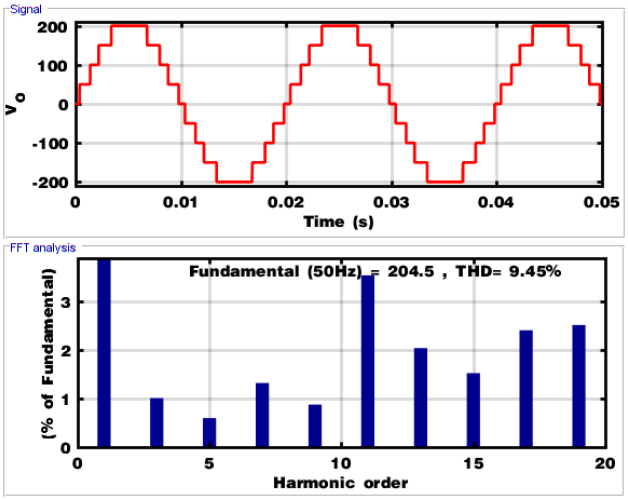

Fig. 9: Simulation output voltage waveform with harmonic spectrum

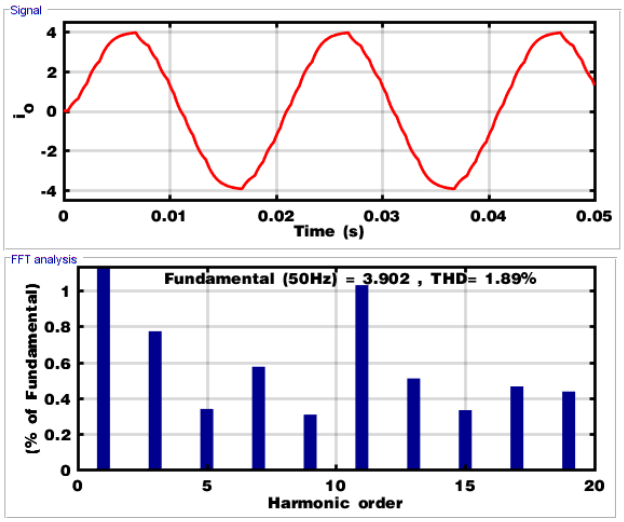

Fig. 10: Simulation output current waveform with harmonic spectrum

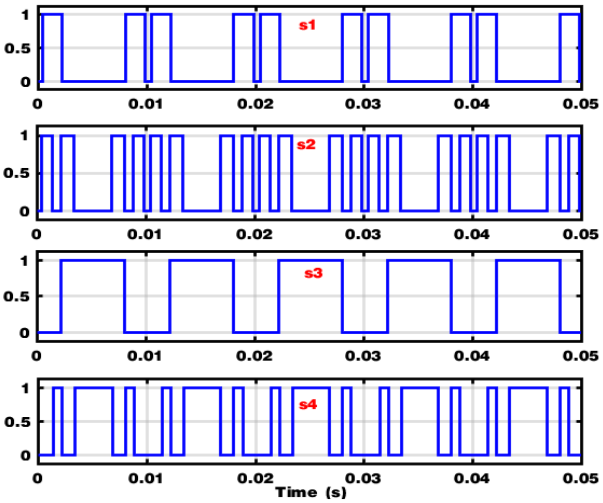

Fig. 11: Gate signals of level generator switches

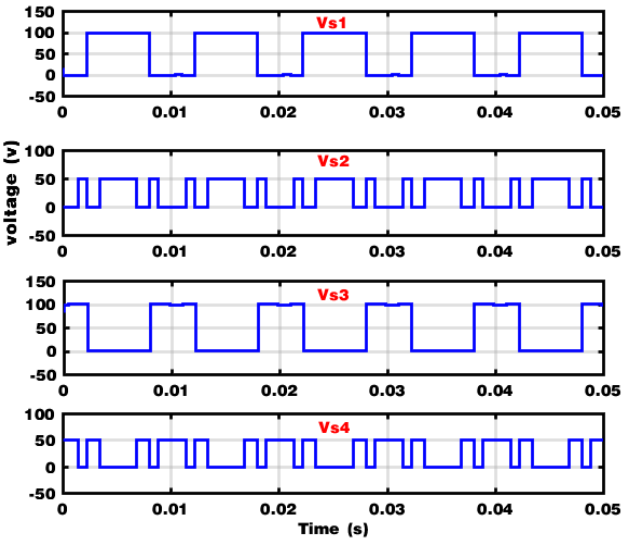

Fig. 12: Voltage across level generator switches.

B. Experimental results

In the practical tests, each dc source has a magnitude of 50V and the load values are **R=50**and **L=50mH**. For experimental tests, the switches gating control is carried out by EZDSP2812 which produce the switching pulses. The switches are IGBTs from the BUP306D and BUP314D type for the level-generation and the H-bridge part, respectively. Nearest level method is used to control the inverter and its gating. The experimented inverter (Fig. 13) uses 4 gate driver circuits, 8 switches (IGBTs and diodes) and 4 DC voltage sources. As it is clear from Fig.14a, the voltage waveform has 9 levels in output. Fig. 14bshows the load current of the experimental result which is almost a sinusoidal waveform with a phase angle difference with respect to the output voltage because of the inductive load. It is shown that the simulations and the experimental results confirm each other. However, the voltage drop on the switches in the experimental results may cause a little difference. It should be noted that the simulations are done with ideal switches.

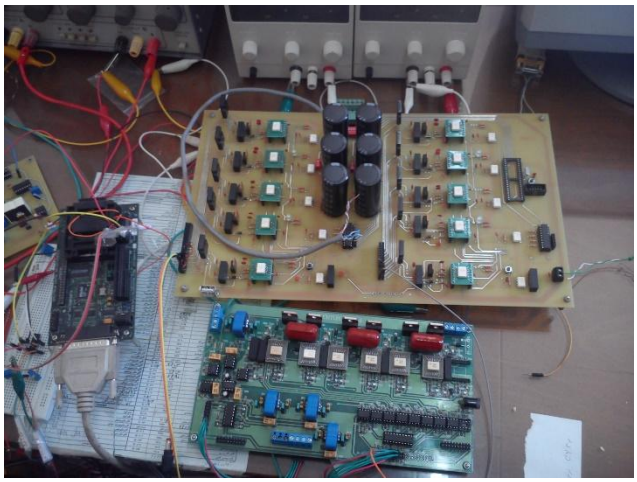

Fig. 13: The experimental set up circuit scheme

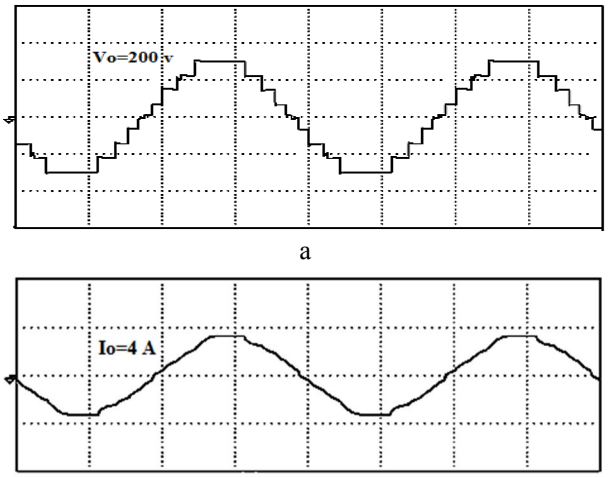

Fig. 14: Experimental results of proposed 9-level topology; a) Output voltage waveform; b) Output current waveform

VI. Conclusion

In this paper, a new symmetric topology for multi-level inverters was introduced. For the proposed topology, the number of IGBTs, the number of required dc voltage sources, and the value of the blocked voltage in the switches were decreased compared to several other symmetrical topologies for a certain number of output voltage levels. This leads to a decrease in the price and size of the inverter. Finally, the efficiency of the proposed symmetric multi-level inverter topology was confirmed by simulation and experimental results of a 9-level inverter. The simulation and experimental results confirms each other, which reflects the fact that the proposed topology can generate the output voltage with the desired magnitudes and levels.

VII. References

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