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A New Boost DC-DC Converter Based on a Coupled Inductor and Voltage Multiplier Cells

Mahmoodreza Eskandarpour Azizkandi[1], Farzad Sedaghati[2,†], and Hossein Shayeghi[3]

[1,2,3] Department of Electrical and Computer Engineering, University of Mohaghegh Ardabili, Ardabil, Iran

A B S T R A C T

A new non-isolated, coupled-inductor, single-switch boost DC-DC converter for photovoltaic (PV) power application is introduced in this paper. A coupled inductor and voltage multiplier cells are used in the presented converter to obtain high voltage conversion ratio. Also, a passive clamp circuit is applied in the converter structure to reduce voltage stress of the power switch. This leads to using of a power switch with lower on-state resistance in the converter which decreases the switch conduction loss. In addition, zero current switching (ZCS) condition for the power switch is achieved due to the use of the clamp circuit. Several advantages such as low operating duty cycle, high voltage conversion ratio, lower voltage stress of semiconductors, lower turn ratio of the coupled inductor, leakage inductance reverse recovery and high efficiency operation make the presented converter suitable for renewable energy applications. Steady state operation of the suggested converter in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is expressed and analyzed. Then, the presented topology is compared with several similar topologies to prove its advantages. Finally, experimental measurement results of a laboratory prototype of the proposed DC-DC converter with about 213W output power and 435V output voltage at 50kHz switching frequency are presented to corroborate its feasibility and performance.

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I. INTRODUCTION

In recent years, renewable energy resources such as photovoltaic (PV), and wind power have attracted many attention to extend using of them instead of fossil fuels. Sustainable energy resources are more useful than fossil fuels because of the scarcity of fossil fuels, global warming and environmental pollution concerns [1]. PV power system is the widest and most available renewable energy resources in the world, which are employed to produce electrical energy. Generally, the ouput voltage level of PV panels are low that is not suitable for connecting them to the grid. In order to solve this problem, it is possible to connect the PV panels in series to produce a high voltage level, but in this case, the problem of shadow effect is created [2]. According to the aforementioned problem, high voltage gain and high efficiency DC-DC converters are required to step up DC voltage level of PV panels [3]. The general structure of a PV system is shown in Fig. 1. According to this figure, a DC-DC converter is utilized to increase PV generated voltage level and deliver to an inverter for injection of power to the grid.

Several boost DC-DC converters with high voltage conversion ratio have been introduced in the literature for PV power application [4], [5]. In isolated converter types, the efficiency is less than that of non-isolated converters and the turn's ratio of the transformer in isolated converters can be adjusted to increase the voltage gain [6], [7]. However, the transformers are bulky and reduce power density. In the several types of DC-DC converters, the conventional boost converter appears as the first choice, when the isolation in DC-DC converters is not required. Because the conventional boost DC-DC converter is the simplest topology of DC-DC converters to increase voltage conversion ratio.

†Corresponding Author: farzad.sedaghati@uma.ac.ir
Tel: +98-4533512910, Fax: +98-4533512904,
University of Mohaghegh Ardabili ,Faculty of Electrical and Computer Engineering, University of Mohaghegh Ardabili, Ardabil, Iran

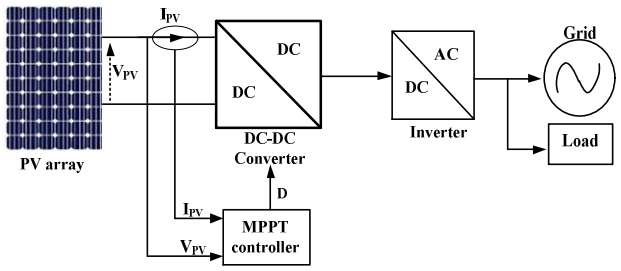


Fig. 1. General structure of a photovoltaic power system.

However, a high duty cycle is needed, which reduces efficiency of the converter. Moreover, voltage stress of the switch and diode is equal to the output voltage, which increases the switches cost for applications with high output voltage. Among the several types of DC-DC converters, non-isolated converters have gained considerable attention because of their relatively lower losses, cost, and size [8-10].

Switched-capacitor and switched-inductor converters are other types of non-isolated DC-DC converters for increasing the voltage gain [11-13]. In switched-inductor topologies, the current stress of the power switches is high while in switched-capacitor based structures, the voltage stress is very high that is the main problem in this type of converters [14].

Coupled inductor based converters are common as well. When a coupled inductor is used in a DC-DC converter, a high voltage gain in low duty cycles is achieved [15-28]. Usually, voltage multipliers and switched capacitors are also utilized in their topologies to increase the output voltage level. It should be noted that in these converters, by adding an active clamp circuit, the efficiency can be improved and the switch voltage stress is decreased. Therefore, switches with low on-state resistance and low conduction loss can be employed. Furthermore, these converters have low reverse recovery ringing of the output diode due to their secondary leakage inductance. Some high step up single switch coupled inductor high gain DC-DC converters are presented in the recently published papers. Although, their voltage gain are not high enough. Interleaved converters based on coupled inductor have been presented in [29] and [30]. These converters have a small amount of magnetic, small size and small input current ripple. However, employing more components number are the main disadvantages of the mentioned converters.

In this paper, integration of voltage multiplier cells and coupled inductor is presented to implement a high step up single switch high gain DC-DC converter. The coupled inductor can be utilized to step up the static gain, and the voltage multiplier cell proffers extra voltage gain. The stored energy in the leakage inductance of the coupled inductor can be recycled via the passive voltage clamp circuit which decreases voltage stress on the main switch, and so decreases conduction loss. The suggested converter interests from several advantages such as achieving high voltage conversion ratio in low duty cycles using low turn ratio of coupled inductor, utilization of only one active switch under zero current switching (ZCS), reduced voltage stress on the semiconductors, low conduction and switching losses, leakage inductance energy recovery and high efficiency.

The rest of the paper is organized as follows: the presented converter configuration and its operation principle in CCM and DCM are studied in Section 2. Steady state analysis of the proposed converter operation in CCM and DCM are expressed in Section 3. In Section 4, design guidelines of the suggested converter are discussed. In Section 5, comparison of the presented converter with several similar converters is given. Section 6 presents the experimental measurement results of a laboratory prototype of the converter, and finally, conclusions are given in Section 7.

II. Configuration and Operation Principle of Proposed Converter

Equivalent power circuit of proposed boost DC-DC converter is shown in Fig. 2. As shown in this figure, the presented converter consists of a power switch, S, six capacitors, C_1, C_2, C_3, C_4, C_5 and C_O, six diodes, D_1, D_2, D_3, D_4, D_5 and D_O, one coupled inductor and output load, R_O. According to this figure, the coupled inductor can be modeled as an ideal transformer including a magnetizing inductance, L_m, and a leakage inductance, L_{Lk}. N_P and N_S are the numbers of primary and secondary windings turn of the ideal transformer, respectively. Capacitor C_1 and diode D_1 are employed as clamp circuit components to recover the energy reserved in the leakage inductor. Capacitor C_2, diode D_2 and the secondary side of the coupled inductor are the circuit elements of the voltage multiplier cell which enhance the voltage of clamping capacitor. Also, the capacitors C_4 and C_5 and diodes D_4 and D_5 operate as a voltage multiplier cell to step up the converter voltage conversion ratio.

In order to simplify the circuit analysis of the suggested converter, the following assumptions are presumed:

- Capacitors C_1-C_5 are large enough and the voltages across them are assumed to be constant in each switching cycle.
- All parasitic components are ignored and all devices are considered to be ideal.
- Coupled inductor turn ratio, n, is equal to be N_S/N_P.

A. Continuous Conduction Mode (CCM) Operation

Operation principle of presented DC-DC converter in CCM includes 5 time intervals. Fig. 3 shows key waveforms of converter operation in CCM. Also, current flow path of the converter in different modes are illustrated in Fig. 4. The operating modes are explained as follow:

Mode 1 [t_0, t_1]: As shown in Fig. 4(a), in this mode, the power switch S is turned on, and diodes D_3, D_4 and D_O are on.

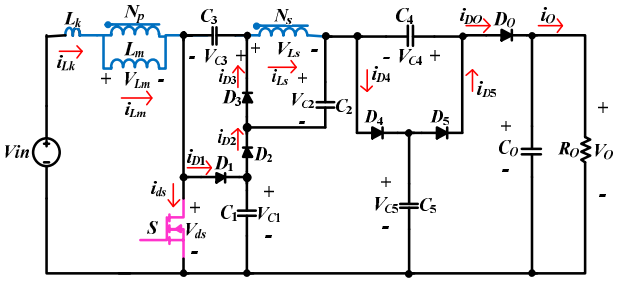


Fig. 2. Equivalent power circuit of proposed boost DC-DC converter.

In this time interval, the current of leakage and magnetizing inductors are increased linearly. The capacitors C_2 and C_5 are charged through diodes D_3 and D_4, respectively. The magnetizing inductance, L_m, is charged by the input voltage source and the energy stored in the capacitors C_3 and C_4 is transferred to the output load. This time interval finishes when the current of leakage inductor becomes equal to the magnetizing current.

Mode 2 [t_1, t_2]: In the second mode, switch S is still on and diodes D_1, D_3, D_4 and D_O are blocked and diodes D_2 and D_5 are on, as given in Fig. 4(b). In this mode, the input source energy is transferred to the leakage and magnetizing inductors and capacitor C_4 is charged via capacitor C_5. The secondary side of transformer charges capacitor C_3 and the output capacitor provides energy to the load. This subinterval is finished when the switch S is turned off.

Mode 3 [t_2, t_3]: As shown in Fig. 4(c), switch S is turned off, and diodes D_1, D_2 and D_5 conduct the current. The current of leakage inductance is reduced linearly and flows through diode D_1 and turns it on. Energy of secondary winding charges capacitor C_3. Also, capacitors C_2 and C_5 are discharged through diodes D_2 and D_5, respectively. When the currents of leakage and magnetizing inductors become equal, this time interval ends.

Mode 4 [t_3, t_4]: During this mode, the power switch S is still in off state, and diodes D_1, D_3, D_4 and D_O are in on state and diodes D_2 and D_5 are reverse biased. In this mode, the currents of the leakage inductance, I_{Lk} and magnetizing inductance, I_{Lm} decrease linearly. The current direction is depicted in Fig. 4(d). Stored energy in the leakage inductance is demagnetized to capacitor C_1 through diode D_1. The input voltage source, V_{in}, and capacitors C_3 and C_4 charge output capacitor, C_O, and transfer energy to the load. When diode D_1 is reverse biased at t=t_4, this time interval ends.

Mode 5 [t_4, t_5]: As shown in Fig. 4(e), in this interval, diodes D_3, D_4 and D_O conduct and the switch S is still off. The leakage and magnetizing inductance currents are decreased linearly. In this mode, the input DC voltage source, V_{in} and the energy stored in the capacitors C_3 and C_4 and inductances of both sides of the transformer supplied the output capacitor, C_O, and transfer required energy to the load.

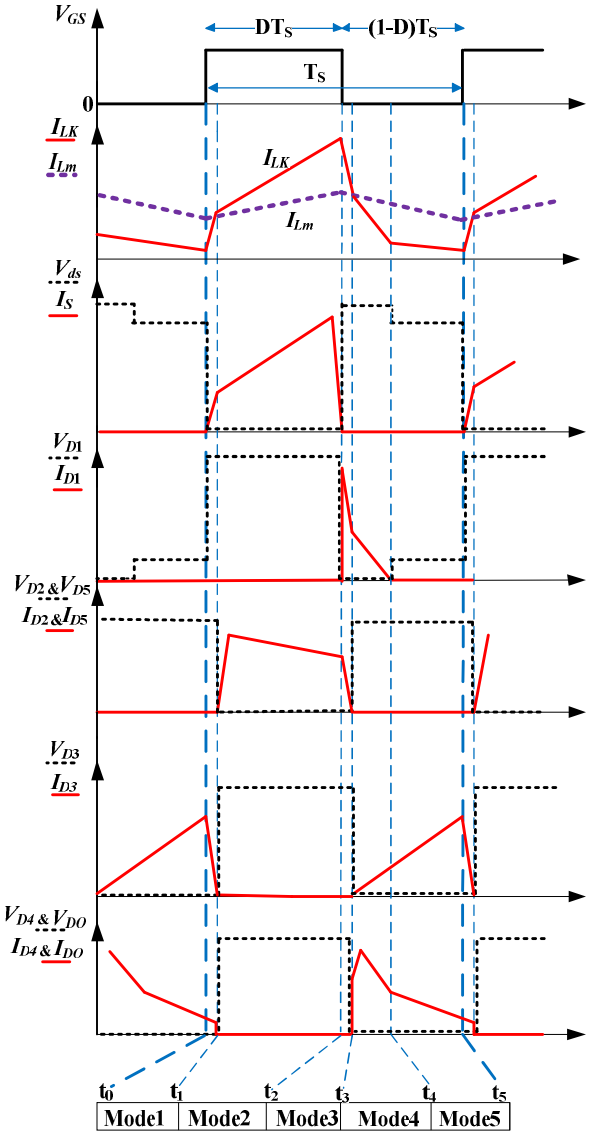


Fig. 3. Key waveforms of proposed DC-DC converter operation in CCM.

This mode finishes when the power switch S starts to conduct at the beginning of the next switching cycle.

B. Discontinuous Conduction Mode (DCM) Operation

Since the leakage inductance is very small, its voltage drop can be neglected with compared to the voltage across the magnetizing inductance. Thus, to simplify the DCM analysis, the leakage inductance of the coupled inductor is neglected. DCM time interval is divided into three modes. The main waveforms of the converter operation modes in DCM are depicted in Fig. 5. Also, the current direction of subintervals is given in Fig. 6. Furthermore, the coupled inductor with its equivalent circuit is illustrated in this figure including a magnetizing inductor, L_m, and an ideal transformer. The operating modes are expressed as follows:

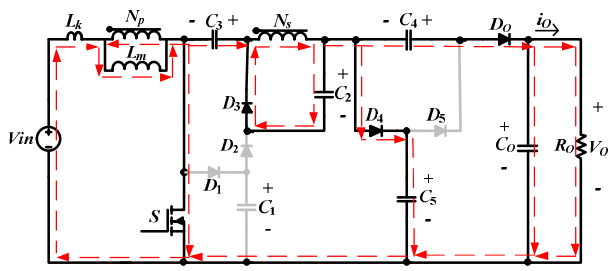


Fig. 4 (a)

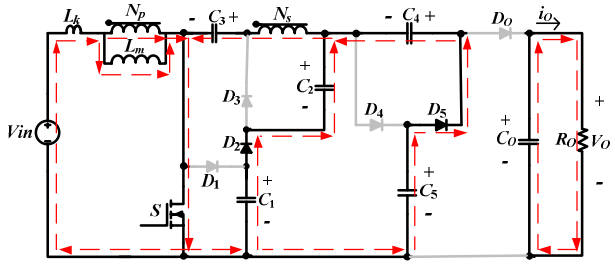


Fig. 4 (b)

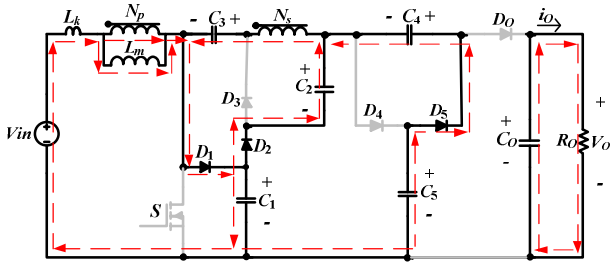


Fig. 4 (c)

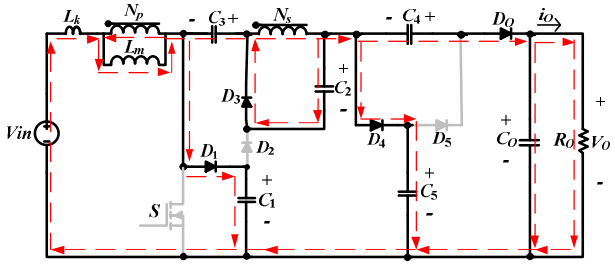
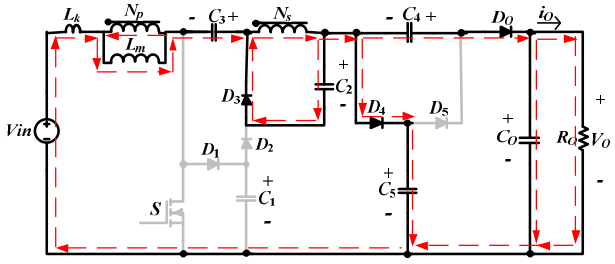


Fig. 4 (d)



(e)

Fig. 4. Current flow path of converter operating modes in CCM: (a) Mode 1, (b) Mode 2,(c) Mode 3, (d) Mode 4, and (e) Mode 5.

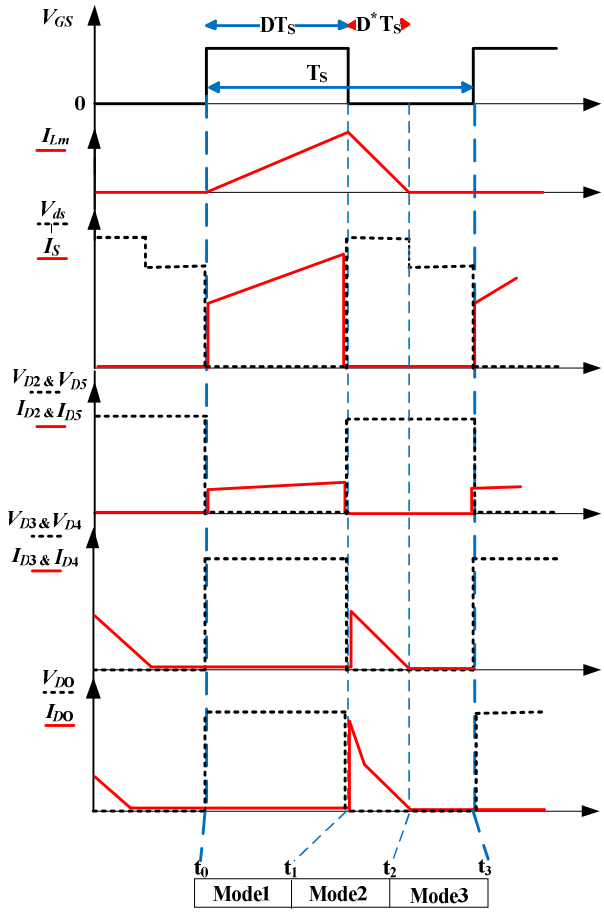


Fig. 5. Main waveforms of presented converter operation in DCM.

Mode 1 [t_0, t_1]: At the beginning of this time interval, switch S is turned on, and diodes D_2 and D_5 are on. According to Fig. 6(a), the magnetizing inductance current, I_{Lm} is increased linearly from zero. Capacitors C_1, C_2 and C_5 are discharged, and the output capacitor energy is transferred to the load. The end of this state is when the main switch S is turned off.

Mode 2 [t_1, t_2]: In the second mode, the active switch is in off state and diodes D_3, D_4 and D_O are on as indicated in Fig. 6(b). According to this figure, the stored energy of magnetizing inductance is transferred to the capacitor C_1 through diode D_1 and turns it on. Capacitors C_3 and C_4 are in series with the input voltage source and L_m, and give their energy to the output capacitor and load. This mode ends when the magnetizing inductance current is decreased to zero.

Mode 3 [t_2, t_3]: As given in Fig. 6(c), during this mode, switch S is still off and diodes D_1-D_5 and D_O are off simultaneously. The current of magnetizing inductance is zero. Therefore, the load, R_O, is supplied by the output capacitor. This subinterval ends when the power switch S is turned on and the switching cycle starts again from Mode 1.

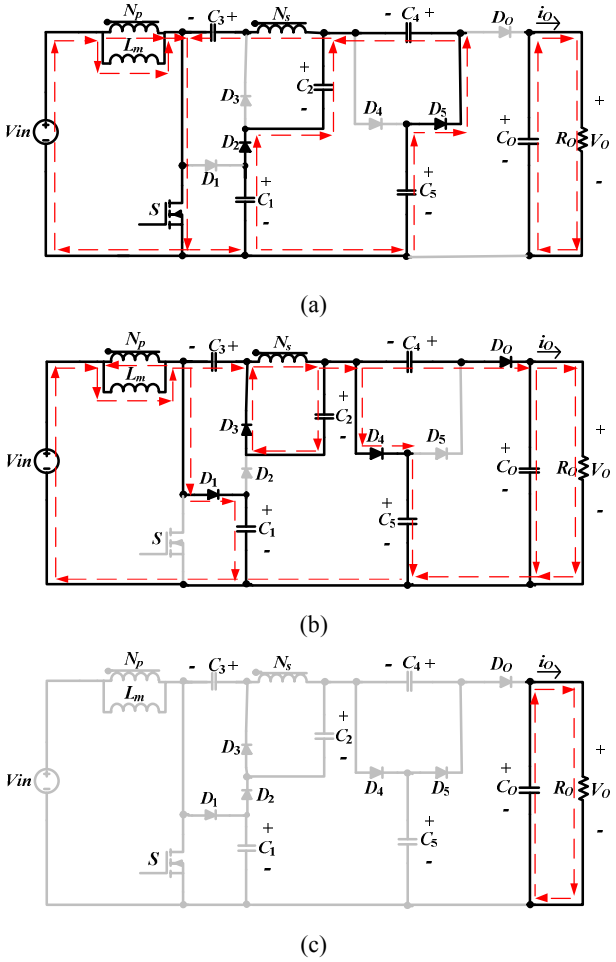


Fig. 6. Current flow path of converter operating modes in DCM: (a) Mode 1, (b) Mode 2, and (c) Mode 3.

III. Steady-State Analysis of Proposed Converter

A. CCM Operation

In order to clarify the analysis of suggested converter in steady-state study, leakage inductance of the coupled inductor is neglected. In addition, power losses of the switching components are not considered. In CCM operation analysis, only stages 2, 4 and 5 are considered because the time duration of modes 1 and 3 are little considerably. In the second mode, power switch S starts to conduct and the magnetizing inductance, L_m, is supplied by the input voltage source, V_{in}. Therefore, according to Fig. 4(b), we have:

$$V_{Lm} = V_{in} \tag{1}$$

$$V_{C3} - V_{C2} - V_{C1} = nV_{in} \tag{2}$$

$$V_{C4} + V_{C1} + V_{C2} - V_{C5} = 0 \tag{3}$$

During modes 4 and 5, the switch S is turned off and magnetizing inductance is discharged. The voltage across L_m is determined by using the following equations:

$$V_{Lm} = V_{in} - V_{C1} \tag{4}$$

$$V_{Lm} = V_{in} - V_{C5} + V_{C2} + V_{C3} \tag{5}$$

The voltage of capacitor C_2 is calculated as given in Equ. (6).

$$V_{C2} = nV_{C1} - nV_{in} \tag{6}$$

In mode 4, the following equation is achieved for the output voltage:

$$V_O = V_{C5} + V_{C4} \tag{7}$$

By using the inductor volt-second balance law, following equations are expressed for the magnetizing inductance, L_m:

$$\int_0^{DT_s} V_{in}\,dt + \int_{DT_s}^{T_s} (V_{in} - V_{C1})dt = 0 \tag{8}$$

$$\int_0^{DT_s} V_{in}\,dt + \int_{DT_s}^{T_s} (V_{in} - V_{C5} + V_{C2} + V_{C3})dt = 0 \tag{9}$$

From Equ. (8), the voltage across capacitor C_1 is equal to Equ. (10).

$$V_{C1} = \frac{V_{in}}{1-D} \tag{10}$$

By using Equs. (6) and (10), the voltages across capacitor C_2 is determined as follows:

$$V_{C2} = \frac{nD}{1-D} V_{in} \tag{11}$$

According to Equs. (2), (10) and (11), the voltage across capacitor C_3 is obtained by using the following equation:

$$V_{C3} = \frac{(n+1)}{1-D} V_{in} \tag{12}$$

From Equ. (9) and also, by using Equs. (11) and (12), the voltage across capacitor C_5 is derived as given in Equ. (13).

$$V_{C5} = \frac{(2+n+nD)}{1-D} V_{in} \tag{13}$$

By substituting Equs. (10), (11) and (13) into Equ. (3), the voltage of capacitor C_4 is expressed as follows:

$$V_{C4} = \frac{(n+1)}{1-D} V_{in} \tag{14}$$

From Equs. (7), (13) and (14), the voltage conversion ratio of the converter in CCM, M_{CCM}, is achieved as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{(3+2n+nD)}{(1-D)} \tag{15}$$

Voltage gain of the proposed converter, M_{CCM}, versus switch duty cycle, D, and the turn ratio of coupled inductor, n, is indicated in Fig. 7. When the turn ratio of coupled inductor is equal to zero, the voltage conversion ratio of the presented DC-DC converter is greater than the conventional boost DC-DC converter. According to Fig. 7, the voltage gain increases considerably with increasing of the turn ratio.

B. DCM Operation

Operation time intervals in DCM can be expressed in three modes. Main waveforms of DCM operation are depicted in Fig. 5, and also, the current direction of operating modes is given in Fig. 6. According to Fig. 6(a), in the first mode, the following equations are achieved:

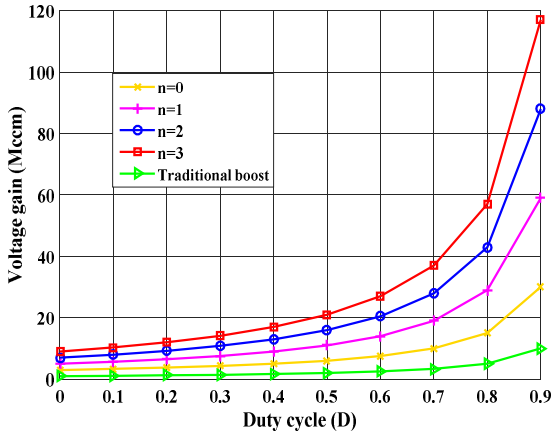


Fig. 7. Voltage gain of presented converter in CCM, M_{CCM}, versus power switch duty cycle, D, and turn ratio of coupled inductor, n.

$$V_{Lm}^{1} = V_{in} \tag{16}$$

$$\frac{V_{Ls}}{V_{Lp}} = \frac{V_{Ls}}{V_{Lm}} = \frac{N_s}{N_p} = n \tag{17}$$

$$V_{C4} = V_{C5} - V_{C1} - V_{C2} \tag{18}$$

According to Equs. (16) and (17), during mode 1, the voltage of the secondary winding is derived as follows:

$$V_{Ls}^{1} = nV_{in} \tag{19}$$

If D^* is defined as duty cycle of the magnetizing inductance current from peak point ramped down to zero, by applying the volt-second balance law to the magnetizing inductance, the following equation is obtained:

$$V_{Lm}^{1}\,dt + \int_{DT_s}^{(D+D^*)T_s} V_{Lm}^{2} dt + \int_{(D+D^*)T_s}^{Ts} V_{Lm}^{3} dt = 0 \tag{20}$$

Considering $V_{Lm}^{3} = 0$, and substituting Equ. (16) into Equ. (20) yields:

$$V_{Lm}^{1}\,dt + \int_{DT_s}^{(D+D^*)T_s} V_{Lm}^{2} dt = 0 \tag{21}$$

$$V_{Lm}^{2} = -\frac{D}{D^*} V_{in} \tag{22}$$

Therefore, according to mode 2, the voltage of secondary winding is calculated as follows:

$$V_{Ls}^{2} = nV_{Lm}^{2} = n\left(-\frac{D}{D^*}V_{in}\right) = \left(-\frac{nD}{D^*}V_{in}\right) \tag{23}$$

As shown in Fig. 6(b), by applying Kirchhoff's voltage law in mode 2, the following equation can be achieved:

$$V_{C5} = V_{C1} + V_{C2} + V_{C3} \tag{24}$$

According to Fig. 6(b) and using Equs. (22) and (23), the voltages across capacitors C_1 and C_2 are obtained as given in Equs. (25) and (26).

$$V_{C1} = -V_{Lm}^{2} + V_{in} = \frac{D + D^*}{D^*} V_{in} = \left(1 + \frac{D}{D^*}\right) V_{in} \tag{25}$$

$$V_{C2} = -V_{LS}^{2} = \frac{nD}{D^*} V_{in} \tag{26}$$

During the second time interval, the output voltage, V_O, is expressed as follows:

$$V_O = V_{C1} + V_{C2} + V_{C4} \tag{27}$$

Considering the voltage equations for Fig. 6(a), and using Equs. (18), (19), (24), (25) and (26), the voltage across the capacitors C_3, C_4 and C_5 are obtained as follow:

$$V_{C3} = V_{LS}^{1} + V_{C2} + V_{C1} = \left(n + 1 + \frac{D}{D^*} + \frac{nD}{D^*}\right) V_{in} \tag{28}$$

$$V_{C5} = \left(n + 2 + \frac{2D}{D^*} + \frac{2nD}{D^*}\right) V_{in} \tag{29}$$

$$V_{C4} = \left(n + 1 + \frac{D}{D^*} + \frac{nD}{D^*}\right) V_{in} \tag{30}$$

Substituting Equs. (29) and (30) into Equ. (27), and using a simplification, voltage gain of the suggested DC-DC converter in DCM operation is achieved as given in the following:

$$M_{DCM} = \frac{V_O}{Vin} = \left[(2n+3) + 3(n+1)\frac{D}{D^*}\right] \tag{31}$$

Finally, D^* is determined as follows:

$$D^* = \frac{3(n+1)DV_{in}}{V_O - (2n+3)V_{in}} \tag{32}$$

IV. Design Procedure of Proposed Converter

A. Voltage Stress Analysis

In order to select proper semiconductor components for presented converter, the voltage stress across the switching components, such as main power switch and diodes, are determined. During CCM operation, the voltage stresses of switch S and diodes D_1~D_5 and D_O are achieved as given in Equs. (33)-(37).

$$V_{stress-S_1} = \frac{1}{1-D} V_{in} = \frac{M+n}{M(3n+3)} V_O \tag{33}$$

$$V_{stress-D_1} = -\frac{1}{1-D} V_{in} = -\frac{M+n}{M(3n+3)} V_O \tag{34}$$

$$V_{stress-D_2} = -\frac{n+1}{1-D} V_{in} = -\frac{M+n}{3M} V_O \tag{35}$$

$$V_{stress-D_3} = -\frac{n}{1-D} V_{in} = -\frac{n(M+n)}{M(3n+3)} V_O \tag{36}$$

$$V_{stress-D_{4,5,O}} = -\frac{n+1}{1-D} V_{in} = -\frac{M+n}{3M} V_O \tag{37}$$

Thus, one of the main merits of the presented converter is that the voltage stress across the main power switch and diodes are lower than the output voltage.

B. Inductor Design

The value of magnetizing inductor, L_m, is significant to make characteristic of the coupled inductor. In practice, the coupled inductor stores energy like an inductor. Also, the magnetizing inductor is designed as the magnetizing current to be continuous. Thus, the minimum value of the magnetizing inductance is defined as follow:

$$L_m \geq \frac{nDT_s}{\Delta i_{Lm}} V_{in} = \frac{nD}{fs\,\Delta i_{Lm}} V_{in} \tag{38}$$

Where Δi_{Lm} is the magnetizing inductance current ripple.

C. Capacitors Design

Capacitors C_1-C_5 are designed for presented converter by assuming same voltage ripple. According to Equs. (10)-(14), voltage of capacitors C_1-C_5 are achieved. Since the charge absorbed or produced by all capacitors are equal, the size of the capacitors are obtained as follow:

$$\Delta Q = \frac{DI_O}{f_S} \tag{39}$$

$$\Delta V_C = \frac{\Delta Q}{C} \tag{40}$$

$$C_i = \frac{DI_O}{\Delta V_{Ci} f_S} \tag{41}$$

where i=1, 2, 3, 4

V. COMPARISON STUDY

In order to clarify the advantages of presented DC-DC converter, some comparisons are discussed in this section. Some features of the suggested converter and similar structures presented in [19] and [21-26] are indicated in Table I. As shown in this table, with taking into consideration the voltage gain, the components of the suggested converter is equal to the converters presented in [23-25], however, the voltage conversion ratio of the presented topology is higher than the other topologies. Also, components number of the converter presented in [19] is higher, and its voltage gain is lower than the proposed converter. Moreover, the converter proposed in [26] has 3-winding coupled inductor. With consideration of n_3=1, this converter has a lower voltage gain than the presented DC-DC converter.

Fig. 8(a) indicates voltage gain comparison results of the proposed converter and the topologies presented in [19] and [21-25] for various duty cycles. According to this figure, the voltage conversion ratio of the proposed structure is greater than the other structures for all ranges of duty cycles (even for very low duty cycles). This advantage is due to the integration of a coupled inductor with voltage multiplier cells in the suggested converter.

The relationship among the normalized voltage stress on the main switch of the suggested structure and other structures is illustrated in Fig. 8(b). According to this figure, the normalized voltage stress on the main switch of the proposed converter under the same voltage gain is less than the other converters. However, for the voltage gain less than 10, the normalized voltage stress in converter presented in [21] is less than the proposed structure. Also, the presented converter in [21] has less voltage stress than the proposed converter in higher turn ratios. However, this converter has a very low voltage gain in comparison to the proposed converter. Thus, a switch with low $R_{DS(on)}$ resistance can be used in the presented converter to reduce the cost and increase the overall efficiency.

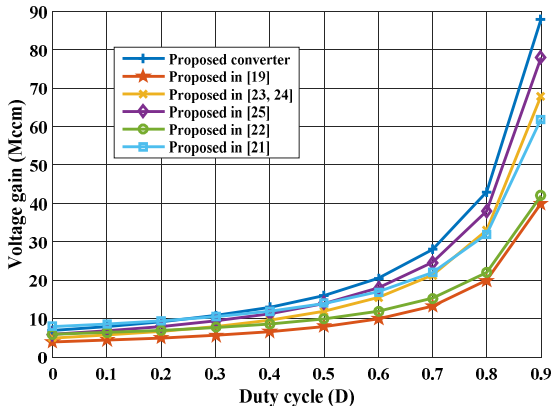
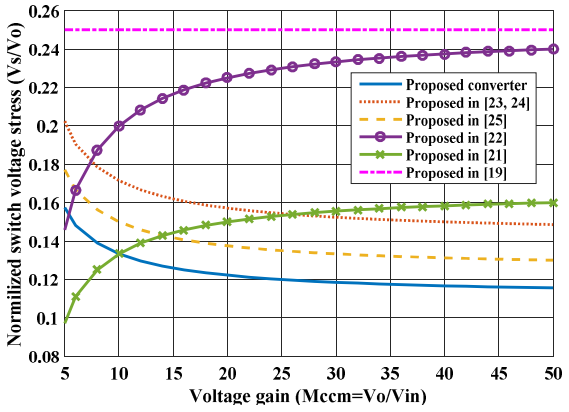


Fig. 8 (a)



(b)

Fig. 8. Comparison results of proposed DC-DC converter with some similar step up topologies: (a) voltage gain of several structures for different duty cycles, and (b) normalized voltage stress of power switches versus voltage gain in several topologies.

TABLE I

Comparison of Presented DC-DC Converter with Several Similar Topologies.

Reference	Number of Components				Voltage Gain	Voltage Stress on Switch
	Diode	Cap	Switch	Core		
Proposed converter	6	6	1	1	$\frac{3+2n+nD}{(1-D)}$	$\frac{M+n}{3n+3}Vin$
Converter in [19]	7	5	2	2	$\frac{n+2}{(1-D)}$	$\frac{M}{n+2}Vin$
Converter in [24]	6	6	1	1	$\frac{1+2n+nD}{(1-D)}$	$\frac{M+n}{3n+1}Vin$
Converter in [23]	6	6	1	1	$\frac{1+2n+nD}{(1-D)}$	$\frac{M+n}{3n+1}Vin$
Converter in [25]	6	6	1	1	$\frac{2+2n+nD}{(1-D)}$	$\frac{M+n}{3n+2}Vin$
Converter in [26]	6	6	1	1 (3winding)	$\frac{2+n_2+2n_3-n_3D}{(1-D)}$	$\frac{M-n}{n+2}Vin$
Converter in [22]	5	5	1	1	$\frac{2+2n-nD}{(1-D)}$	$\frac{M-n}{n+2}Vin$
Converter in [21]	5	5	1	1	$\frac{2+3n-nD}{(1-D)}$	$\frac{M-n}{2n+2}Vin$

Cap = capacitor; $M = M_{CCM} = (V_O / V_{in})$

VI. Experimental Test Results

To verify theoretical analysis and clarify performance of suggested DC-DC converter, a 213W prototype is designed and fabricated in the laboratory as shown in Fig. 9. The main characteristics of the fabricated prototype are presented in Table II. The presented structure converts 29V input voltage to 435V in the output. The switching frequency of the converter is chosen to be 50kHz. Therefore, the size of passive components is reduced. Ultrafast rectifiers with low forward voltage drop are utilized as power diodes. Main power switch is selected MOSFET IRFP260n with low on-state resistance. The type of coupled inductor core is ferrite EE55/28/21 and the coupled inductor turn ratio, n, is 1:2.

Experimental measurement results of the converter operation in CCM are given in Figs. 10-14. In all of the figures, the time per division is set to be 8µs. Input and output voltage waveforms are illustrated in Fig. 10(a). The input and output voltages are equal to 29V and 435V, respectively. Also, as shown in this figure, the ripple of the output voltage is very low. The voltage and current of power switch S is indicated in Fig. 10(b). It is clear that the maximum voltage on the power switch is about 60V.

TABLE II

Circuit Parameters of Implemented Prototype.

Specifications	Values
Input voltage	29 V
Output voltage	435 V
Output power	213 Watt
Duty cycle	0.50
Switching frequency	50 kHz
C_1, C_2, C_3, C_4 and C_5 C_{O1} C_{in}	47 uF/ 250 V 220 uF/ 450V 470 uF/ 63V
Coupled inductor	L_m=100uH $n=N_S/N_P=2$ EE-55 core
Power switch S	IRFP260n
D_1, D_2, D_3, D_4, D_5 and D_O	MUR1560
Switch gate driver	TLP250

Thus, a switch with low $R_{DS(on)}$ resistance can be utilized. Also, according to Fig. 10(b), it is obvious that the current of the switch S is zero when the power switch is turned off, which verify the ZCS condition of the presented structure.

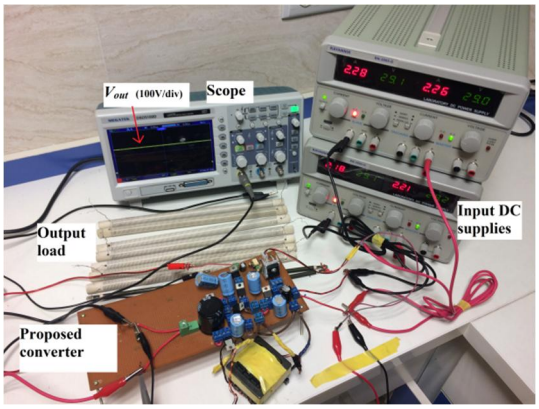


Fig. 9. Overall system of implemented prototype of presented structure.

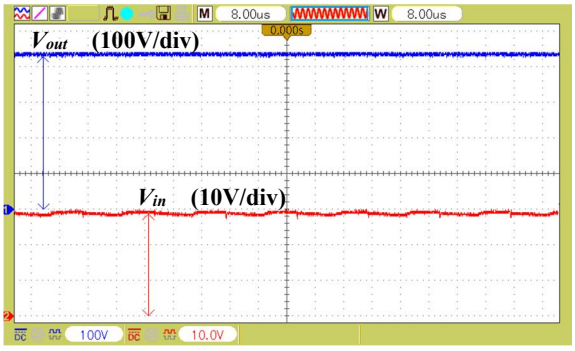


Fig. 10 (a) input and output voltages

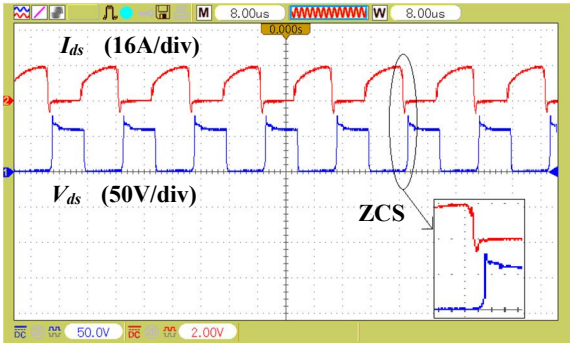
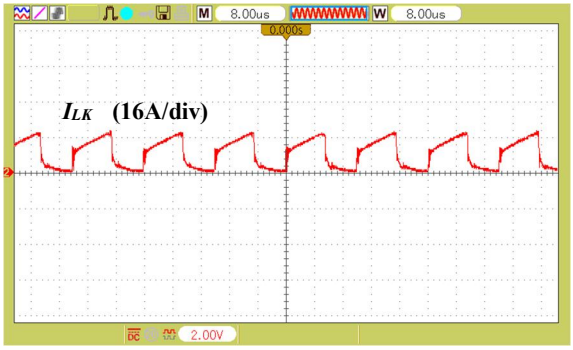


Fig. 10 (b) voltage and current of switch S



(c) leakage current of coupled inductor.

Fig. 10. Experimental measurement results of presented DC-DC converter: (a) input and output voltages, (b) voltage and current of switch S, and (c) leakage current of coupled inductor.

According to this figure, duty ratio of the main switch is close to 0.5. Moreover, as shown in Fig. 10(b),when the power switch starts to conduct, the current with maximum of 16A flows through the switch. The coupled inductor leakage current is shown in Fig. 10(c). The resultant waveform is similar to Fig. 3, which confirms the theoretical analysis.

Fig. 11(a)-(d) represents the voltage across diodes. The measured voltage across the diodes D_1, D_3, D_4, and D_O are found to be about 60V, 102V, 158V, and 157V, respectively. It is clear that the voltage stress of diodes are far lower than the output voltage; hence, the ultrafast diodes are employed to completely eliminate the reverse recovery current. The capacitors C_1-C_5 voltage waveforms are shown in Fig. 12(a)-(c). The voltages across the capacitors C_1 and C_3, V_{C1} and V_{C3}, are about 62V and 163V, respectively, which are shown in Fig. 12(a). According to Fig. 12(b), the voltage across the capacitors C_2 and C_4, V_{C2} and V_{C4} are equal to 53V and 157V, respectively. The voltage across the capacitor C_5, V_{C5}, is about 272V which is depicted in Fig. 12(c).

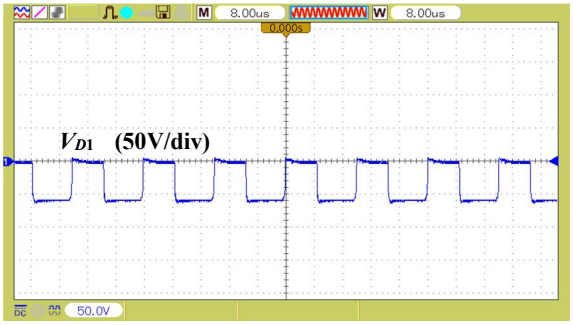


Fig. 11(a) Voltage waveform of diode D_1

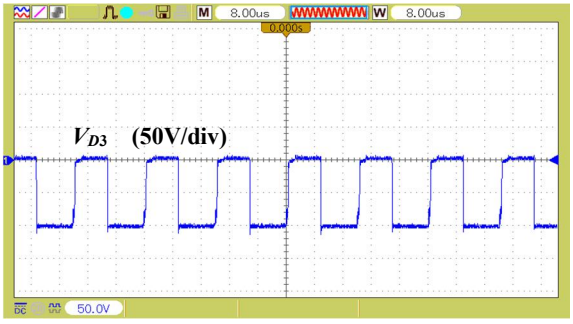


Fig. 11 (b) Voltage waveform of diode D_3

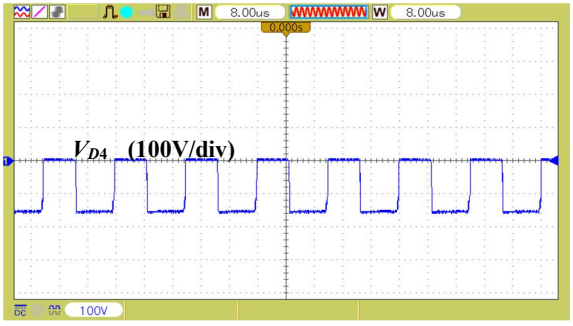
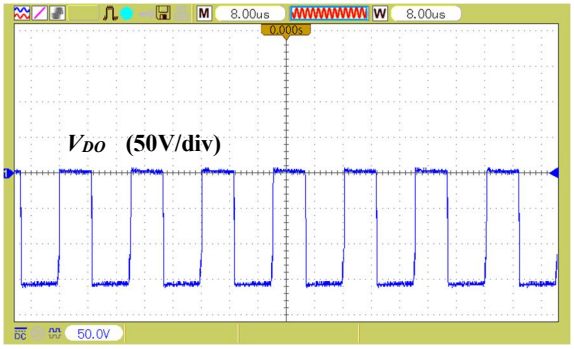


Fig. 11 (c) Voltage waveform of diode D_4



(d) Voltage waveform of diode D_O

Fig. 11. Voltage waveform of diodes: (a) D_1, (b) D_3, (c) D_4, and (d) D_O.

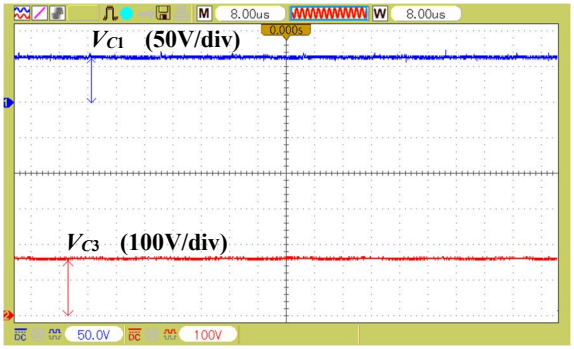


Fig. 12 (a) Voltage waveform of capacitors C_1 and C_3

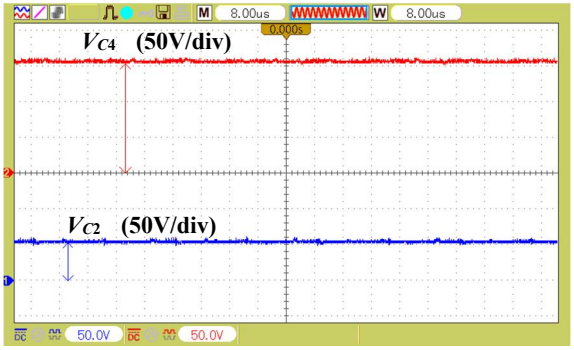
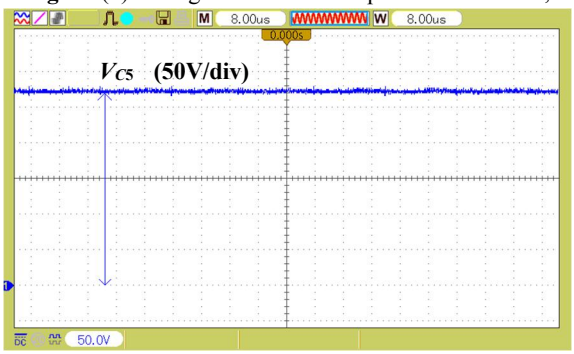


Fig. 12 (b) Voltage waveform of capacitors C_2 and C_4,



(c) Voltage waveform of capacitor C_5

Fig. 12. Voltage waveform of capacitors: (a) C_1 and C_3, (b) C_2 and C_4, and (c) C_5.

The current of diodes D_1-D_5, and D_O are depicted in Fig. 13(a)-(f). The obtained results confirm theoretical waveforms, given in Fig. 3.

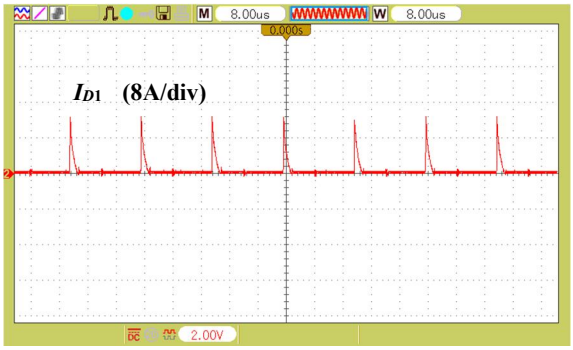


Fig. 13 (a) Current waveform of diode D_1

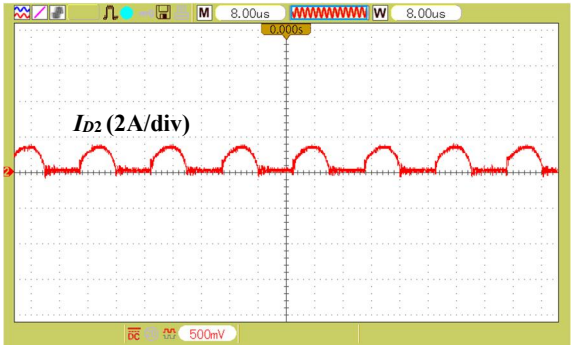


Fig. 13 (b) Current waveform of diode D_2

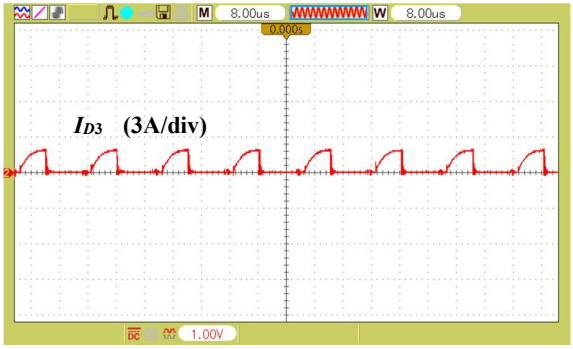


Fig. 13 (c) Current waveform of diode D_3

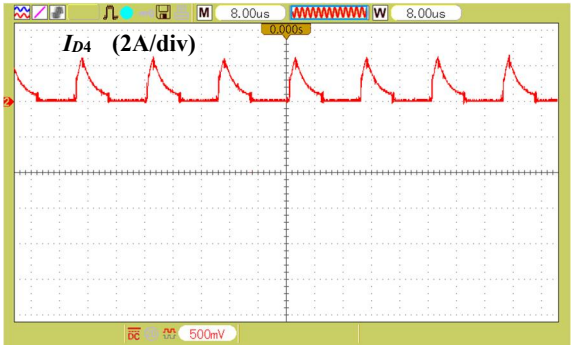


Fig. 13 (d) Current waveform of diode D_4

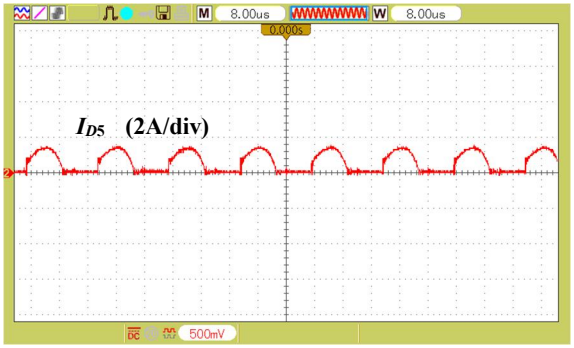
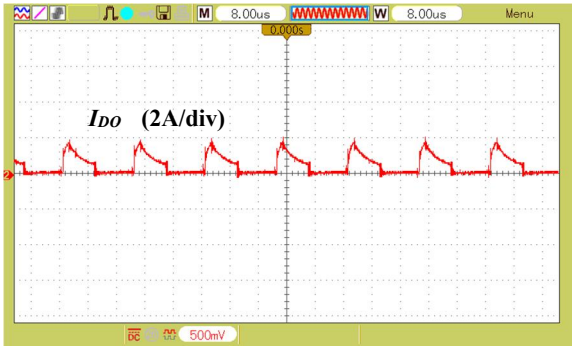


Fig. 13 (e) Current waveform of diode D_5



(f) Current waveform of diode D_O

Fig. 13. Current waveform of diodes: (a) D_1, (b) D_2, (c) D_3, (d) D_4, (e) D_5, and (f) D_O.

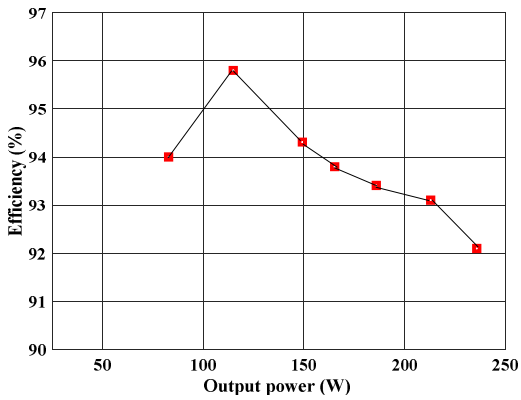


Fig. 14. Measured efficiency of presented DC-DC converter.

Fig. 14 shows efficiency of the suggested DC-DC converter for several output powers. The maximum efficiency of the converter under the output power of 115W is equal to 95.8%, and for the output power of 213W, the efficiency is equal to 93.1%.

Finally, according to the experimental measurement results, feasibility and analysis of the suggested topology are confirmed. Several advantages of the proposed DC-DC converter such as high voltage gain without a large duty cycle, ZCS turn off condition for the main power switch, low voltage stress across main switch and diodes, recycled leakage inductor and high efficiency make it suitable for renewable energy applications such as PV power system.

VII. Conclusions

In this paper, a non-isolated, high step up, single switch DC-DC converter was proposed. In the presented converter, high voltage gain is achieved by using a coupled inductor and voltage multiplier cells. The voltage conversion ratio of the presented converter is increased by raising the coupled inductor turn's ratio. The voltage stress on the main switch is low and so, a switch with low on-state resistance can be chosen. Also, the zero current switching (ZCS) of the power switch in off state was demonstrated. The converter operation in CCM and DCM were discussed in detail. Moreover, the steady state analysis and design procedure of the suggested topology were expressed. Then, the presented converter is compared with several similar structures where the comparison results show that the proposed converter voltage gain is higher and voltage stress of the power switch is lower than the other topologies. Finally, to demonstrate the performance of the presented converter, a laboratory prototype was implemented and tested.

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Mahmoodreza Eskandarpour Azizkandi was born in Hashtrood, Iran, in 1993. He received his B.S. degree in Electronics Engineering from Bonab University, Bonab, Iran, in 2016, and his M.S. degree in Power Electronics Engineering from the University of Mohaghegh Ardabili, Ardabil, Iran in 2019. His research interests include renewable energies, industrial electronics and power electronic converters.



Farzad Sedaghati was born in Ardabil, Iran, in 1984. He received the M.S. and Ph.D. degrees both in electrical engineering in 2010 and 2014 from the University of Tabriz, Tabriz, Iran. In 2014, he joined the Faculty of Engineering, Mohaghegh Ardabili, where he has been an Assistant Professor since 2014. His current research interests include renewable energies and power electronic converters design and applications.



Hossein Shayeghi received the B.S. and M.S.E. degrees in electrical and control engineering in 1996 and 1998, respectively, and the Ph.D. degree in electrical engineering from Iran University of Science and Technology, Tehran, Iran, in 2006. Currently, he is a full Professor in the Technical Engineering Department of the University of Mohaghegh Ardabili, Ardabil, Iran. His research interests are in the application of robust control, artificial intelligence and heuristic optimization methods to power system control design, operation, and planning, power system restructuring, and renewable energies applications. He has authored and co-authored five books in the electrical engineering area, all in Farsi, one book and two book chapters in international publishers, and more than 320 papers in international journals and conference proceedings. Prof. Shayeghi collaborates with several international journals as reviewer board member and works on the editorial committee of eight international journals. He has served on several other committees and panels in governmental, industrial, and technical conferences. He was selected distinguished researcher of the University of Mohaghegh Ardabili several times. In 2007, 2010, 2011, 2013 and 2017 he was also elected as distinguished researcher in engineering field in Ardabil province of Iran. He has been included in the Thomson Reuters' list of the top one percent of most-cited technical engineering scientists in 2015, 2016, 2017 and 2018, respectively. Also, he is a member of the Iranian Association of Electrical and Electronic Engineers (IAEEE).

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