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A Single-Phase Extendable Topology for Multilevel Inverters

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ABSTRACT

This paper presents a single-phase topology for multilevel inverters with minimum number of switching devices. The proposed topology significantly reduces the number of DC voltage sources, switches, and power diodes as the number of output voltage levels increases. The proposed multilevel inverter is constructed using series-connection of multilevel strings. Suggested multilevel string is composed of multiple basic switching units. The proposed multilevel inverter has extendable configuration that increases the number of output voltage levels more and more by adding more stages. The proposed multilevel inverter would be implemented in both symmetric and asymmetric configurations. Two different algorithms are introduced for determination of magnitude of DC voltage sources to reach the maximum number of output voltage levels with minimum number of semiconductor devices. Important characteristics of both symmetric and asymmetric configurations are extracted and compared with similar multilevel inverter topologies. Finally, a prototype of the proposed multilevel inverter is simulated and implemented experimentally to verify operation of the proposed multilevel inverter.

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I. INTRODUCTION

Multilevel inverters include an array of power electronic switches and DC voltage sources; generate voltages with staircase waveforms [1]. During recent decades, multilevel inverters are presented as key technologies in high-power medium-voltage power conversion systems. Therefore, multilevel inverters have become an important field of interest in industries and researches. While the classical topologies of multilevel inverter have proved to be a viable alternative in a wide range of high-power medium-voltage applications, there has been an active interest in the evolution of novel topologies.

The first converter topology to produce multilevel AC voltage from various DC voltage sources was proposed by Baker and Bannister in 1970 [2]. The suggested topology consists of single-phase inverters connected in series that is known as cascaded H-bridge (CHB) inverter. In contrast to the CHB inverter, a modified inverter topology was proposed in 1980 that can produce multilevel voltage from a single DC source with some diodes connected to the neutral point. This topology is known as neutral point clamped (NPC) inverter and/or diode clamped topology [3]. Other well-known multilevel inverter named as flying capacitor (FC) was introduced in 1990 [4], [5]. The cascaded H-bridge, diode clamped and flying capacitors topologies are referred to as the "classical topologies" of multilevel inverter. The mentioned classical topologies have been analyzed more and more during paste decades. In [6], a voltage balancing technique in a space vector modulated multilevel for diode clamped inverter has been presented. Analysis of synchronization strategy for cascaded H-Bridge multilevel inverter topology with carrier based sinusoidal phase shifted pulse width modulation (PSPWM) technique has been studied in [7]. A fault-diagnosis and fault-tolerant control

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scheme for flying capacitor multilevel inverters has been introduced in [8]. A new DC-power control method for CHB converter is proposed in [9].

However, beside classical topologies advantages, many researchers have focused on new topologies with more advantages during the recent decades. A multilevel voltage source inverter topology for photovoltaic applications, with phase-opposition carrier disposition multicarrier PWM switching technique was presented in [10]. In [11], a multilevel inverter with hybrid topology based on the cascaded H-bridge converter with consideration of optimized design, capacitor voltage balancing and harmonic profile of the output waveform has been proposed. To solve the problem of series-connected diodes in the conventional diode clamped inverter, a modified diode clamped topology was proposed in which apart from the clamping of the main switches with clamping diodes, mutual clamping amongst the clamping diodes themselves is also provided in [12]. A three-phase three-level inverter with two level sub-inverters in series with each phase along with asymmetric source configuration to achieve a nine level waveform to implement a medium voltage drives application has been presented in [13]. A multilevel topology based on dual two-level voltage source inverter to obtain a multilevel waveform thereby reducing grid side current harmonics and mitigating output voltage derivatives was introduced in [14]. A modification in the configuration of cascaded H-bridge converter using an active front end to solve regenerative mode of operation problem and effective control of the input current and output voltage was presented in [15]. In [16], presentation and implementation of a cascaded multilevel boost inverter for electric vehicle and hybrid electric vehicle applications without using of inductors and multiple power supplies was given. The other important multilevel inverter topology is modular multilevel converter (MMC) [17]. MMC has become an attractive topology for medium and high-power applications because of its several advantages such as modularity and redundancy.

During recent decade, very efforts have focused on multilevel inverter topology design to reduce power switches count, which appeared in the literature [18]-[28]. In this paper, a new topology for multilevel inverters is presented. The proposed topology is formed of cascade connection of multiple multilevel strings that are constructed using series-connected basic switching units. The proposed multilevel inverter uses reduced number of switching devices. Symmetric and asymmetric configurations of proposed inverter are presented and analyzed. A comparison among the proposed multilevel inverter and similar topologies is given in detail. Finally, a laboratory scale prototype of the presented multilevel inverter is simulated and implemented, and then measurement results are given.

II. Proposed Multilevel Inverter Topology

A. *Configuration of basic switching unit*

Fig. 1(a) shows basic switching unit configuration for proposed multilevel inverter which is composed of a DC voltage source, a power transistor and a diode. The proposed basic unit has two operation modes. In these modes, the power switch and power diode operate complementary. In the first mode, when the power switch is off, the diode becomes forward biased through the DC voltage source and conducts the current. In this mode, unit voltage, V_U, is equal to zero. In the second mode, the switch is turned on, and the diode becomes reverse biased through the switch and voltage source, and then turns off.

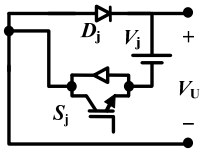


Fig. 1 (a)

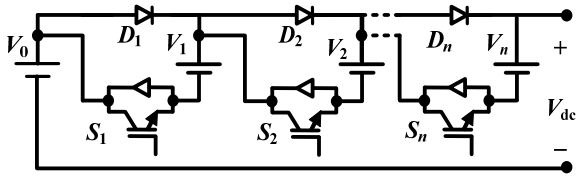


Fig. 1 (b)

Fig. 1. Configurations of (a) basic switching unit, (b) multilevel string.

In this mode, unit voltage is equal to V_j. As shown in Fig. 1(a), the diode should be able to withstand the voltage V_j .

B. *Configuration of multilevel string based on proposed basic units*

Number of series-connected basic units can be increased to raise the maximum voltage appearing in the converter output. Fig. 1(b) shows the series-connection of the basic switching units, named as a multilevel string. Operation of the multilevel string is similar to the operation of basic unit so that, if a power switch does not receive any gate pulse, its complement diode conducts. When the power switch is turned on, its complement diode becomes reverse biased and turns off. As a result, the DC voltage source of the unit is connected in series with the previous DC voltage source. Table I indicates switching states of the multilevel string.

C. *Configuration of proposed multilevel inverter*

Fig. 2 shows configuration of the proposed multilevel inverter. The proposed multilevel inverter is constructed using series-connection of suggested multilevel strings. Some changes should be applied in the given configuration to generate maximum voltage levels behind the H-bridge

converter. To get this aim, except one of the strings, all strings should be bypassed to do not produce any voltage level in some instants. Therefore, all the strings except the first one includes a bypass diode at the output, and also the diode in the first basic unit is replaced with a power switch.

TABLE I
SWITCHING STATES OF PROPOSED MULTILEVEL STRING WITH *n* NUMBER OF BASIC UNITS

State number	On-state switches	V_{dc}
1	-	V_0
2	S_1	$V_0+ V_1$
3	S_1, S_2	$V_0+ V_1+V_2$
.	.	.
.	.	.
***n*+1**	S_1, S_2,…, S_n	$V_0+ V_{1+} \ldots_+V_n$

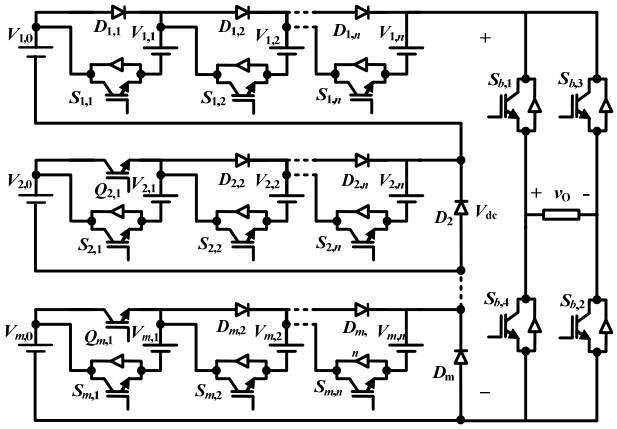


Fig. 2. Configuration of proposed multilevel inverter.

In this way, when the aforementioned switch is off, the diode bypasses the multilevel string, and when the switch is turned on, the diode is reverse biased and turns off, so the string can produce the desired voltage level in its output. In the depicted configuration, each string generates multilevel DC voltages that are added together as V_{dc}. The generated voltage is always positive. To operate as an inverter, the output voltage polarity should be changed in every half cycle. To get this aim, a conventional H-bridge converter is added to the output of the improved configuration. With consideration of the proposed multilevel inverter structure, it is realized that the generated multilevel voltage is provided using less number of power switches. As an example, equivalent circuits of each generated voltage level in positive half-cycle of 13-level output voltage are shown in Fig. 3. It is important to notice that because diodes are applied in the switching cells, the proposed multilevel inverter can only operate for unity and near unity power factor loads.

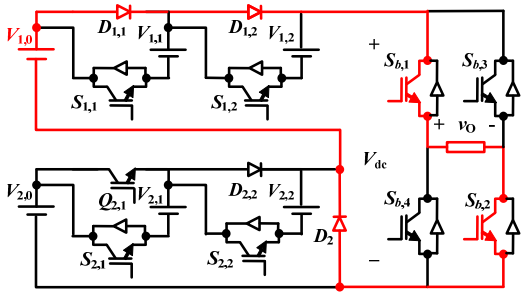


Fig. 3 (a)

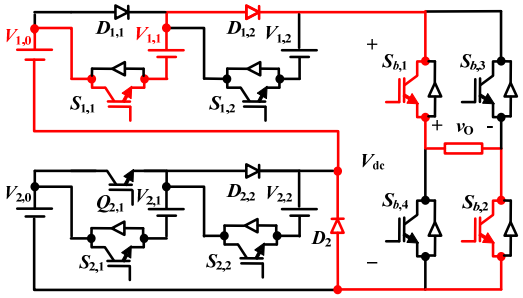


Fig. 3 (b)

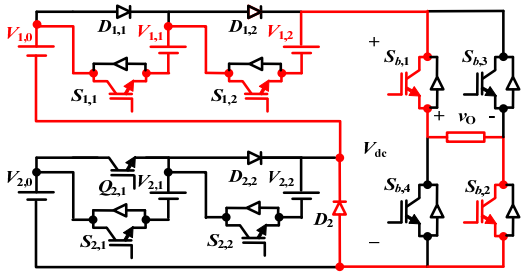


Fig. 3 (c)

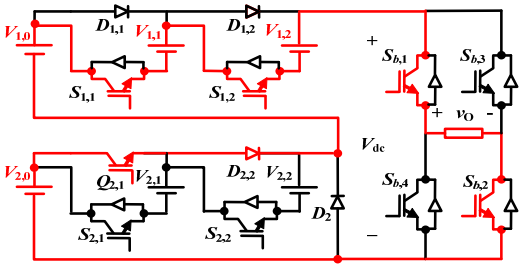


Fig. 3 (d)

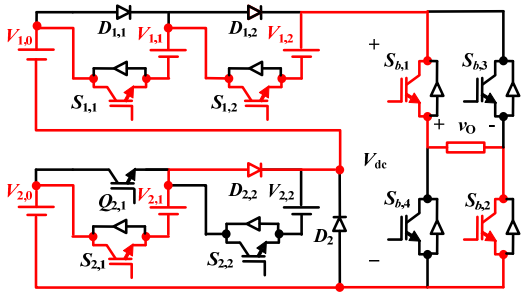


Fig. 3 (e)

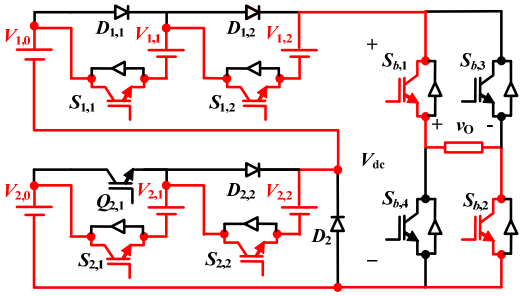


Fig. 3 (f)

Fig. 3. Equivalent circuits of each generated voltage level in positive half-cycle of 13-level output voltage, (a) equivalent circuit of $V_{1,0}$ voltage level, (b) equivalent circuit of $V_{1,0} + V_{1,1}$ voltage level, (c) equivalent circuit of $V_{1,0} + V_{1,1} + V_{1,2}$ voltage level, (d) equivalent circuit of $V_{1,0} + V_{1,1} + V_{1,2} + V_{2,0}$ voltage level, (e) equivalent circuit of $V_{1,0} + V_{1,1} + V_{1,2} + V_{2,0} + V_{2,1}$ voltage level, (f) equivalent circuit of $V_{1,0} + V_{1,1} + V_{1,2} + V_{2,0} + V_{2,1} + V_{2,2}$ voltage level.

III. Symmetric and Asymmetric Configurations of Proposed Multilevel Inverter

A. Symmetric configuration

In determination of magnitude of DC voltage sources for a multilevel inverter, it should be noted that all of the voltage steps should be generated in the converter output using available voltage sources. The proposed inverter can have symmetric configuration such that all of the DC voltage sources have equal values. For n number of basic units in each multilevel string, and m number of multilevel strings, the number of output voltage steps is equal to Equ. (1). Switching states of symmetric configuration in positive half-cycle is given in Table II.

$$N_{Level} = 2m(n+1)+1 \quad m \geq 1, \quad n \geq 1 \tag{1}$$

The number of required diodes, n_D, and power switches, n_{Sw}, to generate a multilevel voltage with N_{step} steps are given in Equ. (2) and Equ. (3).

$$n_D = \frac{N_{Level}-1}{2} - m, \quad N_{Level} \geq 5 \tag{2}$$

$$n_{Sw} = \frac{N_{Level}-1}{2} + 3 \quad m \geq 2, \quad N_{Level} \geq 5 \tag{3}$$

Voltage and current ratings of switches are important factors in the cost and size of inverter implementation. In the multilevel inverters, the switches current rating is equal to load current that is supplied. However, it is different for voltage ratings. Total blocking voltage (TBV) of the suggested topology is calculated as given in Equ. (4).

$$TBV = [5m(n+1)-1]V \tag{4}$$

TABLE II
SWITCHING STATES OF PROPOSED MULTILEVEL INVERTER WITH SYMMETRIC CONFIGURATION FOR POSITIVE HALF-CYCLE

State number	Basic units on-state switches	V_{dc}
1	-	$1V$
2	$S_{1,1}$	$2\ V$
3	$S_{1,1}$, $S_{1,2}$	$3\ V$
4	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$	$4\ V$
. . .	. . .	. . .
***n*+1**	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$,	$(n+1)V$
***n*+2**	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $Q_{2,1}$	$(n+2)V$
***n*+3**	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $S_{2,1}$	$(n+3)V$
. . .	. . .	. . .
2(*n*+1)	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $S_{2,1}$..., $S_{2,n}$	$2(n+1)V$
. . .	. . .	. . .
***m*(*n*+1)**	$S_{1,1}$, ..., $S_{1,n}$, $S_{2,1}$..., $S_{2,n}$,... $S_{m,1}$,... $S_{m,n}$	$m(n+1)V$

B. Asymmetric configuration

Using unequal values for inverter DC voltage sources, it is possible to get more voltage steps in the inverter output. To get the maximum number of voltage steps using minimum number of basic units beside the generation of all voltage steps, two different design methods are presented as given in the following.

***First design method*:** In the first design method, magnitude of the first DC voltage source, V_0, and voltage source of the first unit, V_1, is equal to V, and the value of the rest of DC voltage sources is equal to $2V$. The algorithm is given in Equ. (5). Table III indicates switching states of asymmetric configuration with first design method in positive half-cycle.

$$V_{i,j} = \begin{cases} V & j=1, \quad i=1,2 \\ 2V & j=1, \quad i=3,...,n \\ 2V & j \neq 1, \quad i=1,...,n \end{cases} \tag{5}$$

With applying of this design method for the magnitude of voltage sources, the number of inverter output voltage steps is achieved as given in Equ. (6).

$$N_{Level} = 4m(n+1) - 3 \tag{6}$$

In this method, the total numbers of diodes and switches to generate N_{step} steps in the output voltage are obtained as follow:

$$n_D = \frac{N_{Level}+3}{4} - m, \quad m \geq 2, N_{Level} \geq 5 \tag{7}$$

$$n_{Sw} = \frac{N_{Level}+3}{4} + 3, \quad N_{Level} \geq 5 \tag{8}$$

The voltage rating of the first switch, S_1, is equal to V, and voltage rating of the rest of switches is equal to $2V$.

TABLE III
SWITCHING STATES OF PROPOSED MULTILEVEL INVERTER WITH FIRST DESIGN METHOD ASYMMETRIC CONFIGURATION IN POSITIVE HALF-CYCLE

State number	Basic units on-state switches	V_{dc}
1	-	V
2	$S_{1,1}$	$2V$
3	$S_{1,2}$	$3V$
4	$S_{1,1}$, $S_{1,2}$	$4V$
. . .	. . .	. . .
2*n*	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$,	$2nV$
2(*n*+1)	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $Q_{2,1}$	$2(n+1)V$
2(*n*+2)	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $S_{2,1}$	$2(n+2)V$
. . .	. . .	. . .
(4*n*+2)	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $S_{2,1}$..., $S_{2,n}$	$(4n+2)V$
. . .	. . .	. . .
2*m*(*n*+1)-2	$S_{1,1}$, ..., $S_{1,n}$, $S_{2,1}$...., $S_{2,n}$,... $S_{m,1}$,... $S_{m,n}$	$[2m(n+1)-2]V$

Total blocking voltage of the designed configuration is calculated as given in Equ. (9):

$$TVR = [10(mn + m - 1) - 1]V \tag{9}$$

***Second design method*:** In the second design method for asymmetric configuration of the proposed multilevel inverter, the magnitude of the first three DC voltage sources are equal to V, and the magnitude of the rest of DC voltage sources are equal to $3V$, that is given in Equ. (10). Table IV gives switching states of asymmetric configuration with second design method in positive half-cycle.

$$V_{i,j} = \begin{cases} V & j = 1, \quad i = 1,2,3 \\ 3V & j = 1, \quad i = 4,...,n \\ 3V & j \neq 1, \quad i = 1,...,n \end{cases} \tag{10}$$

Using the mentioned design method to determine the magnitude of DC voltage sources, the number of output voltage steps is equal to Equ. (11).

$$N_{Level} = 6(mn + m - 2) + 1, \quad n \geq 1 \tag{11}$$

The required numbers of diodes and switches, to produce N_{step} steps in the output voltage are calculated using Equ. (12) and Equ. (13).

$$n_D = \frac{N_{Level}+11}{6} - m, \quad m \geq 2, \quad N_{Level} \geq 5 \tag{12}$$

$$n_{sw} = \frac{N_{Level}-1}{6} + 5, \quad N_{Level} \geq 5 \tag{13}$$

TABLE IV
SWITCHING STATES OF PROPOSED MULTILEVEL INVERTER WITH SECOND DESIGN METHOD ASYMMETRIC CONFIGURATION IN POSITIVE HALF-CYCLE

State number	Basic units on-state switches	V_{dc}
1	-	V
2	$S_{1,1}$	$2V$
3	$S_{1,1}$, $S_{1,2}$	$3V$
4	$S_{1,3}$	$4V$
. . .	. . .	. . .
3(*n*-1)	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$,	$3(n-1)V$
3*n*	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $Q_{2,1}$	$3nV$
3(*n*+1)	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $S_{2,1}$	$3(n+1)V$
. . .	. . .	. . .
6*n*	$S_{1,1}$, $S_{1,2}$, $S_{1,3}$, ..., $S_{1,n}$, $S_{2,1}$..., $S_{2,n}$	$6nV$
. . .	. . .	. . .
3[*m*(*n*+1)-2]	$S_{1,1}$, ..., $S_{1,n}$, $S_{2,1}$...., $S_{2,n}$,... $S_{m,1}$,... $S_{m,n}$	$3[m(n+1)-2]V$

The voltage rating of the first and second switches, S_1 and S_2 is equal to V, and voltage rating of the rest of switches is equal to $3V$. Total blocking voltage of the studied configuration is given in Equ. (14).

$$TBV = [15(mn + m - 2) - 1]V \tag{14}$$

IV. CALCULATION OF POWER LOSS

Power losses of the switches in a multilevel inverter mainly include conduction loss and switching loss [29]. In the low switching frequencies, the conduction losses are dominant. However, in the high switching frequencies, the switching losses become considerable. For a transistor with the anti-parallel diode, both the transistor and the diode have on-state resistance and on-state voltage which cause conduction losses. Although, transistor and the diode on-state resistance and on-state voltage vary with temperature and can be considered constant to simplify analysis. Assume that the on-state voltages of the diode and transistor are V_T and V_D, respectively and their resistances are considered to be R_T and

R_D, respectively. Instantaneous conduction loss of a diode, $P_{c,D}(t)$, and a transistor, $P_{c,T}(t)$, can be written as follow:

$$p_{c,T}(t) = [V_T + R_T i^{\beta}(t)]i(t) \tag{15}$$

$$p_{c,D}(t) = [V_D + R_D i(t)]i(t) \tag{16}$$

where β is constant of the transistor, $i(t)$ is the instantaneous current through the transistor or diode. Considering that at the instant of t, there are N_T transistors and N_D diodes in the current path, the average value of the conduction power loss, P_c, of the multilevel inverter can be written as follows:

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} [N_T(t)p_{c,T}(t) + N_D(t)p_{c,D}(t)]dt \tag{17}$$

To calculate the switching losses of the multilevel inverter, the energy lost during turn-on and turn-off period of a switch is calculated, and then it is extended for the multilevel inverter. Suppose that the voltage and current of a switch vary linearity during switching. Using this approximation, the lost energy during turn-on and turn-off period of a switch can be obtained as follow:

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,k} I\, t_{off} \tag{18}$$

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6}V_{sw,k} I'\, t_{on} \tag{19}$$

where, $E_{on,k}$ and $E_{off,k}$ are the lost energy during turn on and turn off period of the switch k, and t_{on} and t_{off} are the turn-on and turn-off times of the switch. Also, $V_{sw,k}$ is the voltage on the switch k before turning on or after turning off. I and I' are the currents through the switch k before turning off and after turning on, respectively. For the multilevel inverter, the switching power loss, P_{sw}, is equal to the sum of all turn-on and turn-off energy losses in a fundamental cycle of the output voltage. This can be written as follows:

$$P_{sw} = f\sum_{k=1}^{N_{switch}}\left(\sum_{i=1}^{N_{on,k}} E_{on,ki} + \sum_{i=1}^{N_{off,k}} E_{off,ki}\right) \tag{20}$$

where f is the fundamental frequency, $N_{on,k}$ and $N_{off,k}$ are the numbers of turn-on and turn-off of the switch k during a fundamental cycle. Also, $E_{on,ki}$ is the energy loss of the switch k during the i^{th} turn-on, and $E_{off,ki}$ is the energy loss of the switch k during the i^{th} turn-off. The total power loss of the multilevel inverter, P_{loss}, is equal to the sum of the conduction and switching losses as given in Equ. (21).

$$P_{loss} = P_c + P_{sw} \tag{21}$$

V. Comparison Study

Beside the conventional multilevel inverter topologies, some of new topologies have been presented to reduce the number of semiconductor devices. In this section, symmetric and asymmetric configurations of the proposed multilevel inverter are compared with each other. Also, the symmetric configuration is compared with similar appearing symmetric CHB multilevel inverter and presented topologies in [30]-[32]. For comparison studies, three important factors include the number of switches, TBV of switches, and the inverter total power losses are considered.

A. *Comparison of symmetric and asymmetric configurations of proposed multilevel inverter*

In this subsection, characteristics of symmetric and asymmetric configurations of proposed multilevel inverter are compared. Maximum number of steps in output voltage, N_{step}, versus number of multilevel strings, m, for symmetric and first design (FD) and second design (SD) methods of asymmetric configurations are shown in Fig. 4(a). This figure shows when the number of multilevel strings is increased, the increase in number of output voltage steps is remarkable for asymmetric configuration with second design method. Fig. 4(b) shows the number of power switches, n_{sw}, versus number of output voltage steps. It is clear that the symmetric configuration needs the most number of power switches for a specified number of voltage steps, and asymmetric configuration with second design method needs the least. Comparison result of switches TBV is given in Fig. 4(c).

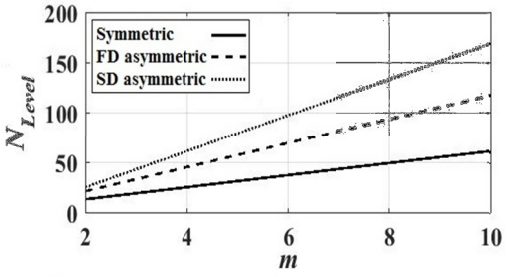


Fig. 4 (a)

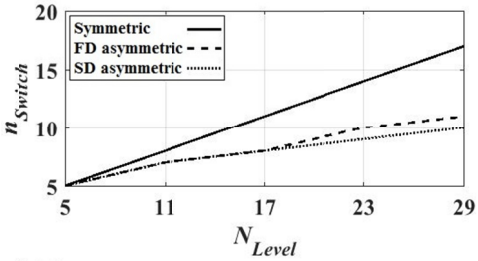


Fig. 4 (b)

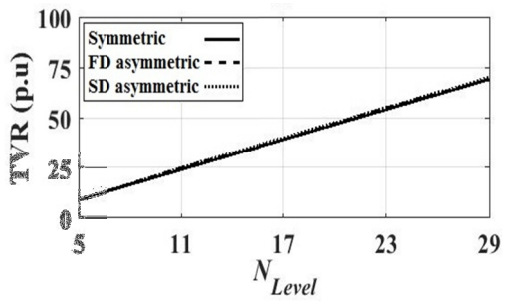


Fig. 4 (c)

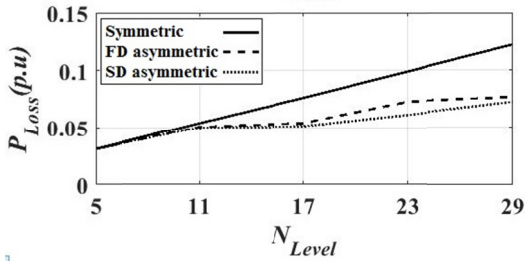


Fig. 4 (d)

Fig. 4. Comparison of (a) number of output voltage steps versus number of multilevel strings, *m*, (b) number of power switches versus output voltage steps, (c) total blocking voltage versus output voltage steps, (d) total power losses versus output voltage step, in symmetric and asymmetric configurations of proposed multilevel inverter.

This figure indicates that with increasing of inverter output voltage steps, TBV of symmetric and asymmetric configurations are almost similar. The power losses, P_{Loss}, versus the number of output voltage steps for symmetric and asymmetric topologies are shown in Fig. 4(d). This figure indicates that as the number of output voltage steps are increased, the total power losses of all three configurations are increased. It is clear that the power losses of symmetric configuration are higher than two asymmetric configurations, and between two asymmetric configurations the second design method asymmetric configuration has lower power losses.

B. *Comparison of symmetric configuration of proposed multilevel inverter with similar topologies*

In this subsection, characteristics of symmetric configuration of the proposed multilevel inverter are compared with symmetric configurations of CHB multilevel inverter and topologies presented in [30]-[32]. The number of switches for the suggested symmetric configuration is calculated using Equ. (3). For the CHB and the studied topologies, the numbers of switches in terms of number of output voltage steps are achieved as follow:

$$n_{switch,CHB} = 2(N_{step} - 1) \tag{22}$$

$$n_{switch,[30]} = N_{step} + 3 \tag{23}$$

$$n_{switch,[31]} = N_{step} + 3 \tag{24}$$

$$n_{switch,[32]} = N_{step} + 1 \tag{25}$$

Fig. 5(a) shows the number of inverters switches versus the number of output voltage steps. As indicated in this figure, the proposed topology uses less number of switches in comparison with the other topologies. Reduction in number of switches reduces the number of required driver circuits for the switches and also reduces complexity of inverter. The TBV on the switches of multilevel inverter is another important factor that should be compared for different topologies. The normalized TBV on the switches for the proposed topology is calculated using Equ. (4), and for the other topologies are calculated as given in the following.

$$\frac{TBV_{CHB}}{V_{dc}} = 2N_{step} - 1 \tag{26}$$

$$\frac{TBV_{[30]}}{V_{dc}} = 3N_{step} - 1 \tag{27}$$

$$\frac{TBV_{[31]}}{V_{dc}} = \begin{cases} \frac{1}{32}(3N_{step}^2 + 74N_{step} - 25), \\ N_{step} = 2k + 1 \\ \frac{1}{32}(3N_{step}^2 + 74N_{step} - 29), \\ N_{step} = 2k, \frac{N_{step}}{2} = 2k + 1 \\ \frac{1}{32}(3N_{step}^2 + 74N_{step} - 45), \\ N_{step} = 2k, \frac{N_{step}}{2} = 2k \end{cases} \tag{28}$$

$$\frac{TVR_{[32]}}{V_{dc}} = \begin{cases} \frac{1}{16}(3N_{step}^2 + 26N_{step} - 13), N_{step} = 2k \\ \frac{1}{16}(3N_{step}^2 + 26N_{step} - 9), N_{step} = 2k + 1 \end{cases} \tag{29}$$

Fig. 5(b) shows comparison result of the normalized TBV on the switches of discussed topologies. As indicated in this figure, after the CHB multilevel inverter, the proposed topology has lower TBV in comparison with the other topologies. To compare the total power losses of the discussed multilevel inverters, their per unit power losses versus the output voltage steps are shown in Fig. 5(c). For the power losses calculation, the circuit elements data are: V_T=2.5 V, V_D=1.5 V, R_T=0.15 Ω, R_D=0.15 Ω, β=1, t_{on}=t_{off}=2 μs. The comparison has been performed according to RMS phase

voltage of 220 V and 200 W load. The results verify acceptable power losses of the proposed multilevel inverter in comparison with similar topologies.

C. *Calculation of component count per level factor*

Another important factor for comparison study is the components per level factor (F_{cl}). This factor indicates total elements number of a converter for generation of a specified voltage level. F_{cl} factor is defined as given in Equ. (30).

$$F_{cl} = \frac{n_{Sw} + n_D + n_C + n_{DC} + n_{Tsf} + n_{Drv}}{N_{Level}} \quad (30)$$

where n_{Sw}, n_D, n_C, n_{DC}, n_{Tsf}, $n_{Drv,}$ and N_{Level} indicate number of switches, diodes, capacitors, DC sources, transformers, driver and number of voltage level per phase, respectively. The comparison is performed among the proposed multilevel inverter topology, CHB multilevel inverter and topologies presented in [30]-[32] for n=2. Table V shows the required components number of studied topologies and their corresponding F_{cl} value. From the comparison results, it is clear that for the intended voltage levels, the proposed topology requires less number of components in comparison to the other topologies.

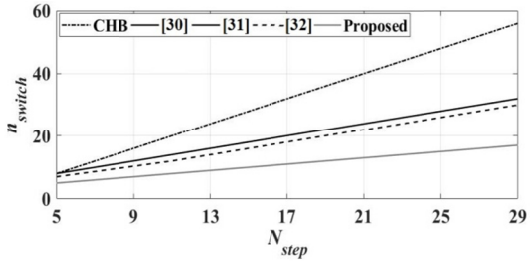


Fig. 5 (a)

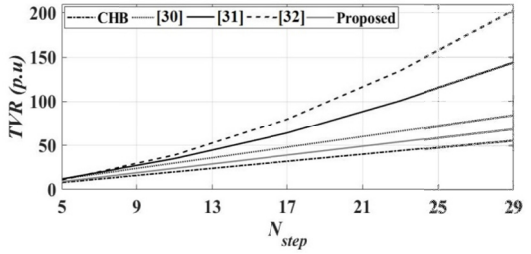


Fig. 5 (b)

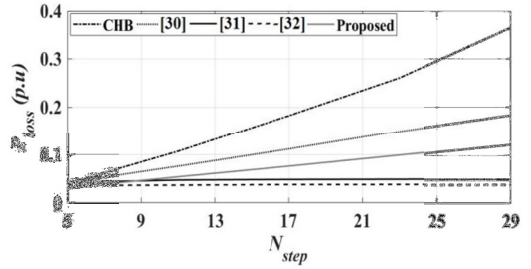


Fig. 5 (c)

Fig. 5. Comparison of characteristics of proposed multilevel inverter with similar topologies, (a) number of power switches, n_{sw}, (b) total blocking voltage, TBV, and (c) total power losses, P_{Loss}, versus output voltage step, $N_{step,}$ for n=2.

VI. Simulation and Experimental Results

Simulation and experimental tests are performed to verify operation of the proposed multilevel inverter. The proposed multilevel inverter with two multilevel strings and three basic units in each strings (m=2 and n=3) is simulated in MATLAB/SIMULINK, and implemented as a laboratory-scale prototype. The structure of the simulated and implemented converter is indicated in Fig. 6(a) and Fig. 6(b). All tests are performed under resistive-inductive load with R=150Ω and L=70mH. In the implemented prototype, IRFP450 Power MOSFETs and 1N5408 diode are used.

TABLE V
COMPONENTS COUNT AND COMPONENTS PER LEVEL FACTOR OF STUDIED MULTILEVEL INVERTERS

N_{Level}	Topology	n_{Sw}	n_D	n_C	n_{DC}	n_{Tsf}	n_{Drv}	n_X	F_{cl}
5	CHB	8	0	0	2	0	8	0	3.6
	[30]	8	0	0	2	0	8	0	3.6
	[31]	8	0	0	2	0	8	0	3.6
	[32]	7	0	0	2	0	7	0	3.2
	Proposed	5	1	0	2	0	5	0	2.6
9	CHB	16	0	0	4	0	16	0	4
	[30]	12	0	0	4	0	12	0	3.11
	[31]	12	0	0	4	0	10	0	2.88
	[32]	10	0	0	4	0	10	0	2.66
	Proposed	7	3	0	4	0	7	0	2.33
13	CHB	24	0	0	6	0	24	0	4.15
	[30]	16	0	0	6	0	16	0	2.92
	[31]	16	0	0	6	0	12	0	2.61
	[32]	14	0	0	6	0	14	0	2.61
	Proposed	9	4	0	6	0	9	0	2.15
17	CHB	32	0	0	8	0	32	0	4.23
	[30]	20	0	0	8	0	20	0	2.82
	[31]	20	0	0	8	0	14	0	2.47
	[32]	18	0	0	8	0	18	0	2.58
	Proposed	11	5	0	8	0	11	0	2.05
21	CHB	40	0	0	10	0	40	0	4.28
	[30]	24	0	0	10	0	24	0	2.76
	[31]	24	0	0	10	0	16	0	2.38
	[32]	22	0	0	10	0	22	0	2.57
	Proposed	13	7	0	10	0	13	0	2.04
25	CHB	48	0	0	12	0	48	0	4.32
	[30]	28	0	0	12	0	28	0	2.72
	[31]	28	0	0	12	0	18	0	2.32
	[32]	26	0	0	12	0	26	0	2.56
	Proposed	15	8	0	12	0	15	0	2
29	CHB	56	0	0	14	0	56	0	4.34
	[30]	32	0	0	14	0	32	0	2.68
	[31]	32	0	0	14	0	20	0	2.27
	[32]	30	0	0	14	0	30	0	2.55
	Proposed	17	9	0	14	0	17	0	1.96

In order to generate required voltage steps, a proper algorithm for inverter switching should be applied. The generated output voltage should have all steps and minimum total harmonic distortion (THD). In order to have equal size for all voltage steps, fundamental and other harmonic components are obtained from Equ. (31) [33].

$$H_n = \begin{cases} \frac{4V}{n\pi}\sum_{j=1}^{S}\cos(n\alpha_j) & n = 2k+1 \\ 0 & n = 2k \end{cases} \quad (31)$$

where V is the amplitude of each voltage step, S is the number of steps, and a_j is the optimized harmonic switching angles. The angles α_j are expressed using the following equation:

$$\alpha_j = \sin^{-1}\left(\frac{j-0.5}{S}\right) \quad j = 1,2,...,S \quad (32)$$

Using the above algorithm, THD of the output voltage is equal to Equ. (33).

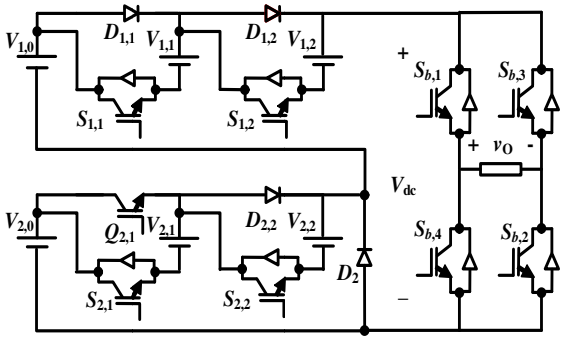


Fig. 6 (a)

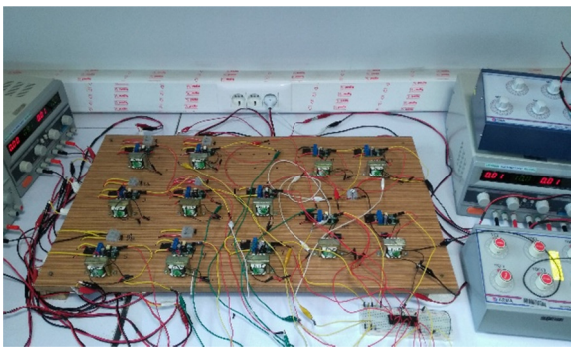


Fig. 6 (b)

Fig. 6. Structure of (a) simulated and (b) implemented multilevel inverter, with 2 multilevel strings, *m*=2, and three basic units in each strings, *n*=3.

$$THD = \frac{\sqrt{\sum_{n=3,5}^{\infty} V_n^2}}{V_1} = \sqrt{\left(\frac{V_O}{V_1}\right)^2 - 1} \quad (33)$$

where

$$V_O = \frac{2\sqrt{2}V_{dc}}{\pi}\sqrt{\sum_{n=1,3,5,..}^{\infty}\left(\sum_{j=1}^{S}\frac{\cos(n\alpha_j)}{n}\right)^2} \quad (34)$$

$$V_1 = \frac{2\sqrt{2}V_{dc}}{\pi}\sum_{j=1}^{S}\cos\alpha_j \quad (35)$$

where V_O is the RMS value of output voltage, and V_n is the RMS value of n^{th} harmonic component of output voltage.

Offline switching pattern is applied for generation of gate signals that is shown in Fig. 7(a). A switching table is provided in the EPROM memory of the microcontroller, and data of the switching states and the obtained switching angles are sent to the microcontroller port. Fig. 7(b) shows the isolator and driver circuit of each switch. This circuit consists of an opto-isolator, a Schmit trigger, and a buffer. Each switch requires an isolated driver circuit. The isolation can be provided using either pulse transformers or opto-isolators. Opto-isolators can work in a wide range of input signal pulse width, but a separate isolated power supply is required for each switching device.

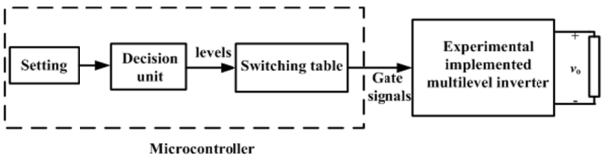


Fig. 7 (a)

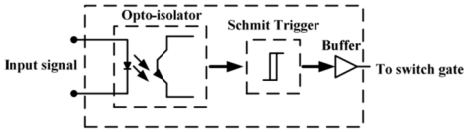


Fig. 7 (b)

Fig. 7. (a) Structure of applied pattern for generation of gate signals, (b) gate driver circuit of switches.

The opto-isolator based gate driver circuit is used in the prototype inverter.

Fig. 8 shows simulation and experimental measurement results of output voltage and current waveforms of symmetric configuration of proposed multilevel inverter. The generated voltage has 13 levels, and since the load of the converters is almost a low-pass filter (*R–L*), the output current contains less high-order harmonics than the output voltage. Fig. 9 depicts FFT analysis of the output voltage and current of proposed 13-level inverter. THD of voltage is limited to 6.44%. Also, its related current THD is 2.12%.

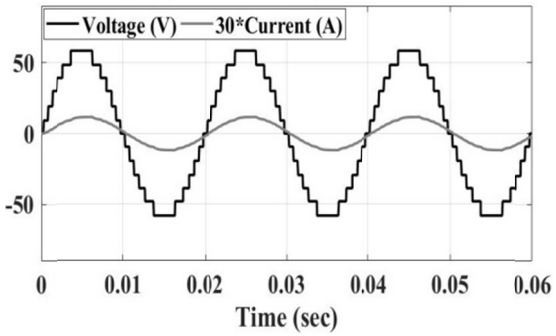


Fig. 8 (a)

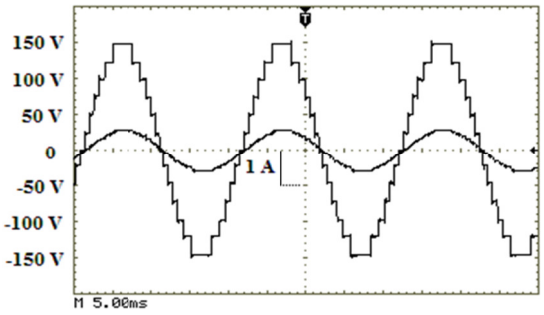


Fig. 8 (b)

Fig. 8. (a) Simulation and (b) experimental measurement results of proposed 13-level output voltage and current.

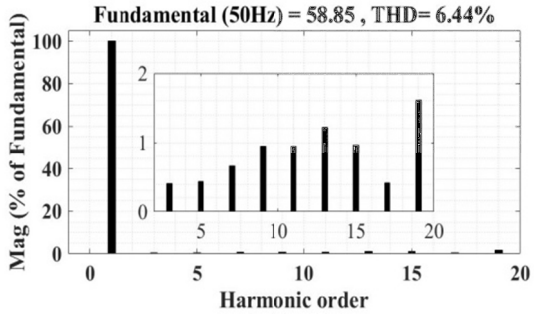


Fig. 9 (a)

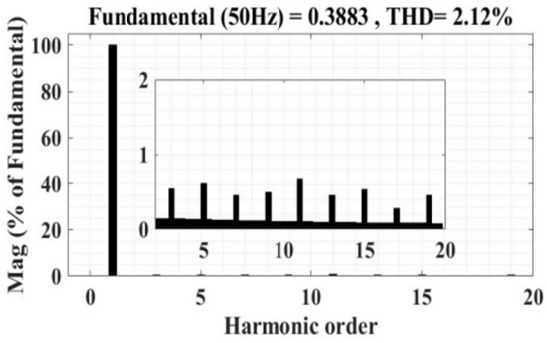


Fig. 9 (b)

Fig. 9. Proposed 13-level inverter; (a) FFT analysis of the output voltage, and (b) FFT analysis of the output current.

In the second study, the implemented inverter is set to asymmetric configuration with first design method, and generates 21-level output voltage. Fig. 10 shows simulation and experimental measurement results of 21-level output voltage and its related current waveforms. FFT analysis of the output voltage and current of 21-level inverter are given in Fig. 11. Output voltage THD is 3.95% and its related current THD is limited to 1.76% that is in range of IEEE519 standard. Operation of asymmetric configuration with second design method is considered as third study. According to presented algorithm in the second design method, output voltage is generated with 25 separated steps. Fig. 12 shows simulation and experimental measurement results of voltage and current of studied configuration. Also, FFT analysis of 25-level output voltage and its related current is indicated in Fig. 13. Output voltage THD is 3.51% and its related current THD is 1.73%, which are acceptable values. Clearly, waveforms of the second and third tests have better quality than the first test from harmonic spectrum point of view.

As shown in these figures, the results verify the ability of the suggested converter in generation of desired multilevel voltage waveforms. However, the main demerit of the proposed multilevel inverter is its limitation in providing the low power factor loads where some spikes are created in the generated multilevel voltage. Therefore, the proposed multilevel inverter is applicable for loads with unity or near unity power factor loads such as in UPS for home appliances, banks or hospitals emergency electric power.

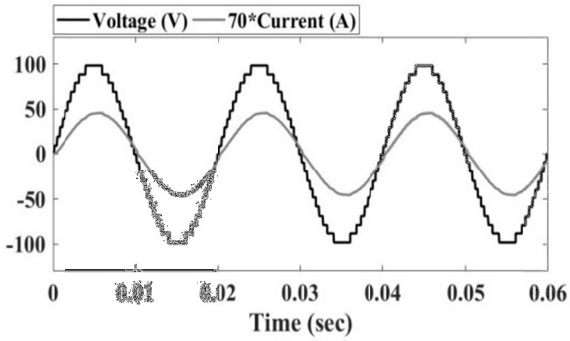


Fig. 10 (a)

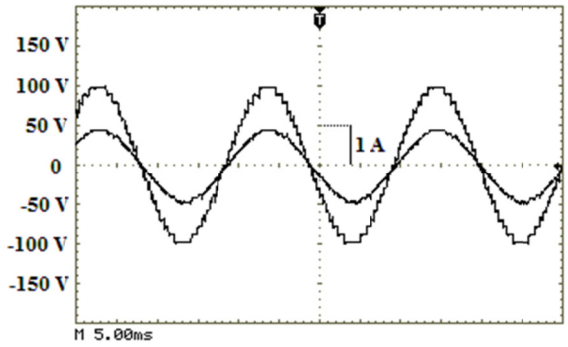


Fig. 10 (b)

Fig. 10. (a) Simulation and (b) experimental r measurement esults of proposed 21-level output voltage and current.

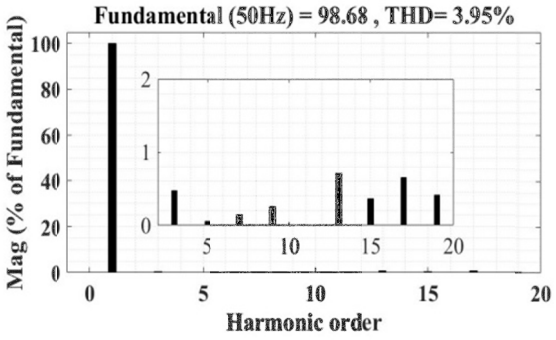


Fig. 11 (a)

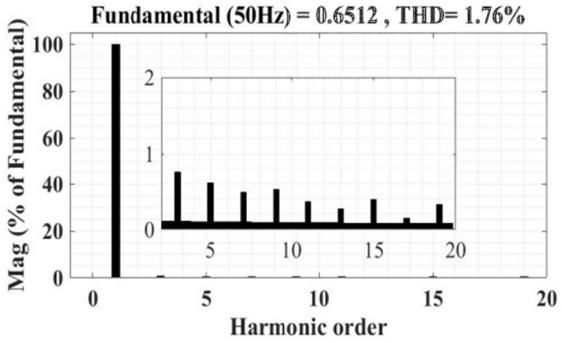


Fig. 11 (b)

Fig. 11. Proposed 21-level inverter; (a) FFT analysis of the output voltage, and (b) FFT analysis of the output current.

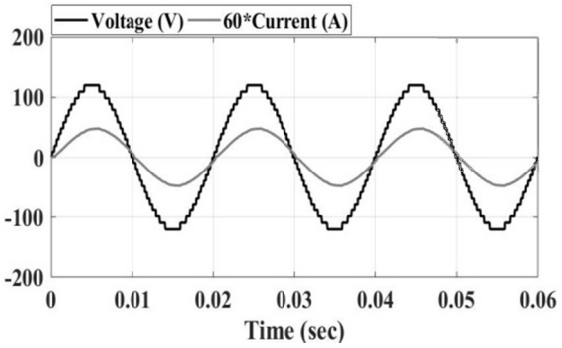


Fig. 12 (a)

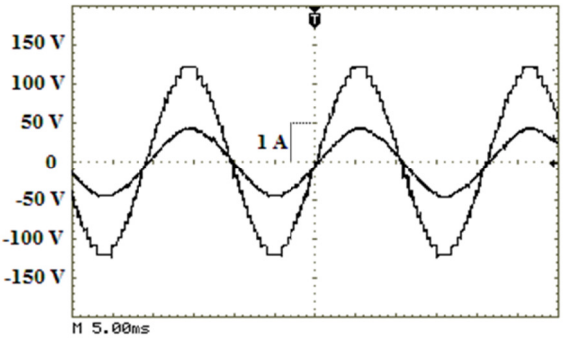


Fig. 12 (b)

Fig. 12. (a) Simulation and (b) experimental measurement results of proposed 25-level; output voltage and current.

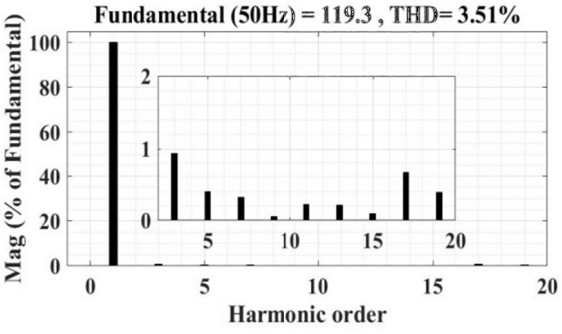


Fig. 13 (a)

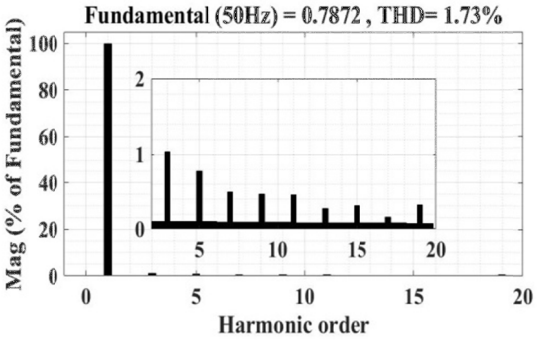


Fig. 13 (b)

Fig. 13. Proposed 25-level inverter; (a) FFT analysis of the output voltage, and (b) FFT analysis of the output current.

VII. CONCLUSIONS

A new configuration of multilevel inverters has been presented in this paper. The proposed multilevel inverter has the capability of extension to generate more number of levels in output voltage. The inverter can be designed both in symmetric and asymmetric configurations. Two different methods for determination of magnitude of DC voltage sources have been proposed. Comparison results show that the asymmetric configuration with second design method needs less number of elements and has less power losses for a specified voltage level than symmetric and first design method asymmetric configurations. Also, the symmetric configuration of the proposed multilevel inverter requires the least number of power switches, and also has acceptable power losses in comparison with conventional CHB multilevel inverter and similar topologies presented in [30-32]. A prototype of the suggested multilevel inverter with symmetric and two asymmetric configurations has been simulated and implemented. Simulation and experimental measurement results have validated acceptable performance of the multilevel inverter.

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