

Efficiency improvement and inrush current reduction in a non-isolated DC-DC converter

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A B S T R A C T | *DC-DC boost converters are unable to provide high step-up voltage gains due to the effect of power switches, rectifier diodes, and the equivalent series resistance of inductors and capacitors. A high step-up DC-DC converter based on the modified SEPIC converter is presented in this paper. Step up non-isolated converters generally suffer from problems such as high voltage stress and low efficiency. In this study, non-isolated boost converter structures, SEPIC, SEPIC modified circuit, and a proposed converter is studied. Then compare the performance of these typologies is located and presented as a chart. The operation analysis, design procedure for proposed converter is obtained from 15V input voltage and 150V output voltage and with 100 watts output power. Using the proposed converter, the input inrush current and the invading voltage of the output have decreased. The time response analysis states that the proposed converter acts faster with deployment time than other converters.*

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1. INTRODUCTION

Due to the limited fossil fuel sources and pollution caused by its use, the concept of using clean and renewable energy sources has been proposed in recent years. Photovoltaic systems with a clearer vision, high reliability, low operating cost, Eco-friendly and easier maintenance of renewable energy has been more attention [1]. One of the weaknesses of solar cells is the low efficiency (equivalent to 5 to 20 percent) that is directly converted into electricity [2]. The low voltage produced by the solar cells, the need for series and parallel to them, to reach a relatively high voltage in modules is mandatory Demand for high-static DC-DC converters for some applications, powered by a low voltage DC source such as renewable energy sources, fuel cells, embedded systems, portable electronic equipment, emergency power supplies and battery systems are ever increasing [3, 4]. When some loads

works with DC or AC voltage ratio higher than ten times the input source voltage, it is called a high voltage step [5]. In order to achieve high voltage and increase the efficiency of systems, the use of high-power DC-DC converters is inevitable. Some of the problems of converting low voltage to high voltage are considered in the use of DC-DC converters include low input voltage, high inrush current and increased static gain. Boost converter, a non-isolated ordinary DC-DC converter with limited static gain and high voltage switching stress is used in ref. [6]. Despite the dependent elements same as the inductor and the capacitor in the converters, there is a limitation in increasing the voltage gain. The switch (MOSFET) is placed in a conventional boost converter under intense voltage stress, and the use of a high-level switch is inevitable and ultimately leads to high losses. Also, when the diode is reversed, a high voltage stress occurs in it [7, 8]. Although conventional SEPIC converter switch is more stress, but it can deliver the output with the same input polarity [9]. The modified SEPIC converter has twice the static gain compared to the normal boost converter, and the switching voltage is half the value of the output voltage [10-12]. In [12],

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a converter with a high static gain and reduced switching stress is proposed based on the design of the SEPIC converter. With faster deployment time and maximum output voltage in less time, reduces the input current to the inductor. In this paper, a DC-DC converter is provided by adding an inductor to the proposed converter [12]. Using the proposed converter, the input inrush current and the invading output voltage have been decreased. The time response analysis states that at in the input and output constant voltage, the proposed converter operates faster with deployment time than other converters considered in this paper. The structure of the paper is as follows: In section II, different structure of the DC-DC converter is shown. In section III, a new structure of DC-DC converter is proposed. In section IV, the simulation and results of the research are presented. Section V concludes this paper.

II. DC-DC CONVERTERS

The Boost converter is a conventional step-up converter, which is used in high voltage applications. An example of this converter is shown in Figure 1(a) [12]. The boost converter switch is turned on for a long time because it use of the high duty cycle, which increases the switching losses. The switch stress and inrush current are also high in the conventional boost converter [13].

For the Boost converter, the values are calculated as [14]:

$$D = 1 - \frac{V_{in}}{V_{out}} \quad (1)$$

$$L_1 = \frac{V_{in} D}{\Delta i_L f} \quad (2)$$

$$C_o = \frac{D}{R \left(\frac{\Delta V_{out}}{V_{out}} \right) f} \quad (3)$$

f is the switching frequency, L_1 is the inductance and R is the load resistance. V_{in} is input voltage and V_{out} is the output voltage of the inverter. Capacitor C_o , which is effective in reducing the output ripple. Δi_L and ΔV_{out} are inductance current ripple and output voltage ripple respectively. Classic SEPIC conversion circuit is shown in Figure 1(b). Which is an increasing and decreasing converter. The SEPIC static gain range is an interesting feature of this converter. The switch voltage is equal to the amount of input and output voltage and the inrush current is lower than that of the boost converter [5], but the stress of the switch voltage is high [12]. The values for the SEPIC converter are calculated as [14]:

$$D = \frac{V_{out}}{V_{out} + V_{in}} \quad (4)$$

$$L_1 = \frac{V_{in} D}{\Delta i_{L1}} \quad (5)$$

$$L_2 = \frac{V_{in} D}{\Delta i_{L2}} \quad (6)$$

$$C_1 = \frac{D}{R \left(\frac{\Delta V_{C1}}{V_{out}} \right) f} \quad (7)$$

$$C_o = \frac{D}{R \left(\frac{\Delta V_{out}}{V_{out}} \right) f} \quad (8)$$

L_1 and L_2 are the inductors and C_1 and C_o are capacitors of the SEPIC converter. The modification of the SEPIC converter is done by inserting the diode D_M and the capacitor C_M (Figure 1(c)). Many of the functional features of the SEPIC converter are changed with the proposed modifications. Capacitor C_M is charged with the output voltage of classic boost converter. Therefore, the voltage applied to the inductor L_2 during the conduction of the power switch is greater than the classic SEPIC and increases static gain. Voltage polarity of the capacitor C_s in the proposed converter is reversed [5] and [12]. The static gain doubles and the switching voltage drops to the half of the boost converter value. The inrush current flows at the start of the converter, in the inductor L_1 , and to reduce it, a large input inductor is required. This causes soft switching operation to switch on and off for all low input voltages. C_o in the SEPIC converter, the Boost converter and the modified SEPIC (Figure 1(c)) converter is equal. Other values for the modified SEPIC (Figure 1(d)) converters are calculated as follows:

$$D = \frac{V_{out} - V_{in}}{V_{out} + V_{in}} \quad (9)$$

$$L_1 = L_2 = \frac{V_{out} D}{\Delta i_L f} \quad (10)$$

$$C_s = C_M = \frac{I_{out}}{\Delta V_c f} \quad (11)$$

$$\Delta V_c = 0.1 \left(\frac{V_{in}}{1-D} \right) \quad (12)$$

0.1 is nominal capacitor voltage ripple.

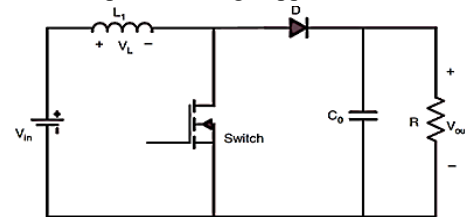


Fig. 1. (a) Boost converter circuit

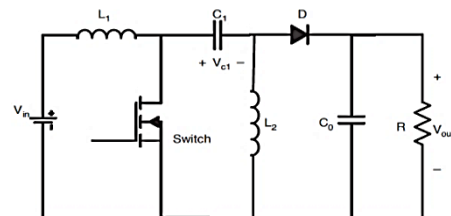


Fig.1(b) SEPIC converter circuit

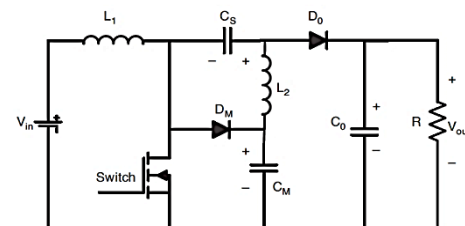


Fig. 1 (c) . modified SEPIC converter

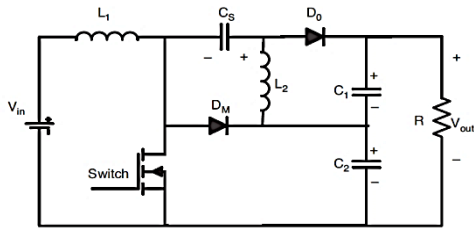


Fig.1 (d) modified SEPIC converter

Fig. 1. (a) Boost converter circuit, (b) SEPIC converter circuit, (c) and (d) modified SEPIC converter

In the modified SEPIC converter (Figure 1(d)), the inverse inrush current, the reverse voltage of the switches is lowered to the previous converters and the converter efficiency has increased, and the performance of the converter is faster than other previous converters. Eq. (8 to 11) also apply to this converter and the capacitors C_1 and C_2 are equal, and equal to half of the C_0 in (3). Overshoot voltage of this converter is its disadvantages.

III. PROPOSED DC-DC CONVERTER

The proposed converter of this paper is shown in Figure 2. In this figure, the converter contains a switch, three inductors L_1 , L_2 and L_3 , two diodes D_0 and D_M , and three capacitors C_1 , C_2 and C_S . When the S switch is closed, bias diodes are reversed and turned off, as shown in Fig. 3. In this case, the inductors save energy. The current of L_2 and L_3 passes through capacitors C_2 and C_S , and L_1 is parallel to the source. Figure 4 shows the switch when it is open. In this case, the diodes turn on and the inductor L_1 is in discharge mode. The L_2 is discharged through the diode D_0 and L_3 through a capacitor C_2 . The total voltage of the capacitor C_1 and C_2 is equal to the output voltage of the converter. Voltage of capacitors C_1 and C_2 is approximately equal (it is shown in Figure 6).

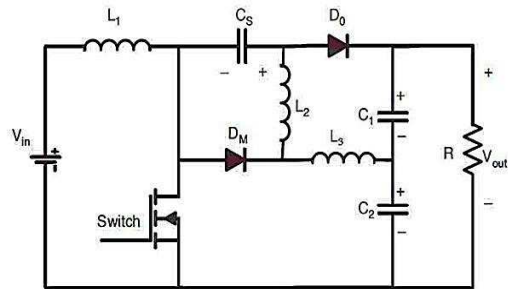


Fig. 2. Proposed converter circuit

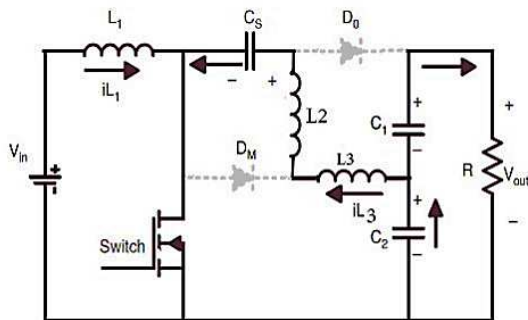


Fig. 3. Proposed converter switched ON condition circuit.

The maximum voltage for the switch and all diodes are less than two thirds of the output voltage. The switching current in the ON mode is equal to the total current of the inductors L_1 and L_2 (see Figures 5-7).

$$V_{out} = V_{C1} + V_{C2} \quad (13)$$

$$V_{C1} = V_{C2} = \frac{1}{2} V_{out} \quad (14)$$

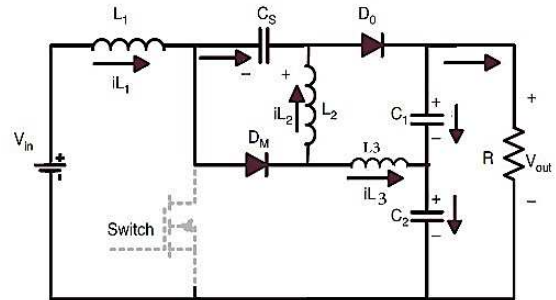


Fig. 4. Proposed converter switched OFF condition circuit.

In this paper, the performance of a typical Boost, SEPIC and Modified SEPIC converter is investigated, because the proposed converter is derived from the modification in the structure of these converters. In the proposed converter, the conventional method has been used to obtain the inductor and capacitor calculation equations. The static gain of the proposed converter is determined by the fact that the mean voltage of the inductor in a steady state is zero. The amount of energy stored in the inductor is equal and symmetrical when the switch is on and/or off. The relationship between the duty cycle is provided in (16) with respect to the steady-state performance.

$$\frac{V_{out}}{V_{in}} = \frac{2D}{1-D} \quad (15)$$

$$D = \frac{V_{out}}{V_{out} + 2V_{in}} \quad (16)$$

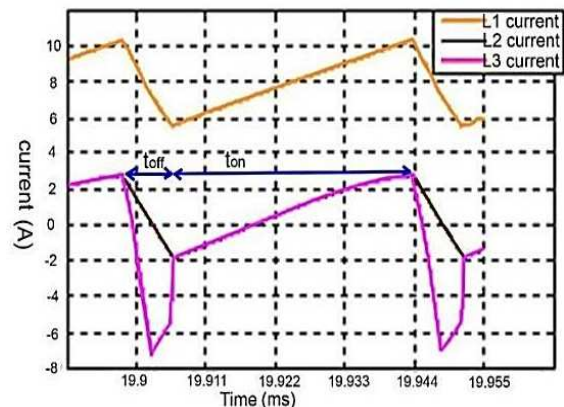


Fig. 5. Inductors current waveform in one cycle ON and OFF switch.

As seen in Figure 5, L_1 and L_2 inductor current ripple is quite similar, so:

$$L_1 = L_2 = \frac{DV_{in}}{f\Delta i_{L1}} \quad (17)$$

$$C_1 = C_2 = \frac{DV_{out}}{Rf\Delta V_{C1}} = \frac{2DV_{out}}{Rf\Delta V_{out}} \quad (18)$$

$$\frac{\Delta V_{out}}{V_{out}} = 1\% \quad (19)$$

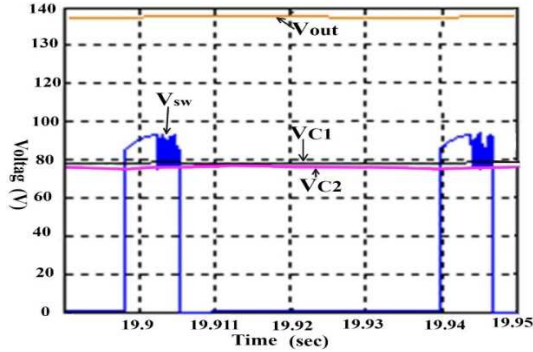


Fig. 6. Load voltage waveform, capacitors C1, C2 and the voltage on the switches.

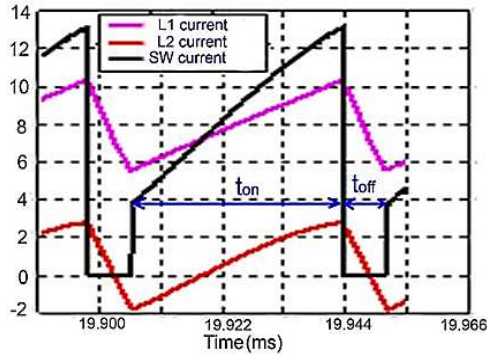


Fig. 7. Current Waveforms of the inductors L1, L2 and the current passing through the switch.

The capacitor average current in one cycle is zero. So:

$$C_s = \frac{i_{out}(1-D)}{0.1(2D-1)fV_{in}} \quad (20)$$

$$C_s = \frac{20D}{Rf(2D-1)} \quad (21)$$

Figure 7 shows that, in-time of the switched ON, the sum of the current flows of the inductors L1 and L2 with the current passing through the switch are equal. To calculate the components of the converters, the base values are shown in Table 1.

According to equation above, parametric values of the converters have been calculated as it is visible in Table 2.

Table 1. Base value of proposed converter

Switching frequency	24 kHz
Output voltage	150 V
Output power	100 W
Input voltage	15 V

Table 2. Parameters and components of converters

Parameters /components	Boost	SEPIC	Modified SEPIC c	Modified SEPIC d	proposed
Input voltage (Vin)	15 V	15 V	15 V	15 V	15 V
Switching frequency (f)	24 kHz	24 kHz	24 kHz	24 kHz	24 kHz
Duty cycle (D)	0.9	0.91	0.82	0.82	0.82
L1	112.5 μ H	113.7 μ H	102 μ H	102 μ H	102 μ H
L2	-	113.7 μ H	102 μ H	102 μ H	102 μ H
C1	-	1.518	-	50 μ F	50 μ F
C2	-	-	-	50 μ F	50 μ F
Co	100 μ F	100 μ F	100 μ F	-	-
Cs	-	-	3.37 μ F	3.37 μ F	3.37 μ F
CM	-	-	3.37 μ F	-	-
R	224.88 Ω	224.88 Ω	224.88 Ω	224.88 Ω	224.88 Ω

IV.SIMULATION AND RESULTS

Proposed converter and other converters shown in Figure 1 is simulated using MATLAB/ Simulink to examine the design parameters above.

As shown in Figure 8, for the same input and output of all converters, the inrush current of the proposed converter is better than other converters in terms of both of the durability and the domain. Also, settling time of input current is faster in the proposed converter.

As shown in Figure 9, for the same input and output for all converters, the output voltage settling time of the proposed converter is faster. As shown in Figure 8 and 9, the proposed converter resulted in modification in the modified SEPIC converter (Figure 1(d)) in order to improve performance, increase the converter efficiency, reduce the intruder input current and decrease the settling time of the output voltage at the switching moment. The result is faster response of this converter than other converters studied. This converter works in combination of boost mode and SEPIC and reduces the inrush current in the inductor L1.

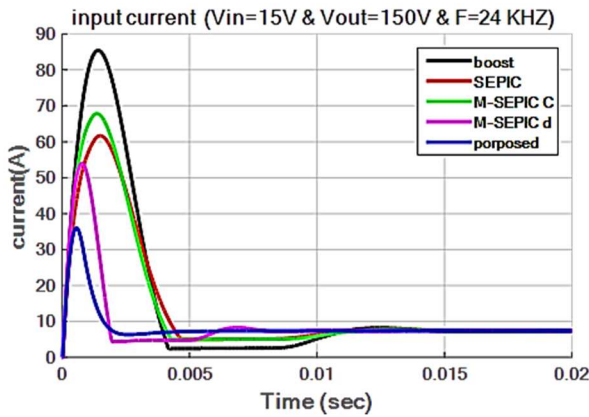


Fig. 8. Compare the inrush current of the studied converters

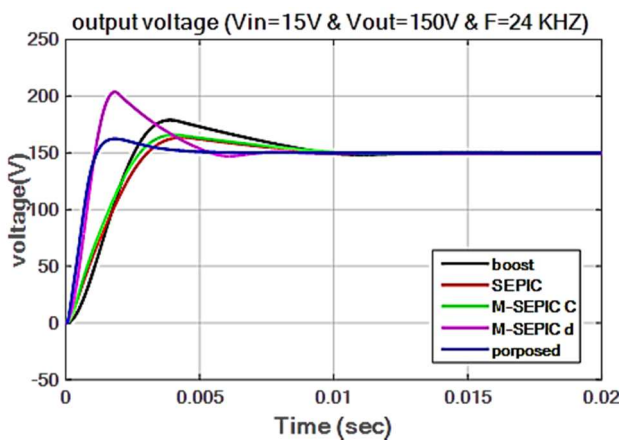


Fig. 9. Settling time the output voltage of the converters

For compare the converters, the MATLAB Simulink is used. Initially, the effect of L_3 on the characteristics of the proposed converter was examined and compared with the two converters the Modified SEPIC (Figure 1(c & d)). Two boost and SEPIC converters have been discarded due to their large difference in their values compared to the other three converters. Also the difference between the duty cycles on these two converters, which makes it less efficient. Figure 10 shows the input inrush current. It is clearly that the proposed converter inrush current control is better. And by increasing the inductor L_3 , the inrush current is reduced.

However, it should be noted that reducing the amount of L_3 will be effective up to a certain range. According to Figure 11, the inverse current ratio to the input current is shown for L_3 changes. It is shown that $L_3=10\mu H$ which is equivalent to 10% of the inductor L_1 , is a proper value.

The effect of the inductor L_3 on the proposed converter efficiency is shown in Figure 12. Increasing of the L_3 value will increase the efficiency of the proposed converter. Even with a small amount of L_3 , it has better performance than other converters and it will lead to Reduces output voltage over shoot too (See Figure 13). It should be consider that the increase of the switch voltage is its disadvantages (See Figure 14). According to the stated contents, the value of the inductor L_3 is suitable up to 10% of the inductor L_1 , and it brings good

results to us. Also the switch voltage is in suitable range (Less than two thirds of the output voltage).

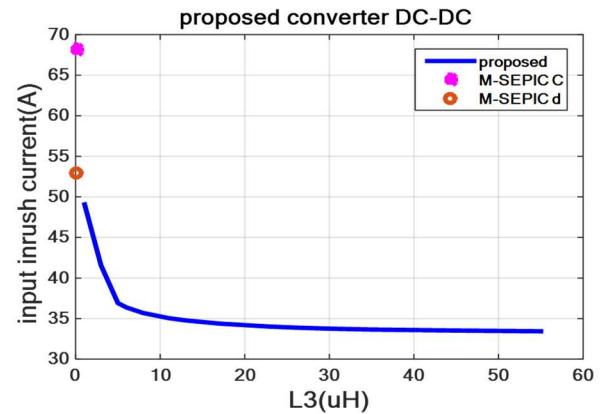


Fig. 10. The effect of inductor L_3 changes on the inrush input current of the proposed converter

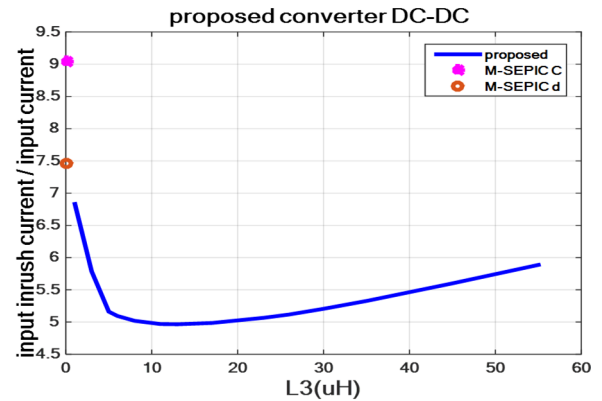


Fig. 11. The effect of L_3 inductance changes on the ratio of the input inrush current on its steady state flow

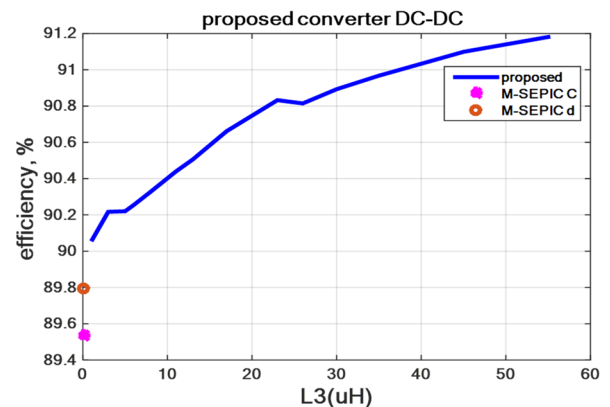


Fig. 12. The effect of L_3 inductance changes on proposed converter efficiency and comparing it with two M-SEPIC-C, M-SEPIC-d

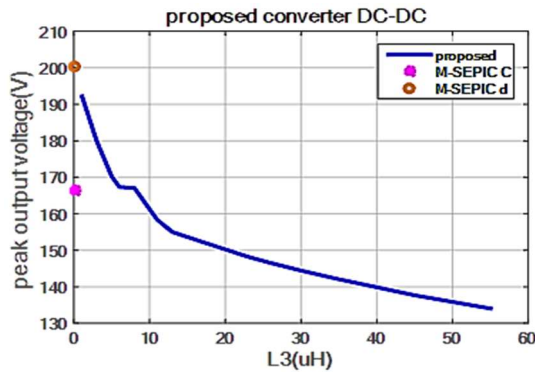


Fig. 13. The effect of L3 inductance changes on the overshoot of the proposed converter and comparing it with two M-SEPIC-C, M-SEPIC-d

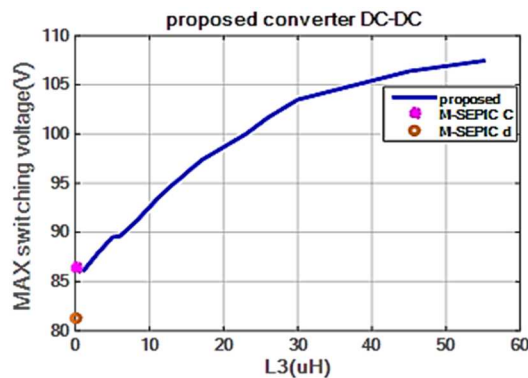


Fig. 14. The effect of L3 inductor changes on the inverse voltage of the proposed converter switch.

The output voltage of the boost, SEPIC, M-SEPIC C, M-SEPIC d, and the proposed converter in both L3 values (8 and 10 μH) are shown in Figure 15. The output voltage and current of the converters is shown in Figure. 15 and 16 under a stable performance with different duty cycles, and the lower voltage of the boost converter and SEPIC is visible to the modified converters and it shows that the modified converters voltage static gain is higher. In particular, it is in the range of 78% - 84% of the duty cycle used for increasing the voltage tenfold. In Figure 17, the changes of output voltage overshoot of converters are observed. The proposed converter performed better output voltage than the M-SEPIC-C and M-SEPIC-d converters. This will improve with increasing the inductor L3. It should be consider that a transient high output voltage can damage the load.

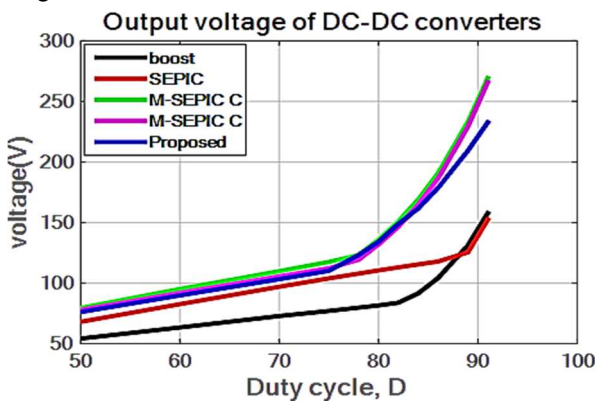


Fig. 15. Output voltage of DC-DC converter

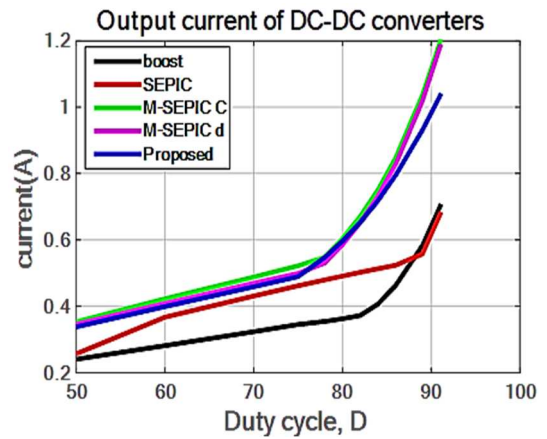


Fig. 16. DC-DC converters output current

Table 3 shows the performance of the converters at 82% duty cycle where the input voltage is constant at 15 V . It is shown that the boost and SEPIC converter in this case have lower output voltage. To produce a voltage tenfold, the duty cycle of these two converters must be more than 90%.

However, the switching voltage of the SEPIC converter is very high but, the switching voltage on the converter is greater than the M-SEPIC-C and M-SEPIC-d which is within the permissible range. If necessary, this voltage can be reduced by reducing the amount of inductor L3. But the current of the proposed converter switch is almost equal to the modified converters and the boost and SEPIC converters due to the lower output voltage have less switching current. As it is shown in Figure 19, there is less input current for classic boost and SEPIC converter too. The current of other converters are almost equal to the input current due to the same output voltage. As shown in Figure 20, the proposed converter is very effective in controlling and reducing the inrush current.

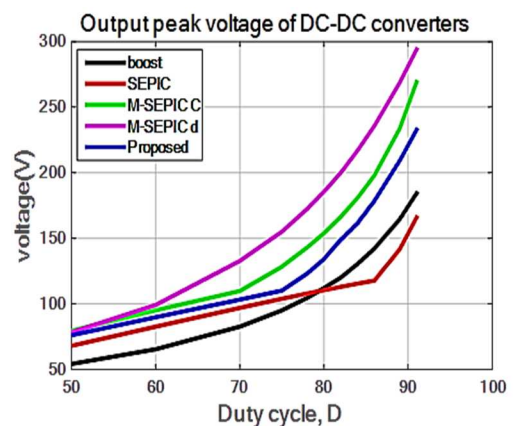


Fig. 17. Output peak voltage of DC-DC converters

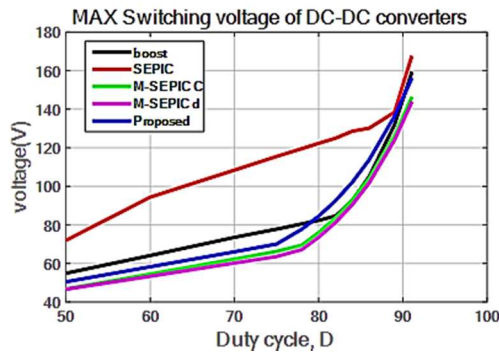


Fig. 18. Switching voltage of DC-DC converters

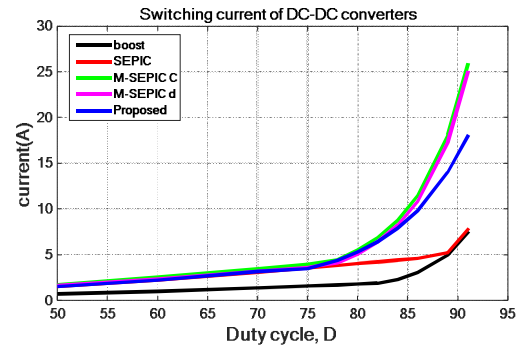


Fig. 19. DC-DC converters switching current

Table 3. Converter performance at 82% duty cycle for constant input voltage value of 15V

Parameter/Components	Boost	SEPIC	M-SEPIC-C	M-SEPIC-d	Proposed L3=8	Proposed L3=10
Output voltage (V)	83.7521	112.948	150.8902	146.5836	147.167	146.8398
Switch voltage (V)	84.615	124.98	83.726	81.285	90.9	92.58
Inductor starting current (A)	59.38	26.78	69.32	54.5	37.4	37
Output current (A)	0.3724	0.5023	0.671	0.6518	0.6544	0.653
Output power (W)	31.189	56.734	101.247	95.543	96.306	95.886

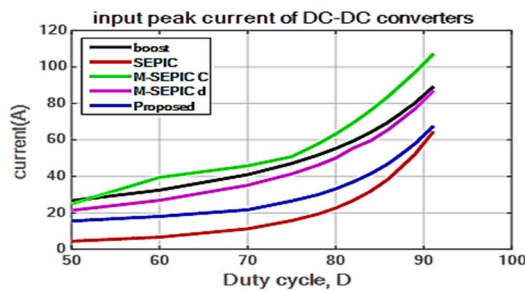


Fig. 20. Input peak current of DC-DC converters

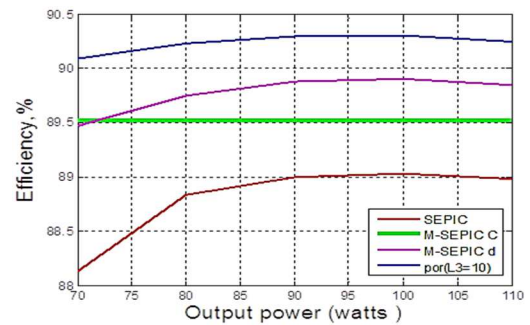


Fig. 22. Measured efficiency of the different converters

In Figure. 21, the time response of transient output voltage response has been analyzed for different types of converters. It is clear that the proposed converter is faster than other converters with settling time. For this reason, the proposed converter offers a faster response to the load and source voltage change.

In Figure 22, the efficiency change of different converters is shown. The proposed converter is in the best state of efficiency compared to other converters. The highest efficiency with 90.3 percent for the proposed converter has occurred in nominal values. The boost and SEPIC converters due to more duty cycle of switched ON ($D = 90$), have further switching losses and less efficiency.

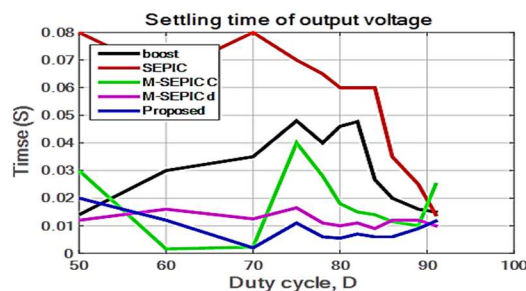


Fig. 21. Settling time of output voltage

V. CONCLUSION

In this paper, a new structure of a non-isolated DC-DC converter with a high voltage static gain is presented. In this proposed converter, an inductor has been added, which reduces the input current. It is led to the reduce of tension at the output voltage. In addition to these features, the time response for the output voltage is improved by reducing the transient time and peak time. In full load conditions and with inductor $L3 = 10\mu H$, the proposed converter is at the highest efficiency with 90.3% efficiency over other topologies presented by others and in the same conditions, the inrush current of the proposed converter is 37.6A that is 18.7A less than the best converters in the previous works. The transient time of the output voltage in of the proposed converter is 5.4ms while for the best previous converter this time was 10.6ms. This impresses on the speed of the system response to load changes. According to all said reasons, the proposed converter can be a good choice for many renewable energy systems applications with a simple design and high efficiency.

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