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High Efficient and High Step-Up Dual Switches Converter Based on Three Coupled Inductors

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ABSTRACT

This paper proposes a novel high step-up converter suitable for distributed generation using renewable power sources. The proposed converter includes a dual switches structure, two voltage multiplier cells and a three-windings coupled inductor for achieving high voltage gain. The configuration of the proposed converter not only reduces the voltage and current stresses of the switches, but also restricts the input source current, which reduces transmission losses and increases the lifetime of the input source. In the proposed converter, the multiplier cells are charged during the switch-on and switch-off periods, which cause to enhance the voltage gain of the converter and improve its productivity. Another feature of the proposed converter is that the inductive leakage energy of the coupled inductor is recycled through a passive clamping circuit which, in turn, has a considerable impact on system efficiency. A comparison is conducted between the performance of the proposed converter and the counterpart converters to demonstrate the proposed converter's superiority in terms of voltage gain, voltage stress across the switches and diodes and number of components. Theoretical analysis and simulation results are provided to demonstrate the authenticity of the proposed converter.

Article Info

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High Step-Up Converter, Low Voltage Stress,
Three-Winding Coupled Inductor
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I. INTRODUCTION

Nowadays, renewable energy sources are widely being employed worldwide owing to the serious problems with fossil fuel sources use including environmental pollution, global climate change and resource depletion. [1]. In the middle of the renewable energy sources, photovoltaic (PV) systems have received considerable attention during recent years and are predicted to attract largest investment by year 2040. Since the output voltage of PV arrays is not high enough to directly connect to DC loads/micro-grid or inverters DC-link supplying an AC load/utility, using of a high step-up DC-DC converter is necessary to boost their low voltage to high voltage. [2 -6].

A renewable energy system consisting of PV array, high step-up converter and an inverter for producing AC voltage are shown in Fig.1 Generally, the conventional high step-up converters like boost converter cannot be adopted to provide the high voltage boost gain since the parasitic parameters will limit the converter to operate with an extreme duty ratio needed for high voltage gain [7]. In recent years, many step-up converters have been developed to overcome this issue [8 –11].

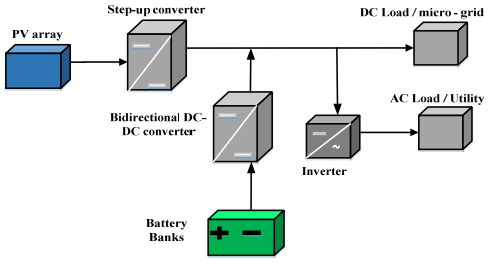

Fig. 1. Typical fuel cells system.

An alternative solution for providing high step-up voltage gain is a two-stage approach based on a cascade connection of two conventional boost converters [8]. However, this increases the number of the components and as a result reduces the system efficiency and rises the cost which is not suited to renewable energy applications. Accordingly, a one stage high step-up converter can be highly desirable in the renewable energy systems. One the main challenge regarding one stage high step-up converters is large voltage and current stresses on the power switches which, in turn, have a negative effect on the converter efficiency. A possible method to deal with this problem is using conventional dual switches structure which is suitable for high power applications [9, 10]. Although, the lower current stress of the power switches can be achieved using this structure, the voltage stress of the switches is still high and much higher voltage gain cannot be

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realized compared to the conventional boost converters. The higher step-up voltage gain can be achieved by integrating the coupled-inductor into the dual switches structure [11 -13]. The switch voltage stress is also alleviated by the transformer function of the coupled-inductor. Nonetheless, owing to the leakage inductance of the coupled inductors, the voltage spike across the switches appears during the off state and the leakage energy diminishes the converter efficiency [14].

In this paper, a new high step-up converter is proposed. This converter combines the advantages of the dual switches structure, coupled inductors and voltage multiplier cells and hence an extremely high step-up gain can be easily achieved with minimum number of voltage multipliers and low turns ratio of the coupled inductor. Eliminating the need for operating with high duty cycle, the proposed converter presents high efficiency in a wide range of operation. In addition, it exhibits low current ripples and low conduction losses which make it attractive for high power applications. Moreover, the voltage stress across the switches and diodes is much lower than the output voltage. In the proposed converter, the energy stored in the leakage inductance of the coupled inductor is recycled through a passive clamping circuit which not only has a considerable impact on system efficiency, but also relieves the voltage spike across the switches.

This paper organizes as follows: In the next section, the proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is presented and its various switching states will be investigated. In section III, the steady state analysis is provided and also in section IV the components stress is evaluated. A comparison between the proposed converter and the counterpart topologies is carried out in Section V. Simulation results are given in Section VI. Finally, the conclusion of this paper are reviewed in section VII.

II. The Proposed Converter Structure and Operating Principles

A. CCM Operation

Fig.2 shows the equivalent circuit of the proposed converter which consists of two active switches, seven diodes and seven capacitors.

In the proposed converter, S_1 and S_2 are turned on and off simultaneously using one control signal. In this figure, L_M and L_K are the magnetizing and the leakage inductances of the three-winding coupled inductor, respectively. The switches S_1 and S_2 share the same operation signal and one control circuit is needed

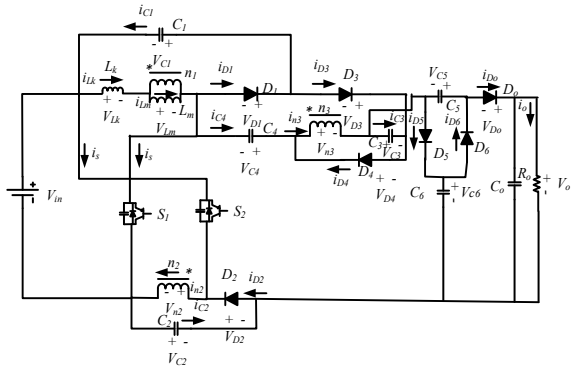

Fig. 2. The equivalent circuit of the proposed converter.

. The waveform of the switches S_1 and S_2 operating in CCM are shown in Fig.3. In the circuit analysis, the proposed converter operates in continuous conduction mode (CCM), and the duty cycle of the power switches is 0.5.

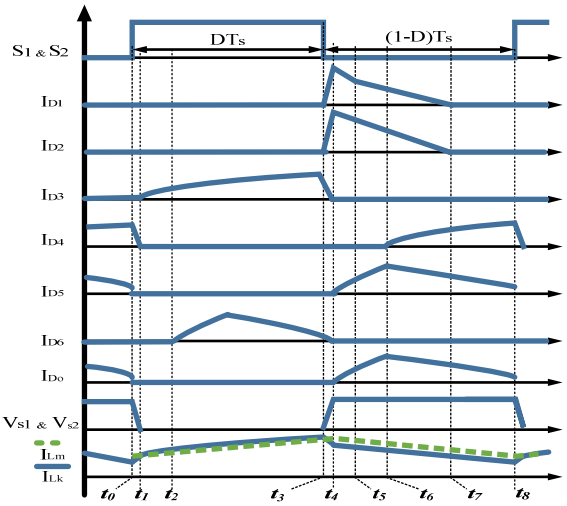

Fig. 3. Operational waveforms of the proposed converter in CCM.

The inductive leakage energy associated with L_K is recycled through the capacitors C_1 and C_2 and not only the efficiency of the proposed systems is improved, but also the voltage spike across the switches during off state is significantly reduced and there is no need to extra snubber circuit.

The steady-state waveforms of the proposed converter operating in CCM are shown in Fig. 3 which are composed of eight operating modes during a switching period as follows:

Mode I [t_0, t_1]: At $t=t_0$, the power switches S_1 and S_2 are turned on, the diodes D_1, D_2, D_3, D_5, D_6 and D_o are reversed-biased and the diode D_4 is forward biased, as shown in Fig.4(a). Accordingly, L_k and L_m are charged by the input voltage source V_{in} and hence the currents passing through the

leakage inductor (i_{Lk}) and the magnetizing inductance (i_{Lm}) increase linearly. Moreover, the current i_{n3} and the diode current i_{D4} decrease in this mode.

Mode II [t_1, t_2]: At t=t_1, both of the power switches S_1 and S_2 remain on, and the diodes D_1, D_2, D_4, D_5, D_6 and D_o are reversed-biased and the diode D_3 is forward biased, as shown in Fig.4(b). The primary side of the coupled inductor is placed in parallel to the input voltage source V_{in} and hence the primary leakage inductance and the magnetizing inductance are charged. A part of the input voltage source energy is also transferred to the tertiary side of the coupled inductor and charges the capacitor C_4.

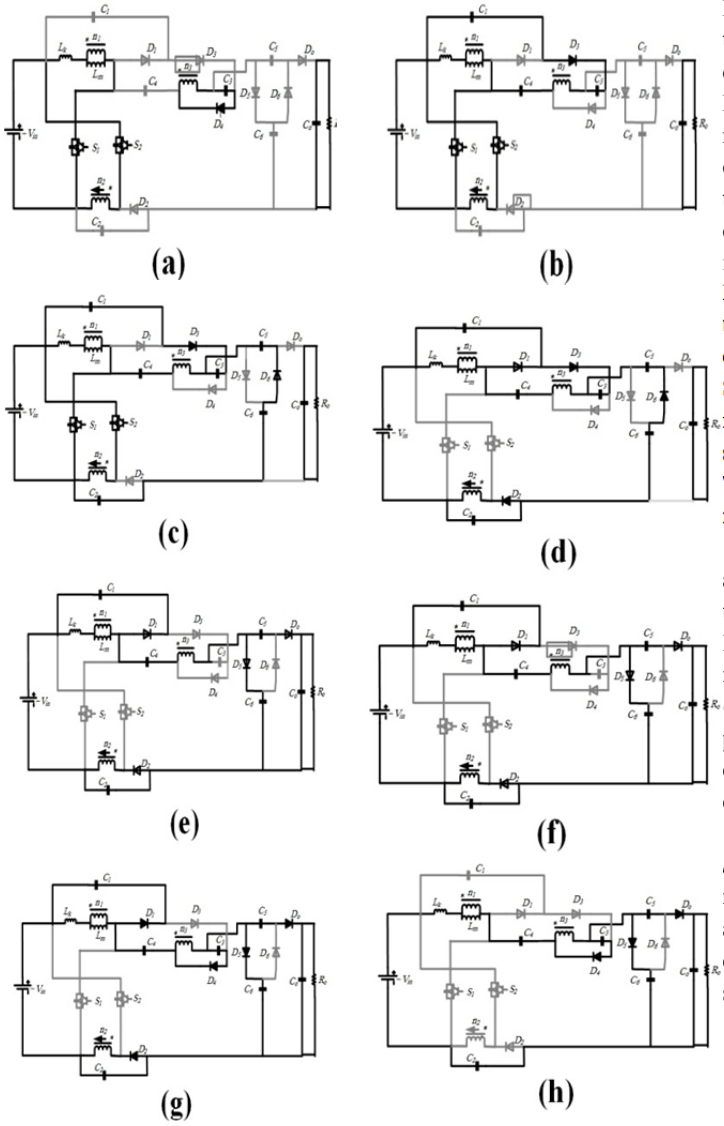

Fig. 4. Operating modes of the proposed converter, (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, (f) Mode VI, (g) Mode VII, (h) Mode VIII.

Mode III [t_2, t_3]: At t=t_2, the power switches S_1 and S_2 remain on and the diodes D_1, D_2, D_4, D_5 and D_o are reversed-biased while the diodes D_3 and D_6 are forward biased, as shown in Fig.4(c). In this state, the capacitor C_6 is discharged and the capacitor C_5 is charged by the energy stored in the leakage inductance L_k and the magnetizing inductance L_m.

Mode IV [t_3, t_4]: At t=t_3, the power switches S_1 and S_2 are turned off, and the diodes D_1, D_2, D_4, D_5 and D_o are reversed-biased while the diodes D_1, D_2, D_3 and D_6 are forward biased, as shown in Fig.4(d). The energy stored in the leakage inductance L_k and the magnetizing inductance L_m is released to the clamped capacitor C_1 and also transferred to the clamped capacitor C_2.

Mode V [t_4, t_5]: At t=t_4, both of the power switches S_1 and S_2 are turned off, and the diodes D_3, D_4 and D_6 are reversed-biased and diodes D_1, D_2, D_5 and D_o are forward biased, as shown in Fig.4(e). The energy stored in the leakage inductance L_k and the magnetizing inductance L_m is still being transferred to the capacitors $C1$ and C_2 in this mode. The capacitor C_o is charged through the input source V_{in}, the coupled inductor and the capacitors C_4 and C_5 and hence the diode currents i_{Do} and i_{D5} increase.

Mode VI [t_5, t_6]: At t=t_5, both of the power switches S_1 and S_2 are turned off, and the diodes D_3, D_4 and D_6 are reversed-biased and diodes D_1, D_2, D_5 and D_o are forward biased, as shown in Fig.4(f). Similar to the previous mode, the diode currents i_{Do} and i_{D5} increase and the output capacitor C_o is charged by the input source V_{in}, the coupled inductor and the capacitors C_4 and C_5. The only difference is that the capacitor C_2 is discharged in this mode.

Mode VII [t_6, t_7]: At t=t_6, both of the power switches S_1 and S_2 are turned off, and the diodes D_3 and D_6 are reversed-biased and the diodes D_1, D_2, D_4, D_5 and D_o are forward biased, as shown in Fig.4(g). The energy stored in the leakage inductance L_k and the magnetizing inductance L_m is released to the clamped capacitor C_1. The secondary side of the coupled inductor is placed in parallel to the capacitor C_2 and also the input source V_{in}, the coupled inductor and the capacitors C_4 and C_5 charges the output capacitor C_o.

Mode VIII [t_7, t_8]: At t=t_7, both of the power switches S_1 and S_2 are turned off, and the diodes D_1, D_2, D_3 and D_6 are reversed-biased and the diodes D_4, D_5 and D_o are forward biased, as shown in Fig.4(h). During this mode, the capacitor C_3 is charged. In addition, the capacitor C_o is charged by the input source V_{in}, the coupled inductor and the capacitors C_2, C_4 and C_5.

B. DCM Operation

The proposed converter operating in discontinuous conduction mode (DCM) is analyzed as follows. Figure 5 shows the operating stages of each mode of the proposed converter during the DCM operation. There are three modes in DCM operation. During the DCM operation to simplify the analysis, the leakage inductor L_k of the coupled inductor is neglected .The operating modes are explained as follows:

Mode I [t_0, t_1]: During this time interval, the power switches S_1 and S_2 are turned on, and the diodes D_3 and D_6 are forward biased. The equivalent circuit is shown in Fig.6 (a).

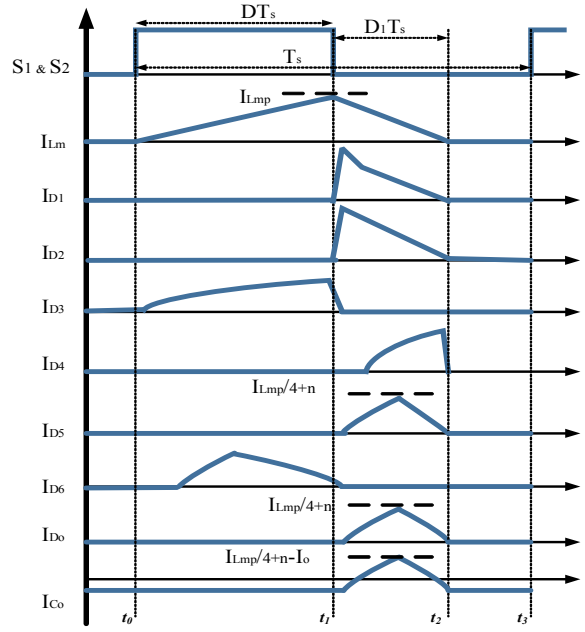

Fig. 5. Some typical waveforms of the proposed converter at DCM operation.

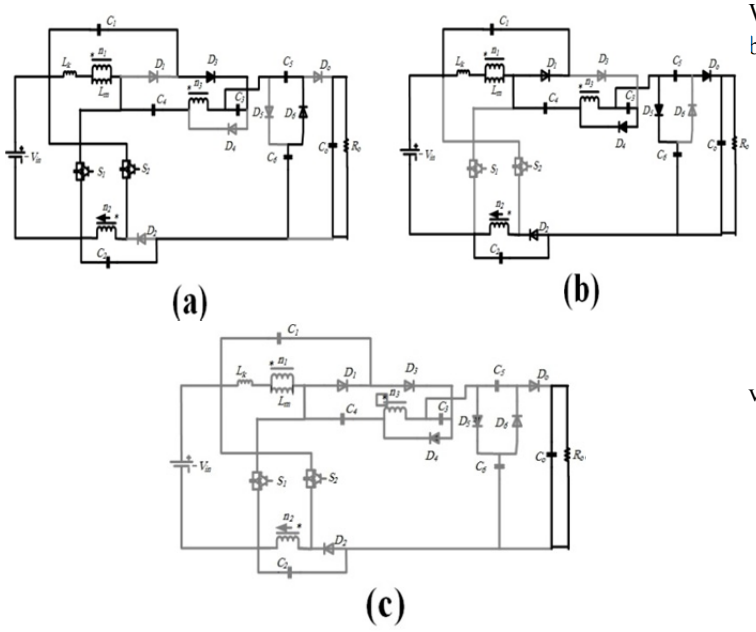

Fig. 6. Operating modes at DCM during a switching period. (a) Modes I; (b) Modes II; and (c) Modes III.

The energy stored in the magnetizing inductance L_m causing the capacitor C_5 to charge. The output capacitor C_o provides the energy to load R. The main switches S_1 and S_2 are turned off at $t = t_1$, and this operation mode is terminated.

Mode II [t_1, t_2]: During this time interval, the main switches S_1 and S_2 are turned off, and the diodes D_1, D_2, D_4, D_5 and D_o are forward biased. The equivalent circuit is shown in Fig.6(b). The energy stored in the leakage inductance L_k and the magnetizing inductance L_m is released to the clamped capacitor C_1. The magnetizing inductor L_m, DC source V_{in}, the coupled inductor and the capacitors C_4 and C_5 charge the output capacitor C_o. This operating mode is terminated when the energy stored in Lm is depleted at $t = t_2$.

Mode III [t_2, t_3]: During this time interval, the main switches S_1 and S_2 are turned off. The equivalent circuit is shown Fig.6 (c). The output capacitor C_o provides energy to the output load. This mode is terminated at $t = t_3$, and the main switches S_1 and S_2 are turned on again during the next mode.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

According to Fig. 4 (b) and using the volt-second balance of the magnetizing inductance L_m, we have

$$V_{Lm} = V_{n1} = V_{n2} = \frac{D}{1-D} V_{in} \tag{1}$$

With attention to Figs. 4(a), (c), (e), (f) and (g), the relation between the capacitor voltages C_1-C_4 can be written as:

$$V_{C1} = V_{C2} = V_{Lm} = \frac{D}{1-D} V_{in} \tag{2}$$

$$V_{C3} = \frac{nD}{1-D} V_{in} \tag{3}$$

$$V_{C3} + V_{n3} = \frac{n}{1-D} V_{in} \tag{4}$$

$$V_{C4} = V_{C1} + V_{C3} + V_{n3} + V_{in} = \frac{1+n}{1-D} V_{in} \tag{5}$$

From Equs. (3)-(5) and Figs. 4(e) and (d), the capacitors voltage C_5 and C_6 can be derived as:

$$V_{C6} = V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_{in} = \frac{n(D+1)+(D+2)}{1-D} V_{in} \tag{6}$$

$$V_{C5} = V_{C6} - V_{C1} - V_{C2} - V_{C3} - V_{in} = \frac{1+n}{1-D} V_{in} \tag{7}$$

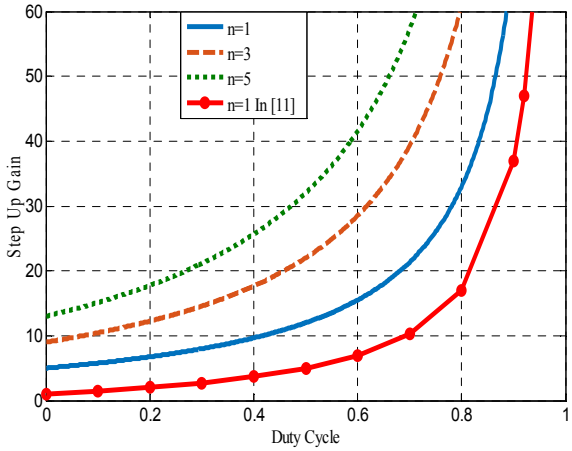

Fig. 7. The voltage gain based on turns ratio and duty cycle.

The output voltage is derived from Fig. 4(h):

$$V_o = V_{C5} + V_{C6} = \frac{n(D+2)+(D+3)}{1-D} V_{in} \quad (8)$$

Thus, the voltage gain of the proposed converter can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{n(D+2)+(D+3)}{1-D} \quad (9)$$

From Equ. (9), it is evident that the proposed converter is able to provide a high step-up voltage gain without requiring an extreme duty ratio. Fig. 7 depicts the voltage gain of the proposed converter versus duty ratio D in different turns ratio n. When the duty cycle is 0.5, the voltage gain attains 12 at turns ratio n of 1. This value is 32 at a turns ratio n of 5 and a duty cycle of 0.5.

B. *DCM Operation*

In mode I of DCM operation Fig. 6 (a), the main power switches are turned on and hence, using the volt-second balance of the magnetizing inductance L_m, we have:

$$V_{Lm} = V_{n1} = V_{n2} = \frac{D}{D_1} V_{in} \quad (10)$$

The magnetizing inductor peak current can be expressed as:

$$I_{Lmp} = \frac{V_{in}}{L_m} DT_s \quad (11)$$

In mode II of DCM operation as shown in Fig. 6(b), the main power switches are turned off and the capacitor Co supplies energy to the load. With attention to Figs. 6(a), (b), the relation between the capacitor voltages C_1-C_4 can be written as

$$V_{C1} = V_{C2} = V_{Lm} = \frac{D}{D_1} V_{in} \quad (12)$$

$$V_{C3} = \frac{nD}{D_1} V_{in} \quad (13)$$

$$V_{C3} + V_{n3} = \frac{n}{D_1} V_{in} \quad (14)$$

$$V_{C4} = V_{C1} + V_{C3} + V_{n3} + V_{in} = \frac{1+n}{D_1} V_{in} \quad (15)$$

From Equs. (13)-(15), the capacitors voltage C_5 and C_6 can be derived as:

$$V_{C6} = V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_{in} = \frac{(3+n)D + 2D_1 + n}{D_1} V_{in} \quad (16)$$

$$V_{C5} = V_{C6} - V_{C1} - V_{C2} - V_{C3} - V_{in} = \frac{D_1 + D + n}{D_1} V_{in} \quad (17)$$

Then, the output voltage is derived:

$$V_o = V_{C5} + V_{C6} = \frac{(4+n)D + 3D_1 + 2n}{D_1} V_{in} \quad (18)$$

The voltage gain of the proposed converter during the DCM mode can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{(4+n)D + 3D_1 + 2n}{D_1} \quad (19)$$

$$D_1 = \frac{((4+n)D + 2n)V_{in}}{V_o - 3V_{in}} \quad (20)$$

According to Fig. 5 the average current value I_{Co}, can be expressed as:

$$I_{Co} = \frac{1}{2} D_1 \frac{I_{Lmp}}{4+n} - I_o \quad (21)$$

Since I_{Co} is equal to zero under steady state, Equs. (11), (20), and I_{Co} = 0 can be substituted to Equ. (21). Thus, Equ. (21) can be rewritten as follows:

$$\frac{[(4+n)D^2 + 2nD]V_{in}^2 T_s}{2[V_o - 3V_{in}](4+n)L_m} = \frac{V_o}{R} \quad (22)$$

Then, the normalized magnetizing-inductor time constant is defined as:

$$\tau_m = \frac{L_m}{RT_s} = \frac{L_m f_s}{R} \quad (23)$$

Where f_s is the switching frequency. Substituting Equ. (23) into Equ. (22), the voltage gain is given by

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{3}{2} + \sqrt{\frac{3}{2} + \frac{D^2}{2\tau_m} + \frac{nD}{(4+n)\tau_m}} \quad (24)$$

C. *Boundary Operating Condition Between CCM and DCM*

If the proposed converter is operated in boundary condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. The boundary normalized

magnetizing inductor time constant τ_{mB} can be derived from Equs. (9) and (24):

$$\tau_{mB} = \frac{(1-D)^2[D^2 + \frac{2nD}{4+n}]}{2n(D+2)^2 - D^2 + 6D + 15} \quad (25)$$

The curve of τ_{mB} is plotted in Fig. 8. If τ_m is larger than τ_{mB}, the proposed converter is operated in CCM.

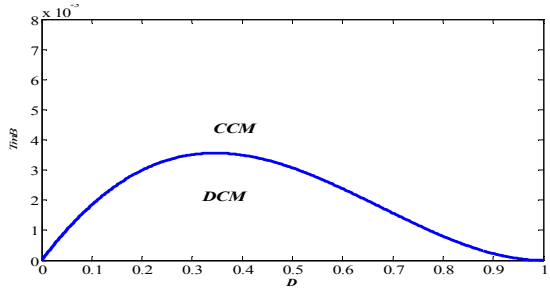

Fig. 8. Boundary condition of proposed converter under n = 3.

IV. POWER LOSS AND VOLTAGE STRESS ON THE COMPONENTS

To simplify the circuit analysis of the proposed converter in CCM, the transient characteristics are not considered and some assumptions are made as follows:

- All components of the proposed converter are ideal.
- The turns ratios of the coupled inductor is: n_1: n_2: n_3 = 1: 1: n.
- Leakage inductances of the coupled inductor are neglected.
- The voltages across all capacitors are considered constant due to their large capacity.

A. Voltage stress of the power devices

The voltage stresses of the main switches S_1, S_2 and all of the diodes are given by Equs. (26) – (29).

$$V_{S1} = V_{S2} = \frac{V_{in}}{1-D} = \frac{V_o}{n(D+2)+(D+3)} \quad (26)$$

$$V_{D1} = V_{D2} = \frac{V_{in}}{1-D} = \frac{V_o}{n(D+2)+(D+3)} \quad (27)$$

$$V_{D3} = V_{D5} = V_{D6} = V_{Do} = (n+1)\frac{V_{in}}{1-D} = \frac{V_o(n+1)}{n(D+2)+(D+3)} \quad (28)$$

$$V_{D4} = n\frac{V_{in}}{1-D} = \frac{V_o n}{n(D+2)+(D+3)} \quad (29)$$

Equ. (26) confirms that the voltage stress on the power switches is always lower than 20% of the output voltage V_o. As a result, low-voltage-rated MOSFETs with low R_{DS} −ON can be adopted leading to lower conduction losses and costs. This specification makes the proposed converter well-suited for high step-up and high-power applications. Although the voltage stress on the diodes D_1 and D_2 are equal to the voltage stress on power switches, the voltage stress on the diodes D_3, D_4, D_5, D_6 and D_o increases as the turns ratio rises. Nonetheless, the voltage stress on theses diodes is always lower than the output voltage V_o. Fig. 9 shows the voltage across all the semiconductor components versus turns ratio n.

B. Analysis of Conduction Losses

Conduction losses in the proposed converter are due to four components: the active switches, the diodes, the coupled inductor and the capacitor.

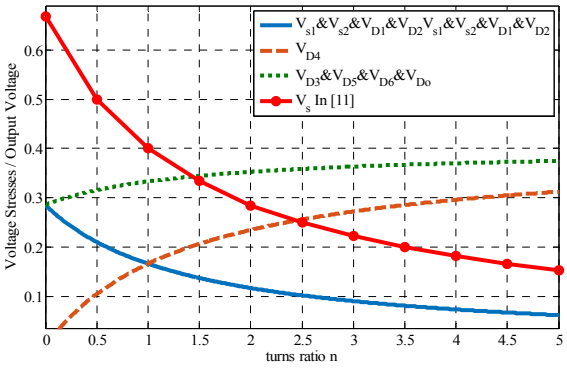

Fig. 9. The voltage stresses on semi-conductor components based on turns ratio n.

It is assumed that the ESR of the capacitors, core losses of the coupled inductor and switching losses are neglected considering its weak influence in front of other components. The leakage inductance of the coupled inductor is not also considered since the greater part of the leakage energy is recycled through the capacitors C_1 and C_2. The equivalent circuit containing the conduction losses of the coupled inductor and the semiconductors are represent in Fig. 10.

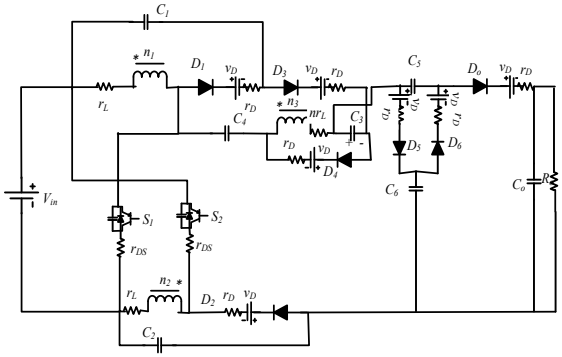

Fig. 10. The equivalent circuit for analyzing contain conduction losses.

For instance, v_D defines the forward voltages drop of the diodes: r_{DS} defines the resistance of power switches; r_L is the copper resistance of the primary side of the coupled inductor; and r_D is the resistance of the diodes. The conduction losses

analysis is performed using small ripple approximation and the capacitance and inductance are considered large enough to maintain the inductor current and capacitor voltages constant. Following the same procedure in previous section and using capacitor charge balance and inductor volt-sec balance, the voltage gain of the proposed converter can be obtained as:

$$M = \frac{\frac{n(D+2)+(D+3)}{1-D} - \frac{5v_D}{V_{in}}}{1 + r_{DS}\cdot r_y + r_L \cdot r_x + \frac{4(r_D + nr_L) + 6r_L}{R(1-D)} + \frac{r_D + nr_L}{RD}} \quad (30)$$

where

$$r_x = \frac{n^2(1+D)^2 + 5D(n+nD) + 6D^2}{(RD(1-D))^2}$$

$$r_y = \frac{(n+nD+D+1)(nD+n+2D+1)}{RD(1-D)}$$

Moreover, the circuit efficiency can be expressed using Equ. (31).

$$\eta = \frac{n(D+2)+(D+3) - 5\frac{v_D}{V_{in}}(1-D)}{\left[1 + r_{DS}\cdot r_y + R_L r_x + \frac{4r_D + (4n+6)r_L}{R(1-D)} + \frac{r_D + nr_L}{RD}\right] n(D+2)+(D+3)} \quad (31)$$

According to Equ. (31), it can be deduced that that the proposed topology will have higher efficiency if the input voltage is substantially higher than the sum of the forward voltage drop of all the diodes, or if the load resistance R is significantly larger than the resistances of coupled inductors and semiconductor devices. Fig.11. shows the voltage gain of the proposed converter versus the duty ratio D in different copper resistances r_L.

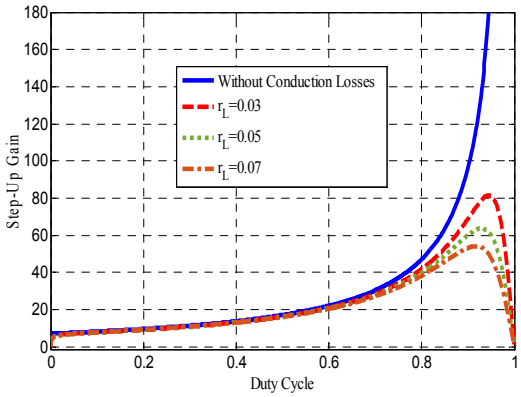

Fig. 11. Calculated voltage gain with different r_L

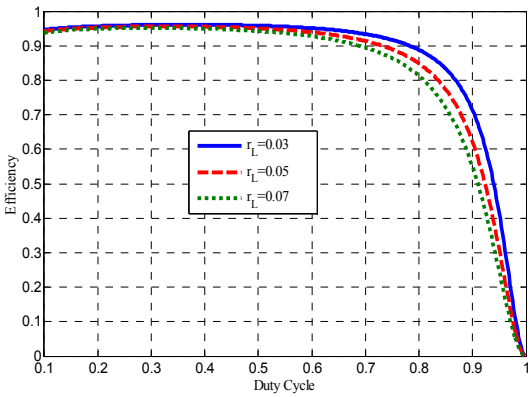

Fig. 12. Calculated efficiency with different r_L.

Fig.12. displays the efficiency of the proposed converter in terms of duty ratio D in different copper resistances r_L. From Fig.11 and Equ. (9), as it was expected, both voltage gain and efficiency are reduced with increasing the coupled inductor resistance r_L. Moreover, when the voltage gain and efficiency are significantly decreased at extreme duty cycles.

V. COMPARISON BETWEEN COUNTERPART CONVERTER

To illustrate the performance of the proposed converter, the results of its comparative evaluation are compared with other high step-up gain converters proposed in [9, 11] and [13] based on voltage gain, voltage stress on switches, the maximum voltage stress on diodes, number of switches, number of diodes and number of coupled inductors.

The performance comparison between these converters are listed in Table I. As it is evident in the table, using similar turns ratio, the proposed converter has the highest step-up gain among the other converters. Furthermore, the voltage stress on the semiconductor devices of the proposed converter is the lowest compared to other converters.

The proposed converter combines the advantages of the dual switches structure, coupled inductors and voltage multiplier cells that causes a high step-up voltage gain can be easily obtained with the low turns ratio of the coupled inductor and under low duty ratio leading to lower conduction losses and lower current ripple. Moreover, the voltage stress across the power switches is much lower than the output voltage resulting in using MOSFETs with lower on-state resistance and hence improving the efficiency. In addition, the inductive leakage energy of the coupled inductor is recycled through a passive clamping circuit which, in turn, has a considerable impact on system efficiency. As a result, the proposed converter presents high efficiency for a wide range of operation which makes it an attractive configuration for high-performance high-power applications. These advantages are obtained, though, at the expense of increasing the number of diodes compared to the converter in [13].

TABLE I
PERFORMANCE COMPARISON AMONG INTERLEAVED HIGH STEP-UP CONVERTERS

High Step-Up Converters	Proposed Converter	Converter in [11]	Converter in [9]	Converter in [13]
Voltage Gain	$\frac{n(D+2)+(D+3)}{1-D}$	$\frac{1+(2n+1)D}{1-D}$	$\frac{3+5D}{1-D}$	$\frac{1+n+D}{1-D}$
Voltage stress on Switches	$\frac{V_O}{n(D+2)+(D+3)}$	$\frac{V_O}{1+(2n+1)D}$	$\frac{V_O}{3+5D}$	$\frac{V_o}{1+n+D}$
maximum voltage stress on diodes	$\frac{V_O(n+1)}{n(D+2)+(D+3)}$	$\frac{(2n+1)V_O}{1+(2n+1)D}$	$\frac{(1+D)V_o}{3+5D}$	$\frac{nV_o}{1+n+D}$
Number of switches	2	2	2	2
Number of diodes	7	5	9	4
Number of inductors	1(coupled inductor)	2(coupled inductor)	4	1(coupled inductor)

Also, in Fig. 13, the curve shows the voltage gain versus the duty ratio of the proposed converter, and the converters in [9], [11], [13], [15] and [16] at CCM operation under n = 3.

VI. SIMULATION RESULTS

To verify the performance of the proposed converter, simulation results of a 420W DC/DC system are presented in this section. The specifications are as follows:

V_{in}: 20 V; V_o: 340 V; P_o: 420 W; fs: 50 kHz; D=0.5

$C_1 = C_2 = C_3 = 20\ \mu F$; $C_4 = C_5 = C_6 = 110\mu F$; $C_o = 220\mu F$;

$L_M = 133\mu H$; $L_k = 0.5\mu H$; $r_{S1\text{-}S2} = 5m\Omega$; v_D =0.8V; $r_D = 3m\Omega$;

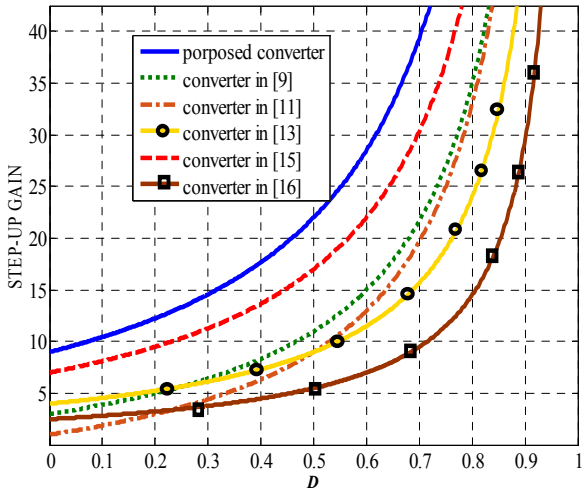

Fig.13. Voltage gain versus duty ratio at CCM operation at n = 3.

Fig. 14 shows the output voltage of the proposed converter with n=1 and n=2. The voltage levels in this figure clearly verify the authenticity of the theoretical analysis of the proposed converter.

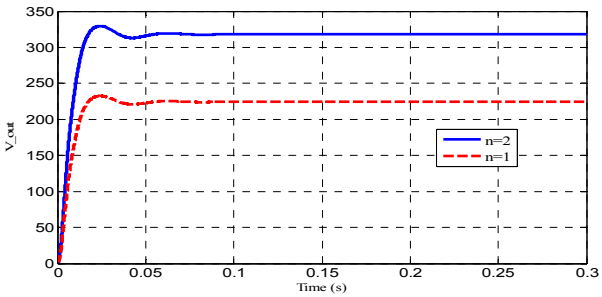

Fig. 14. The output voltage with n=1 and n=2

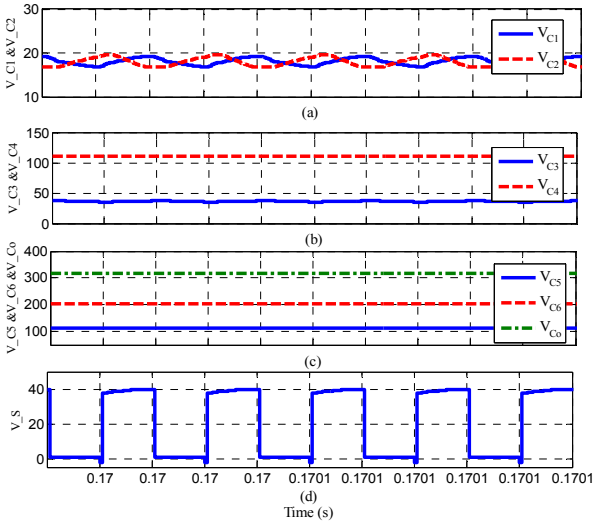

Fig. 15. The measured waveforms

Fig.15 shows the simulation waveforms of the proposed converter. According to Fig.15(a), the voltage across the capacitors C_1 and C_2 are, respectively, about 18.5V, which are confirmed by (2). Fig.15(b) shows the voltage on the capacitors C_3 and C_4 which are, respectively, about 37V and 111V, which agree with (3) and (5). In Fig.15(c), the voltages across the capacitors C_5, C_6 and C_o are shown that are 112V, 205V and 318V, respectively which confirms the validity of (6), (7) and (8). The output load voltage is also equal to the voltage on the capacitor C_o. The voltage stresses on the active switches are depicted in Fig.15(d). As illustrated in this figure, S_1 and S_2 have low voltage stress (about 40[V]), which are in compliance with (26).

VII. CONCLUSION

In this paper, a new high step-up dual switches DC-DC converter is proposed. The proposed converter combines the advantages of the dual switches structure, coupled inductors and voltage multiplier cells that causes a high step-up voltage gain can be easily obtained with the low turns ratio of the coupled inductor and under low duty ratio leading to lower conduction losses and lower current ripple. Moreover, the voltage stress across the power switches is much lower than

the output voltage resulting in using MOSFETs with lower on-state resistance and hence improving the efficiency. In addition, the inductive leakage energy of the coupled inductor is recycled through a passive clamping circuit which, in turn, has a considerable impact on system efficiency. As a result, the

proposed converter presents high efficiency for a wide range of operation which makes it an attractive configuration for high-performance high-power applications. The simulations results demonstrate the validity of the theoretical analysis and the effectiveness of the proposed converter as an efficient high step-up converter.

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