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Symmetric and Asymmetric Configurations for a Multilevel Inverter Using Less Number of Power Switches

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ABSTRACT

This paper proposes a multilevel inverter that produces many steps in output voltage using fewer power electronic switches. The configuration of the proposed inverter is modular and extendable. The suggested topology consists of a combination of series-connected switching units and a conventional H-bridge converter. The presented multilevel inverter is analyzed in both symmetric and asymmetric configurations. Two different methods to determine the size of DC voltage sources of the asymmetric configurations are presented to achieve the maximum steps in the output voltage. The characteristics of both symmetric and asymmetric configurations are given and compared together in detail. The comparison results show that the asymmetric configuration with second design method uses less power switches and has less power losses than symmetric and first design method asymmetric configurations. However, it has more (Total Voltage Rating) TVR than two others. The comparison between symmetric configuration of the proposed multilevel inverter and four similar multilevel inverters shows that the proposed inverter uses fewer power switches and has less power losses. Finally, a laboratory prototype of the multilevel inverter is implemented and the experimental measurement results are given. The experimental measurement results validate proper operation of the proposed multilevel inverter.

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I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and DC voltage sources, the output of which generate voltages with staircase waveforms[1]. Multilevel inverters have become a new field of interest in industry and research. While the classical topologies have proved to be a viable alternative in a wide range of high-power medium-voltage applications, there has been an active interest in the evolution of newer topologies[2]. By increasing the number of levels in the multilevel inverters, the output voltages have more steps in staircase waveform, which has a reduced harmonic distortion. However, the increase in output voltage levels increases the number of devices that must be controlled[3].

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The first converter topology to produce multilevel voltage from various DC voltage sources was proposed by Baker and Bannister in 1970[4]. The topology consists of single-phase inverters connected in series that is known as cascaded H-bridge (CHB) inverter. In contrast to the CHB inverters, modified multilevel inverter topology was proposed in 1980 that can produce multilevel voltage from a single DC source with some diodes connected to the neutral point. This topology is known as the neutral point clamped (NPC) inverter or diode clamped topology[2]. Other well-known multilevel inverter known as flying capacitor was introduced in the 1990[5,6].

The cascaded H-bridge, diode clamped and flying capacitors topologies are referred to as the "classical topologies"multilevel inverters. Classical topologies have been analyzed more and more during paste decades[7–12]. However, beside their advantages, many researchers have focused on new topologies with more advantages during the recent decades. A multilevel topology based on dual two-level voltage source inverter to obtain a multilevel waveform thereby reducing grid side current harmonics and mitigating output voltage derivatives was introduced in[13]. A modification in the conventional cascaded H-bridge configuration using an active front end to solve regenerative mode of operation problem and effective control of the input current and output voltage was presented in[14]. In[15], presentation and implementation of a cascaded multilevel boost inverter for electric vehicle and hybrid electric vehicle applications without using of inductors and multiple power supplies, and utilizing a fundamental switching frequency modulation scheme was shown. The other important multilevel inverter topology is modular multilevel converter (MMC)[16]. MMC has become an attractive topology for medium and high power applications because of its several advantages such as modularity and redundancy.

A configuration of cascaded multilevel inverter in which each module is made up of full and half-bridges,

two isolated equal DC sources and a bidirectional auxiliary circuit is studied in[17]. In this configuration, one leg of the H-bridge and the half-bridge are cut and the related terminals are connected to the both ends of an equal split DC source. Each stage of presented inverter in[18] is composed of capacitor-based unit including two floating capacitors, one embedded DC voltage source and three power switches. In this inverter, the balanced voltage of integrated capacitors can be precisely provided as self-voltage balancing without using any auxiliary circuits or close-loop systems. A three-phase hybrid cascaded modular multilevel inverter topology which is derived from a modified configuration of H-bridge module is given in[19]. For renewable energy source such as photovoltaic (PV), it enables the tranformerless operation and enhances the power quality. A new multilevel inverter configuration which introduces a combination of cascaded H-bridge multilevel inverter with a double level circuit is introduced in[20]. The double level circuit is a half-bridge inverter when combined with a cascaded H-bridge multilevel inverter, increases the output voltage level to nearly twice that of a conventional cascaded H-bridge multilevel inverter.

In this paper, a new topology for multilevel inverter is presented. The proposed topology consists of series-connected switching units. The proposed multilevel inverter uses reduced number of switching devices. Symmetric and asymmetric configurations of proposed inverter are analyzed. The configuration and operation of proposed multilevel inverter make it suitable for operation of modular fuel cell (FC) stacks, motor drive systems and also, harmonic compensation. Finally, a laboratory scale prototype of the presented multilevel inverter is tested, and measurement results are given.

II. PROPOSED MULTILEVEL INVERTER CONFIGURATION

Configuration of proposed multilevel inverter is shown in Fig. 1 The proposed topology consists of series-connected basic switching units which are composed of a DC voltage source, a power transistor and a diode. Fig. 2a shows the basic unit for the proposed inverter. Basic switching units can be connected in series to increase the number of voltage level appears in the converter output, as shown in Fig. 2b.

Operation modes of the switching unit are shown in Fig. 3. As shown in this figure, the proposed switching unit has two operation modes. In these modes, the power switch and power diode operate complementary. In the first mode, when the power switch is off, the diode becomes forward biased through the DC voltage source and conducts the current. In this mode, unit output voltage, V_{dc}, is equal to zero. In the second mode, the switch is turned on, and the diode becomes reverse biased through the switch and voltage source, and then turns off and the unit output voltage is equal to V_j.

Operation of the extended configuration of switching

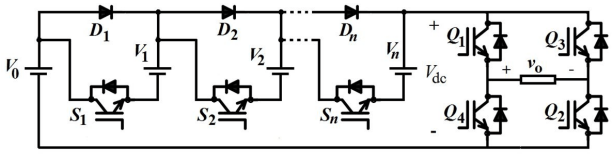
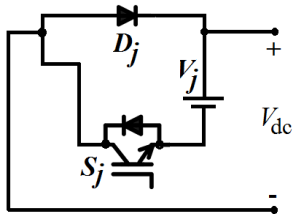
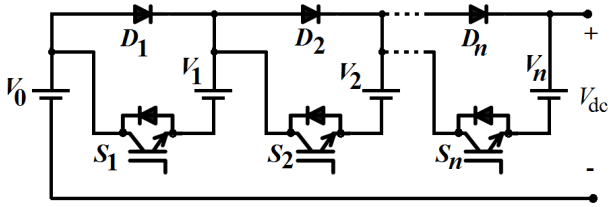


FIG. 1. Configuration of proposed multilevel inverter.



(a)



(b)

FIG. 2. **(a)** Basic unit for DC voltage source switching, **(b)** extended configuration of basic switching unit.

unit is similar to the operation of each switching unit so that, if a power switch does not receive any gate pulse, its complement diode conducts. When the power switch is turned on, its complement diode becomes reverse biased and turns off. As a result, the DC voltage source of the unit is connected in series with the previous DC voltage source. Therefore, it is possible to generate a multi-step DC voltage using the mentioned extended configuration.

The output voltage of the extended configuration is always positive. To operate as an inverter, the output voltage polarity should be changed in each switching cycle. To get this aim, a conventional H-bridge converter is added to output of the extended configuration. Considering the proposed multilevel inverter structure, it is realized that the generated multilevel voltage is provided using less number of power switches.

III. SYMMETRIC AND ASYMMETRIC CONFIGURATIONS OF PROPOSED MULTILEVEL INVERTER

A. Symmetric Configuration

In design of DC voltage source size for a multilevel inverter, it should be noted that all the voltage steps should be generated in the converter output using available volt-

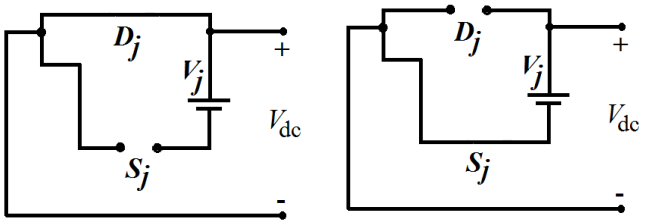


FIG. 3. Equivalent circuit of operation modes of proposed switching unit: **(a)** diode conduction, **(b)** switch conduction.

TABLE I. Switching states of symmetric configuration

State number	Unit. 1	Unit. 2	Unit. 3	Unit. n	Output voltage level, V_{dc}
1	D_1	D_2	D_3	D_n	V
2	S_1	D_2	D_3	D_n	$2\ V$
3	S_1	S_2	D_3	D_n	$3\ V$
4	S_1	S_2	S_3	D_n	$4\ V$
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
$n+1$	S_1	S_2	S_3	S_n	$(n+1)V$

age sources. The proposed inverter can have symmetric configuration such that all of the DC voltage sources have equal values. In this condition, with n number switching units, the number of output voltage steps is equal to (1).

$$N_{step} = 2n + 3, \quad n \geq 1 \tag{1}$$

The number of required power diodes, n_D, and power switches, n_{sw}, to generate a multilevel voltage with N_{step} steps are given in (2) and (3).

$$n_D = \frac{N_{step} - 3}{2}, \quad N_{step} \geq 5 \tag{2}$$

$$n_{SW} = \frac{N_{step} + 5}{2}, \quad N_{step} \geq 5 \tag{3}$$

Voltage and current ratings of switches are important factors in cost and size of inverter implementation. In multilevel inverters, the switches current rating equals to load current that is supplied. However, it is different for voltage ratings. In the symmetric configuration, the voltage rating of each switch in basic unit is equal to V, and voltage rating of H-bridge switches is equal to $(n+1)V$. Limitation of H-bridge switches in blocking the sum of all DC sources should be considered in converter design however, it should be noted that these switches operate in line frequency so, using the switches with high voltage rating extenuates this problem.

Switching states of the proposed multilevel inverter in symmetric configuration is given in Table I. Also, equivalent circuits of each generated voltage level in positive half-cycle of 9-level output voltage in symmetric configuration are illustrated in Fig. 4.

B. Asymmetric Configurations

To determine the size of DC voltage sources, purposes such as generation of maximum number of voltage level using minimum number of circuit components, generation of all voltage levels, and producing the less conduction losses during a switching cycle are considered.

To get the maximum number of voltage steps using minimum number of basic units beside the generation of all voltage steps, two different design methods are presented in the following:

First method: In the first method, the sizes of the first DC voltage source, V_0, and voltage source of the first unit, V_1, are equal to V, and the value of the rest of DC voltage sources is equal to $2V$. This algorithm is given in (4).

$$V_j = \begin{cases} V, & j = 0, 1 \\ 2V, & j \geq 2 \end{cases} \tag{4}$$

By applying of this method for the voltage sources, the number of output voltage steps is achieved as given in (5).

$$N_{step} = 4n + 1, \quad n \geq 1 \tag{5}$$

In this method, the total number of diodes and the total number of switches, required to generate N_{step} steps in the output voltage, are obtained as follow.

$$n_D = \frac{N_{step} - 1}{4}, \quad N_{step} \geq 5 \tag{6}$$

$$n_{SW} = \frac{N_{step} + 15}{4}, \quad N_{step} \geq 5 \tag{7}$$

The voltage rating of the first switch, S_1, is equal to V, and voltage rating of the rest of switches is equal to $2V$. H-bridge converter switches voltage rating is equal to $2nV$. In Table II, switching states of the multilevel inverter for first type asymmetric configuration is given.

Fig. 5 shows equivalent circuits of each generated voltage level in positive half-cycle of 13-level output voltage in asymmetric configuration with first design method.

Second method: In the second method for asymmetric configuration design, similar to the first type, the value of the first and the second DC voltage sources are equal to V, and for the rest of units, the values of DC voltage sources follow an arithmetic progression that is

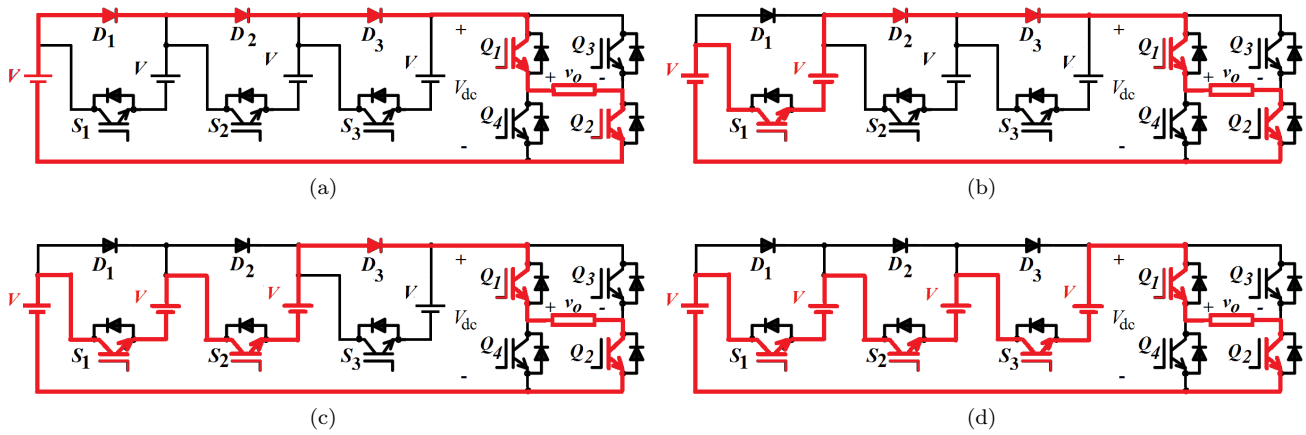


FIG. 4. Equivalent circuits of each generated voltage level in positive half-cycle of 9-level output voltage in symmetric configuration: **(a)** equivalent circuit of V voltage level, **(b)** equivalent circuit of 2 V voltage level, **(c)** equivalent circuit of 3 V voltage level, **(d)** equivalent circuit of 4 V voltage level.

given in (8).

$$V_j = \begin{cases} V, & j = 0, 1 \\ 2(j-1)V, & j \geq 2 \end{cases} \tag{8}$$

By applying of this method for sizing of DC voltage sources, the number of output voltage steps is equal to (9).

$$N_{\text{step}} = 2n^2 - 2n + 5 \quad , n \geq 2 \tag{9}$$

and the total number of diodes and switches, required to produce Nstep steps in the output voltage are calculated using (10) and (11).

$$n_D = \frac{1 + \sqrt{2N_{\text{step}} - 9}}{2}, \quad N_{\text{step}} \geq 5 \tag{10}$$

$$n_{SW} = \frac{9 + \sqrt{2N_{\text{step}} - 9}}{2}, \quad N_{\text{step}} \geq 5 \tag{11}$$

Similar to the previous method, the voltage rating of the first switch is equal to V, and voltage rating of switch in j^{th} unit is equal to $2(j-1)V$. Also, the voltage rating of H-bridge switches is equal to $(n^2-n+2)V$. Switching states of asymmetric configuration in the second method are given in Table III. In Fig. 6, equivalent circuits of each generated voltage level in positive half-cycle of 17-level output voltage with second design method are illustrated.

IV. POWER LOSS CALCULATION

Power losses of the switches in a multilevel inverter mainly include conduction loss and switching loss. In the low switching frequencies, the conduction losses are dominant. However, in the high switching frequencies,

TABLE II. Switching states of asymmetric configuration with first design method

State number	Unit. 1	Unit. 2	Unit. 3	Unit. n	Output voltage level, V_{dc}
1	D_1	D_2	D_3	D_n	V
2	S_1	D_2	D_3	D_n	2 V
3	D_1	S_2	D_3	D_n	3 V
4	S_1	S_2	D_3	D_n	4 V
5	D_1	S_2	S_3	D_n	5 V
6	S_1	S_2	S_3	D_n	6 V
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
$2n$	S_1	S_2	S_3	S_n	$2nV$

the switching losses become considerable. For a transistor with the anti-parallel diode, both the transistor and the diode have on-state resistance and on-state voltage which cause conduction losses. Although, their variation with temperature is considered constant to simplify analysis. Assume that the on-state voltages of the diode and transistor are V_T and V_D, respectively and their resistances are considered to be R_T and R_D, respectively. Instantaneous conduction loss of a diode, $P_{c,D}(t)$, and a transistor, $P_{c,T}(t)$, can be written as follow[21]:

$$p_{c,\,T}(t) = [V_T + R_T i^{\beta}(t)]i(t) \tag{12}$$

$$p_{c,\,D}(t) = [V_D + R_D i(t)]i(t) \tag{13}$$

where β is constant of the transistor, $i(t)$ is the instantaneous current through the transistor or diode. Considering that at the instant of t, there are N_T transistors and N_D diodes in the current path, the average value of the conduction power loss, P_c, of the multilevel inverter can

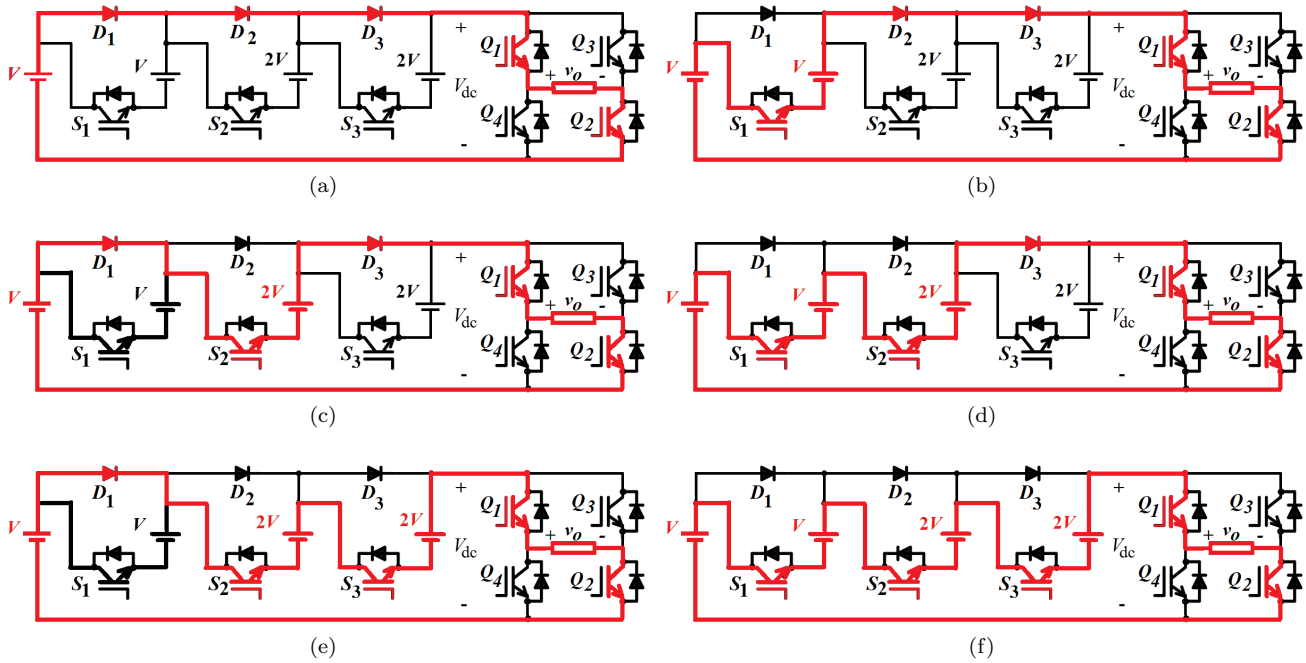


FIG. 5. Equivalent circuits of each generated voltage level in positive half-cycle of 13-level output voltage in asymmetric configuration with frist design method: **(a)** equivalent circuit of V voltage level, **(b)** equivalent circuit of 2 V voltage level, **(c)** equivalent circuit of 3 V voltage level, **(d)** equivalent circuit of 4 V voltage level, **(e)** equivalent circuit of 5 V voltage level, **(f)** equivalent circuit of 6 V voltage level.

be written as follows:

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} [N_T(t)p_{c,\,T}(t) + N_D(t)p_{c,\,D}(t)]dt \qquad (14)$$

To calculate the switching losses of the multilevel inverter, the energy lost during turn-on and turn-off period of a switch is calculated and then, it is extended for the multilevel inverter. Suppose that the voltage and current of a switch vary linearity during switching. Using this approximation, the lost energy during turn-on and turn-off period of a switch can be obtained as follow:

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}I\,t_{off} \qquad (15)$$

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}I^{'}\,t_{on} \qquad (16)$$

where, $E_{on,k}$ and $E_{off,k}$ are the lost energy during turn-on and turn-off period of the switch k, and t_{on} and t_{off} are the turn-on and turn-off times of the switch. Also, $V_{sw,k}$ is the voltage on the switch k before turning on or after turning off. I and $I^{'}$ are the currents through the switch k before turning off and after turning on, respectively. For the multilevel inverter, the switching power loss, P_{sw}, is equal to the sum of all turn-on and turn-off energy losses in a fundamental cycle of the output voltage. This can be written as follows:

$$P_{sw} = f\sum_{k=1}^{N_{switch}}\left(\sum_{i=1}^{N_{on,k}} E_{on,ki} + \sum_{i=1}^{N_{off,k}} E_{off,ki}\right) \qquad (17)$$

where f is the fundamental frequency, $N_{on,k}$ and $N_{off,k}$ are the numbers of turn-on and turn-off of the switch k during a fundamental cycle. Also, $E_{on,ki}$ is the energy loss of the switch k during the i^{th} turn-on, and $E_{off,ki}$ is the energy loss of the switch k during the i^{th} turn-off. The total power loss of the multilevel inverter, P_{loss}, is equal to the sum of the conduction and switching losses as given in (18):

$$P_{loss} = P_c + P_{sw} \qquad (18)$$

V. COMPARISON STUDY

A. Comparison of symmetric and asymmetric configurations

This section compares characteristics of symmetric and asymmetric configurations of proposed multilevel inverter. Maximum number of steps in output voltage versus number of switching units for symmetric and asymmetric configurations is shown in Fig. 7a. This figure

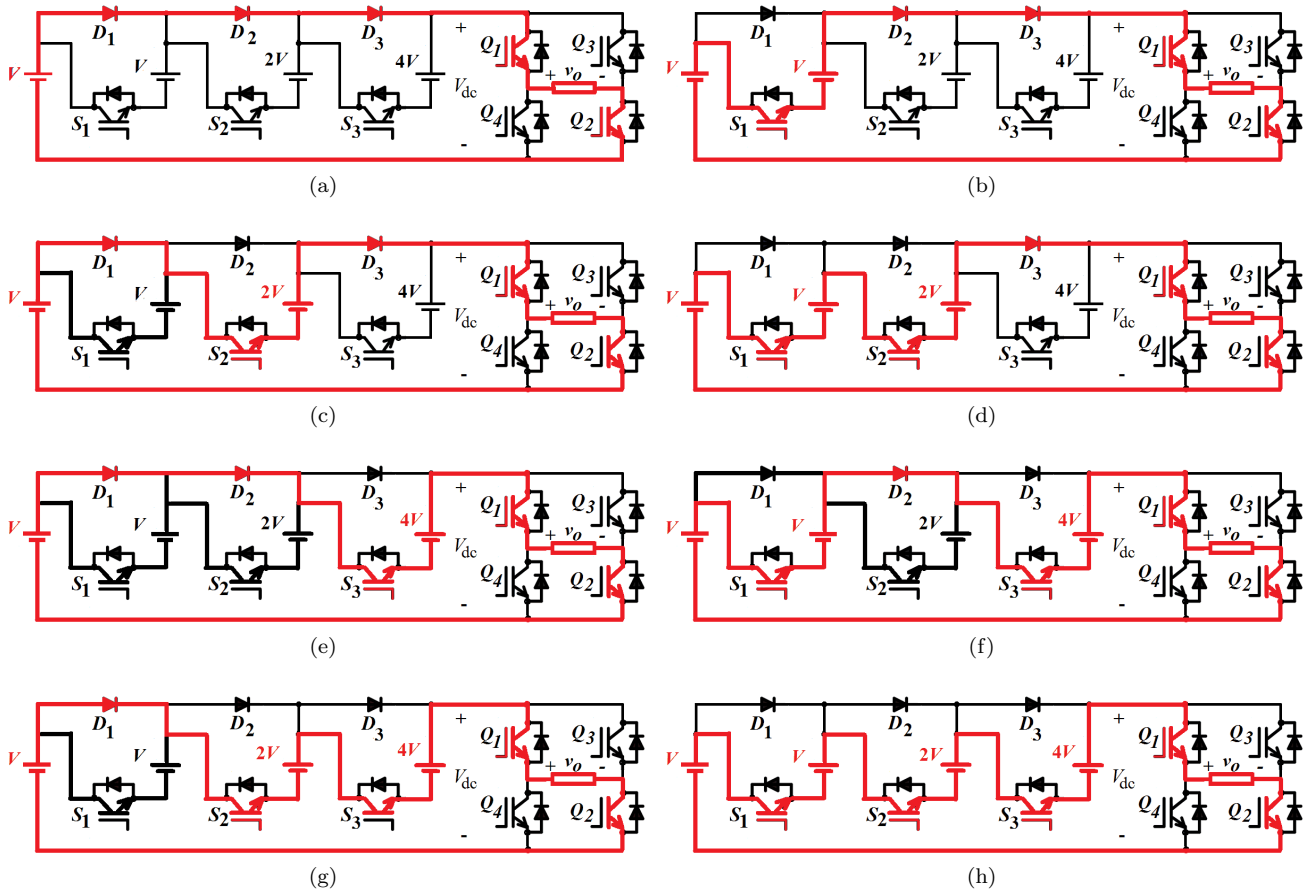


FIG. 6. Equivalent circuits of each generated voltage level in positive half-cycle of 17-level output voltage in asymmetric configuration with second design method: **(a)** equivalent circuit of V voltage level, **(b)** equivalent circuit of 2 V voltage level, **(c)** equivalent circuit of 3 V voltage level, **(d)** equivalent circuit of 4 V voltage level, **(e)** equivalent circuit of 5 V voltage level, **(f)** equivalent circuit of 6 V voltage level, **(g)** equivalent circuit of 7 V voltage level, **(h)** equivalent circuit of 8 V voltage level.

TABLE III. Switching states of asymmetric configuration with second design method

State number	Unit. 1	Unit. 2	Unit. 3	Unit. n	Output voltage level, V_{dc}
1	D_1	D_2	D_3	D_n	V
2	S_1	D_2	D_3	D_n	2 V
3	D_1	S_2	D_3	D_n	3 V
4	S_1	S_2	D_3	D_n	4 V
5	D_1	D_2	S_3	D_n	5 V
6	S_1	D_2	S_3	D_n	6 V
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
n^2-n+2	S_1	S_2	S_3	S_n	$(n^2-n+2)V$

shows when the number of switching units is increased, the increase in number of output voltage steps is remarkable for asymmetric configuration with second design method. Fig. 7b shows the number of power switches versus number of inverter output voltage steps. It is clear that the symmetric configuration needs the most number of power switches for a specified number of voltage steps, and asymmetric configuration with second design method needs the least.

Total voltage rating (TVR) of switches (sum of voltage rating of switches) in three configurations is compared in Fig. 7c. With increasing of switching units, TVR of asymmetric configuration with second design method shows the most increase with compared to the other configurations. As shown in Fig. 7d, power loss of the asymmetric configuration with second design method is less than symmetric configuration and asymmetric configuration with the first design method, especially when the number of output voltage steps is increased.

B. Comparison of proposed multilevel inverter with similar topologies

In this section, the proposed multilevel inverter is compared with conventional cascaded H-bridge (CHB) multilevel inverter and similar multilevel inverters presented in[22–24], all in symmetric configurations. As illustrated

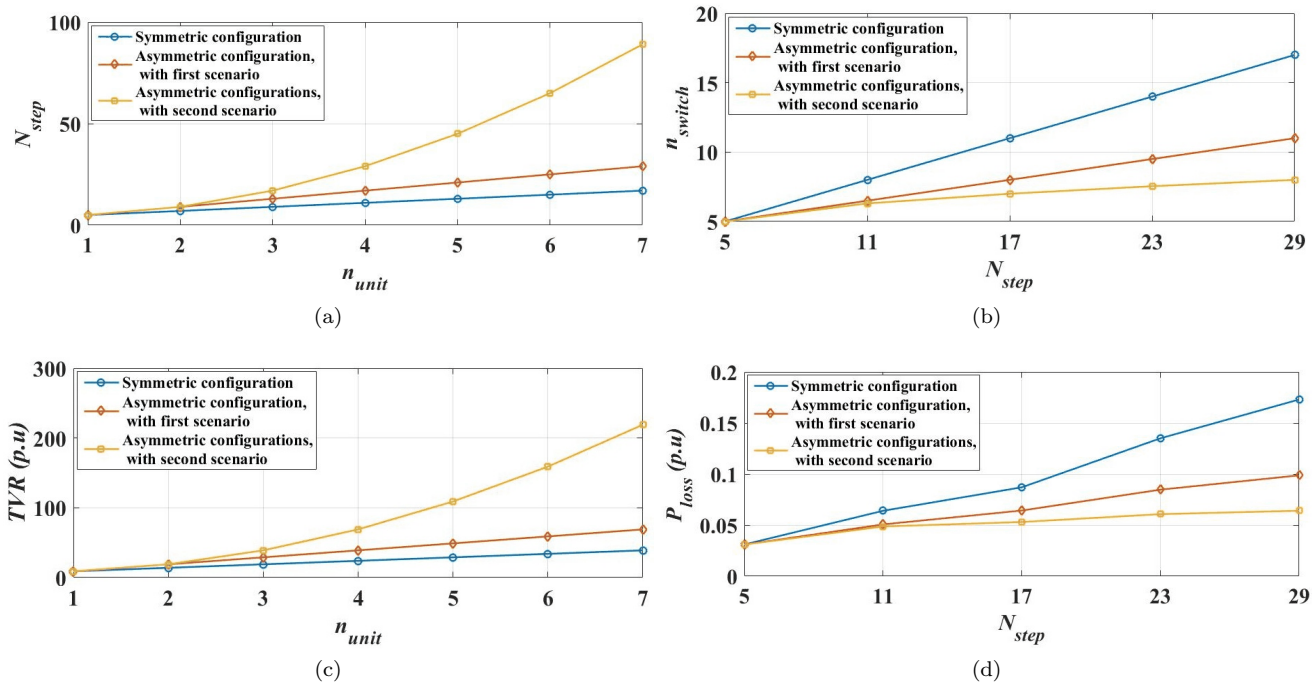


FIG. 7. Comparison of **(a)** number of output voltage steps versus number of units, **(b)** number of power switches versus output voltage steps, **(c)** TVR versus number of units, **(d)** power losses versus output voltage steps, in symmetric and asymmetric configurations of proposed multilevel inverter.

in Fig. 8, for a specified number of voltage steps, the proposed multilevel inverter needs less number of power switches than the other inverters, and it is considerable when the number of voltage steps is high. TVR of the CHB inverter is less than the other inverters, and next one, the proposed multilevel inverter has the acceptable TVR. The proposed multilevel inverter has less power loss with compared to CHB multilevel inverter and the multilevel inverter presented in[22] however, the multilevel inverters presented in[23] and[24] have less power losses than the proposed multilevel inverter. It is notable that the power loss of CHB multilevel inverter is remarkable when the number of voltage steps is high.

Another method for comparison purpose is the components per level factor (F_{cl}). If this factor value be high, the topology requires more number of components to achieve the desired output voltage level. Hence, the main purpose of new topologies is to decrease the factor value. This factor is defined as follows:

$$F_{cl} = \frac{n_{Sw} + n_D + n_C + n_{DC} + n_{Tsf} + n_X + n_{Drv}}{N_{Level}} \tag{19}$$

where n_{Sw}, n_D, n_C, n_{DC}, n_{Tsf}, n_{Drv}, n_X and N_{Level} are the number of switches, diodes, capacitors, DC sources, transformers, driver, other components and number of voltage level per phase, respectively. F_{cl} comparison for various voltage levels is performed among the proposed inverter topology and the inverter topologies presented in[22–24] and CHB configuration. The comparison results are given in Table IV. As given in the table, the proposed multilevel inverter uses the less component counts among the similar topologies.

VI. INVERTER SWITCHING ALGORITHM

In order to generate required voltage steps, a proper algorithm for inverter switching should be applied. The generated output voltage should have all steps and minimum total harmonic distortion (THD).

In order to have equal size for all voltage levels, the fundamental component and different harmonic components are obtained from the following equation[25]:

$$H_n = \begin{cases} \dfrac{4V_{dc}}{n\pi} \displaystyle\sum_{j=1}^{S} \cos(n\alpha_j), & n = 2k \\ 0, & n = 2k+1 \end{cases} \tag{20}$$

where V_{dc} is the amplitude of the each voltage step, S is the number of steps, and a_j is the optimized harmonic switching angles. The angles $_j$ are expressed using the following equation:

$$\alpha_j = \sin^{-1}\left(\frac{j - 0.5}{S}\right) \quad j = 1, 2, \cdots, S \tag{21}$$

Using the above algorithm, THD of the output voltage

TABLE IV. Comparison of F_{CL} among the proposed multilevel inverter and four similar topologies

N_{Level}	Topology	n_{Sw}	n_D	n_C	n_{DC}	n_{Tsf}	n_{Drv}	n_X	F_{cl}
5	CHB	8	0	0	2	0	8	0	3.6
	[22]	8	0	0	2	0	8	0	3.6
	[23]	8	0	0	2	0	8	0	3.6
	[24]	7	0	0	2	0	7	0	3.2
	Proposed	5	1	0	2	0	5	0	2.6
11	CHB	20	0	0	5	0	20	0	4.09
	[22]	14	0	0	5	0	14	0	3
	[23]	14	0	0	5	0	11	0	2.72
	[24]	12	0	0	5	0	12	0	2.63
	Proposed	8	4	0	5	0	8	0	2.27
17	CHB	32	0	0	8	0	32	0	4.23
	[22]	20	0	0	8	0	20	0	2.82
	[23]	20	0	0	8	0	14	0	2.47
	[24]	18	0	0	8	0	18	0	2.58
	Proposed	11	7	0	8	0	11	0	2.17
23	CHB	44	0	0	11	0	44	0	4.30
	[22]	26	0	0	11	0	26	0	2.73
	[23]	26	0	0	11	0	17	0	2.34
	[24]	24	0	0	11	0	24	0	2.56
	Proposed	14	10	0	11	0	14	0	2.13
29	CHB	56	0	0	14	0	56	0	4.34
	[22]	32	0	0	14	0	32	0	2.68
	[23]	32	0	0	14	0	20	0	2.27
	[24]	30	0	0	14	0	30	0	2.55
	Proposed	17	13	0	14	0	17	0	2.10

is equal to (22).

$$THD = \frac{\sqrt{\sum_{n=3,5,\cdots}^{\infty} V_n^2}}{V_1} = \sqrt{\left(\frac{V_O}{V_1}\right)^2 - 1} \qquad (22)$$

where

$$V_O = \frac{2\sqrt{2}V_{dc}}{\pi}\sqrt{\sum_{n=1,3,5,\cdots}^{\infty}\left(\sum_{j=1}^{S}\frac{\cos(n\alpha_j)}{n}\right)^2} \qquad (23)$$

$$V_1 = \frac{2\sqrt{2}V_{dc}}{\pi}\sum_{j=1}^{S}\cos\alpha_j \qquad (24)$$

Where V_O is the RMS value of output voltage, and V_n is the RMS value of n^{th} harmonic component of output voltage.

VII. EXPERIMENTAL MEASUREMENT RESULTS

Proposed multilevel inverter with three switching units is implemented as shown in Fig. 9. IRFP250 Power MOSFETs are used in the implemented prototype. Driver circuit of each switch consists of an opto-isolator, a Schmit trigger, and a buffer. Each switch requires an isolated driver circuit. The isolation can be provided using either pulse transformers or opto-isolators. Opto-isolators can work in a wide range of input signal pulse width, but a separate isolated power supply is required for each switching device. The opto-isolator-based gate driver circuit is used in the prototype inverter.

Fig. 10-12 show the experimental measurement results of the inverter output voltage and current. In the tests, the load is a series RL load ($R = 150\ \Omega$ and $L = 65\ mH$). In the first study, the symmetric configuration for the proposed multilevel inverter is considered. The converter is adjusted to produce a $50 - Hz$, 9-level staircase waveform with 30 V in each step. Since the load of the converters is almost a low-pass filter, the output current contains less high-order harmonics than the output voltage. Fig. 10a shows 9-level staircase waveform of output voltage, and Fig. 10b shows related current waveform.

To generate a desired output waveform with better quality, the number of the output voltage steps should be increased. To get this aim, the second study is devoted to the proposed inverter with asymmetric configuration as its DC voltage sources are adjusted based on the first design method. Fig. 11a and 11b show $50 - Hz$, 13-level staircase waveforms of output voltage and output current, respectively. In this study, the value of V_{dc} is 30 V. In the third study, asymmetric configuration of multilevel inverter with second design method is considered. In this study, the value of V_{dc} is 20 V. Fig. 12 shows a $50 - Hz$, 17-level staircase waveform of output voltage, and its related current waveform.

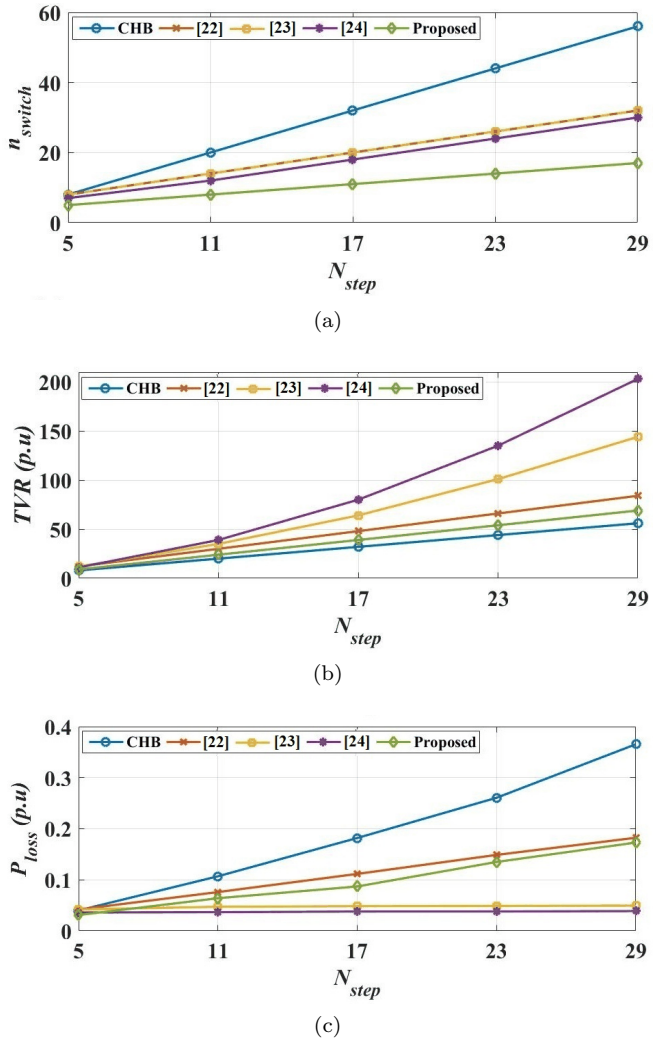


FIG. 8. Comparison of **(a)** number of power switches, **(b)** TVR, **(c)** power losses versus output voltage steps, in proposed multilevel inverter with CHB and presented multilevel inverters in[22–24].

As shown in these figures, the measurement results verify the ability of the suggested topology in generation of desired multilevel voltage waveforms.

VIII. CONCLUSIONS

In this paper, a new configuration for multilevel inverters is presented. The converter can be designed both in symmetric and asymmetric configurations. The analysis shows that to achieve more steps in the output staircase waveform, it is possible to add more cascaded symmetric basic units or use asymmetric configurations. This paper proposes two different methods to design asymmetric configurations and get better quality of output voltage with less number of power switches and DC voltage sources. The comparison between symmetric and asymmetric configurations of the suggested multi-

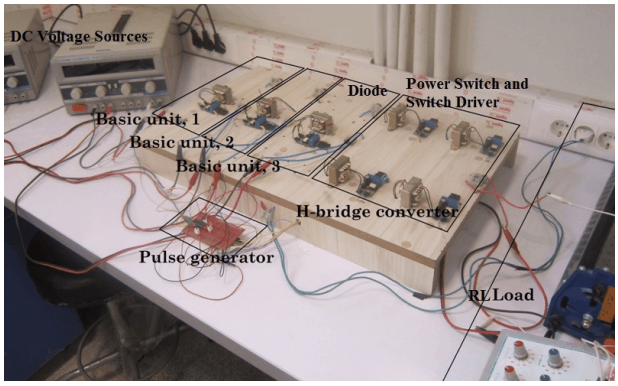


FIG. 9. Implemented prototype of proposed multilevel inverter.

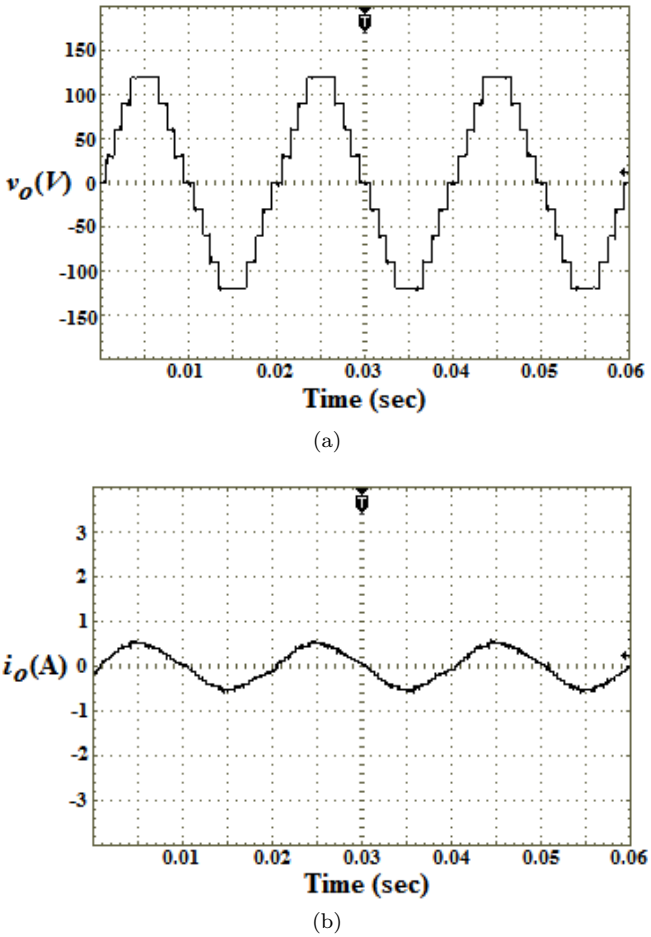
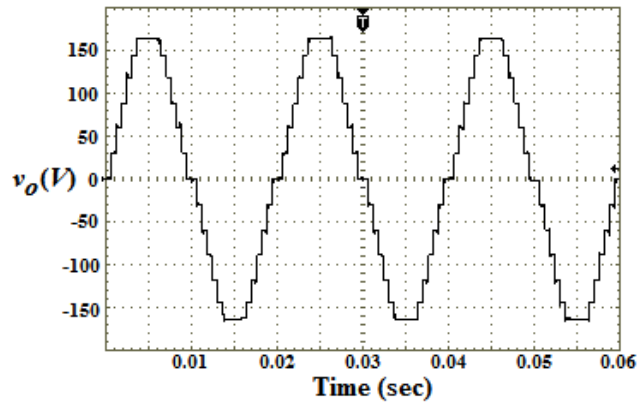
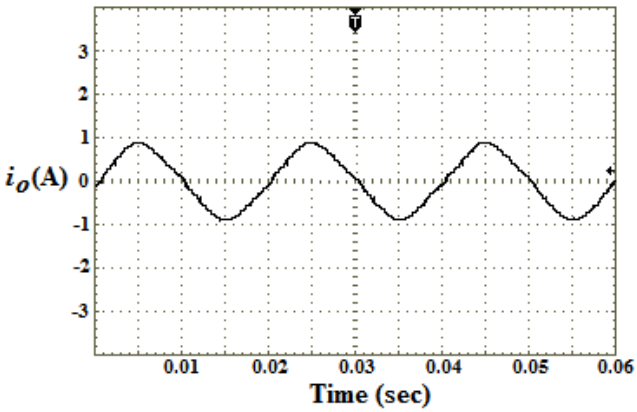


FIG. 10. 9-level: **(a)** output voltage and **(b)** output current of symmetric configuration.

level inverter shows that the asymmetric configuration with second design method uses less power switches and has less power losses than symmetric and first design method asymmetric configurations. However, it has more TVR than two others. The comparison between symmetric configuration of the proposed multilevel

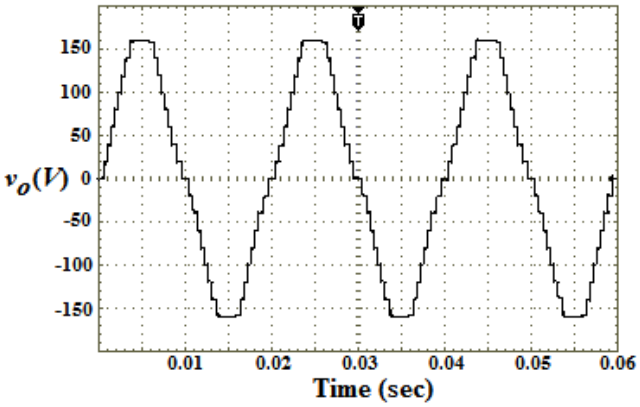


(a)

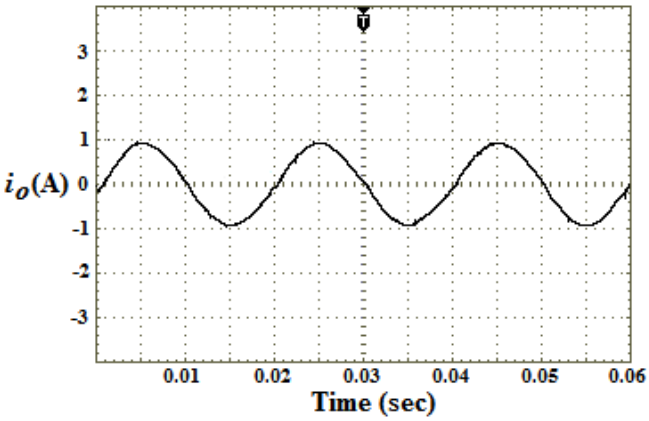


(b)

FIG. 11. 13-level: **(a)** output voltage and **(b)** output current of first type asymmetric configuration.



(a)



(b)

FIG. 12. 17-level: **(a)** output voltage and **(b)** output current of second type asymmetric configuration.

inverter and four similar multilevel inverters shows that the proposed inverter uses less power switches and has less power losses. However, the need for several isolated DC voltage sources, unidirectional power flow and limitation on more extension due to high blocking voltage of H-bridge converter switches are the main drawbacks of the proposed multilevel inverter. A laboratory prototype of the suggested multilevel inverter both in symmetric and asymmetric configurations has been implemented, and experimental measurement results have been given to validate the inverter capability in generating staircase waveforms.

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