A new topology of the switched-inductor/capacitor quasi Z-source inverter with ability of uplifted-boost

Alireza Karbalaei¹, Mohammad Mardaneh²,†, and Mokhtar Shasadeghi³

¹,²,³ Department of Electrical and Electronics Engineering, Shiraz University of Technology, Shiraz, Iran

In this paper, a new topology of switched-inductor/capacitor quasi impedance source inverter is suggested, which in comparison with the other topologies possesses higher boost voltage inversion at high modulation index and low shoot through duty cycle. Also, this topology has features like continuous input current, common ground between the input source and the inverter bridge and, low shoot-through current. To express the proposed topology properties, it is compared experimentally in similar conditions relative to the Enhances Boost quasi Z-Source inverter (EB-qZSI). Similar to the EB-QZSI, because of the presence of a series inductor with input voltage source, the inrush current at start-up is limited in the proposed topology. Also, the low voltage stress on the capacitors and the low current ripple of the inductors and the input source are other advantages. Due to the lower number of diodes in the proposed inverter, the efficiency is higher compared to the EB-qZSI inverter. The performance of the proposed topology is confirmed with MATLAB/SIMULINK software. The results of simulation and experimental validate the theoretical analysis of the proposed topology. The experimental results validate the simulation results and there is a good agreement between the simulation results and the experimental results.

Article Info

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I. INTRODUCTION

In recent years, the researchers have performed extensive research in order to improve the structure of impedance source inverters. Although there is a wide application of voltage source inverter (VSI) and current source inverter (CSI) [1], [2] in the industry, they have problems such as; the lack of buck-boost capabilities that require power conversion in two steps [3]. Therefore, to eliminate the output voltage limitation, it is necessary two-stage conversion with additional converter, the creation of dead time in order to avoid short circuit of the voltage source, and vulnerability to EMI noise that reduces the reliability of the inverter [4],[5]. In 2003, the Impedance Source Inverter (ZSI) was introduced, which was able to overcome the disadvantages of traditional inverters of voltage and current source. The structure of this inverter is composed of an X-shaped network that connects the converter's main circuit to the power supply [6].

These inverters have advantages such as applying as a buck and boost converter in the form of one structure, there is no limitation like dead time and overlap time for VSI and CSI, respectively, suitable performance against noise. This structure is used in all ac-ac, dc-ac, dc-dc, ac-de power stage with buck-boost capability [7]. With all the good advantages of ZSI, but this topology has major disadvantages such as the lack of share common ground between the input power source and the link-dc, the discontinuous input current due to the input diode. In 2008, the quasi impedance source inverters (qZSI) was introduced [8], which included advantages such as, common ground between the input power source and link-dc, the low voltage stress on capacitors and continuous input current. In 2010, diode-assisted qZSI (DA-qZSI) and capacitor-assisted qZSI(CA-qZSI) topologies were proposed [9], which have higher boost factor relative to previous structures. Another feature of these structures is their extensibility, that the boost factor can be increased by adding elements to the base structure. The CA-qZSI topology is shown in Figure 1(a). By replacing the switched-inductor (SL) cell instead of the inductors of ZSI and qZSI, the boost factor and voltage gain increase considerably [10], [11], [12]. The SL cell in these structures consists of a combination of three diodes and two inductors.
Fig. 1. (a). CA-qZSI.  
Fig. 1. (b). SL-ZSI.  
Fig. 1. (c). cSL-qZSI.  
Fig. 1. (d). Enhance boost qZSI (EB-qZSI).  
Fig. 1. (e). ESL-qZSI.

Although SL-ZSI has higher boost factor than previous structures, it has disadvantages such as discontinuous input current, lack of common ground between the input source and bridge inverter and start-up inrush current. SL-qZSI topology, in addition to solving SL-ZSI problems, also has lower voltage stress on capacitors. The SL-ZSI topology is shown in Fig. 1(b). In [13], two other types of structures have been proposed; the ripple input current switched-inductor quasi-Z-source inverter (rSL-qZSI) and the continuous-input current switched-inductor quasi-Z-source inverter (cSL-qZSI). These structures in the same conditions with the SL-qZSI, possess lower voltage stress on the capacitor, and suppression of start-up inrush current. Fig. 1(c) shows the cSL-qZSI structure. In [14] and [15], enhanced boost ZSI (EB-ZSI) and enhanced boost qZSI (EB-qZSI) topologies were proposed, respectively, which have a high boost factor. But, the structure of enhanced boost ZSI has disadvantages such as discontinuous input current, the high voltage stress on capacitors, lack of common ground between the input source and the inverter bridge, and the problem of startup inrush current [16], while, the enhanced boost qZSI structure overcome these problems. This topology is shown in Fig. 1(d). The extended switched/inductor quasi-Z-source inverter (ESL-qZSI) was proposed that, compared with the SL-qZSI topology, has advantages such as higher voltage gain and lower voltage stress [17]. In 2018 [18], two other topologies, called embedded switched-inductor qZSI (ESL-qZSI) an improved embedded switched-inductor qZSI (iESL-qZSI), were proposed. The low ripple current of the inductors, the low voltage stress on the capacitors, and the high boost factor and their symmetry are the advantages of these topologies. The ESL-qZSI topology is shown in Fig. 1(e).

This paper proposes a topology that, in the same conditions with other topologies, has advantages such as high boost factor and high voltage gain in the high modulation index and low shoot through duty cycles, the low voltage stress on capacitors, low shoot through current, and high efficiency. Other advantages of this topology include the continuous input current, suppressed start-up inrush current, and common ground between the input source and the bridge inverter.

II. PROPOSED TOPOLOGY

According to Fig. 2, the proposed structure can be divided into two parts. The first part is related to the inductor/capacitor-switched cells, and the second part is related to the impedance network. In the first part, the proposed structure has two inductor/capacitor switched cells, which one of the cells with the input voltage source consists of two inductors \((L_1\) and \(L_3\)), two diode \((D_1\) and \(D_4\)) and capacitor \((C_3)\). And the other cell can be likened to a semi-cell, consisting of capacitor \((C_2)\), inductor \((L_2)\), and a diode \((D_2)\) and the inductor \((L_2)\). The second section has three capacitors \((C_1, C_2, \text{ and } C_4)\), and diode \((D_3)\). In total, the proposed structure has four inductors, four diodes which couples voltage source \(V_{i}\) to inverter bridge, and five capacitors. Compared to similar structures like EB-qZSI and ESL-qZSI, this structure has one fewer diodes but an additional capacitor. In TABLE. I the suggested topology compared with other topologies in terms of the number of elements.

A. Circuit Analysis

The operating principles of this structure are the same as the base (q)ZSI. Therefore, it includes shoot-through zero states, six active states and two zero states. For easier analysis
Table I
Comparison of the number of elements used in the proposed topology with other topologies

<table>
<thead>
<tr>
<th>No. of components</th>
<th>CA-qZSI</th>
<th>DA-qZSI</th>
<th>SL-ZSI</th>
<th>cSL-qZSI</th>
<th>rSL-qZSI</th>
<th>Enhanced Boost</th>
<th>ESL-qZSI</th>
<th>iESL-qZSI</th>
<th>Proposed structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Inductor</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Diode</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>Power switch</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
</tbody>
</table>

Fig. 2. Proposed topology.

the operating states can be considered as shoot-through and non-shoot-through states \((N \cdot ST)\). Fig. 3a shows the equivalent circuit of shoot through the state \((ST)\). During \(ST\), both the upper and lower switches of inverter main circuit in one leg or two legs and or all three legs are on. Therefore, the diodes \(D_2, D_3, D_4\) are off, but the \(D_1\) diode is on. By writing the relations of \(KVL\) in the circuit of Fig. 3a, the voltage relations of inductors in terms of capacitor voltages are obtained as follows. In this case, the dc-link voltage is zero.

\[
\begin{align*}
V_{L_1} & = V_{C_2} + V_{C_5} \\
V_{L_2} & = V_{C_1} + V_{C_3} \\
V_{L_3} & = V_{C_4} \\
V_{L_4} & = V_{C_1} + V_{C_2} \\
V_{dc,max} & = 0
\end{align*}
\]

(1)

In accordance with Fig. 3 (b), in \(N \cdot ST\), the diodes \(D_2, D_3, D_4\) and \(D_4\) are on and the \(D_1\) diode is off. Similarly, the voltage relations of the inductors can be obtained in terms of the capacitor voltages as follows.

\[
\begin{align*}
V_{L_1} & = V_{C_5} - V_{C_1} \\
V_{L_2} & = V_{C_1} - V_{C_4} \\
V_{L_3} & = -V_{C_3} \\
V_{L_4} & = V_{C_1} - V_{C_5} \\
V_{dc,max} & = V_{C_1} + V_{C_2}
\end{align*}
\]

(2)

Using the volt-sec balance principle and under steady state condition, the average voltage of the inductor \(L_1\) is equal to zero, so:

\[
V_{C_2} = (1 - D)V_{dc,max} - V_{C_5}
\]

(4)

And also, in steady-state, the average voltage of the inductor \(L_2\) is zero and considering the volt-sec balance principle for \(L_2\) gives:

\[
V_{C_1} = (1 - D)V_{dc,max} - V_{C_3}
\]

(5)

In steady-state condition, the average voltage of the inductor \(L_3\) is zero and applying volt-second principle for \(L_3\) gives:

\[
V_{C_4} = \frac{(1 - D)}{D}V_{C_3} = (1 - D)V_{dc,max}
\]

(6)

In the above relation, the capacitor voltage \(C_3\) in terms of the dc-link voltage is as follows:

\[
V_{C_3} = DV_{dc,max}
\]

(7)

In steady-state condition, the average voltage of the inductor \(L_4\) is zero and considering the volt-sec balance principle for \(L_4\) gives:

\[
V_{C_1} = (1 - D)V_{dc,max} - V_{C_5}
\]

(4)
\[ V_{C2} = \frac{DV_{C2} + V_i}{1 - D} \]  

(8)

By replacing (8) in (4), \( V_{C2} \) is derived:

\[ V_{C2} = (1 - D)^2V_{dc,max} - V_i \]  

(9)

By replacing relation (7) in (5), the voltage on capacitor \( C_i \) is obtained in terms of the dc-link voltage.

\[ V_{C1} = (1 - 2D)V_{dc,max} \]  

(10)

Finally, by replacing the relations (9) and (10) in (3), the boost factor of the proposed topology is obtained as follows:

\[ B = \frac{V_{dc,max}}{V_i} = \frac{1}{1 - 4D + D^2} \]  

(11)

In Table II and Fig. 4, the comparison of the boost factor of proposed structure with other structures has been done, which indicates that the higher boost factor of the proposed structure than the other structures in the same input voltage and shoot-through duty cycle. So, in the proposed structure in shoot through duty cycle of 0.2, 0.21 and 0.25, the boost factors will be 4.17, 4.9 and 16, respectively.

In various papers, several PWM control techniques such as sine-PWM (SPWM) control for impedance source inverters have been proposed, whose aim is to achieve a wide area of modulation, simple implementation, loss of commutation for each switching period, and low stress on the system [19]. SPWM techniques include simple boost control, maximum boost control, and constant maximum boost control, and simple boost control technique is the fundamental technique among them [20], [21], [22]. The relation between \( M \) and \( B \) depends on the type of PWM control strategy. To control switches in this topology, the simple boost PWM method is used. In this control method, there are two shoot-through states in each switching period. As shown in Fig. 5, by adding two positive \( (V_p) \) and negative \( (V_n) \) signals to the traditional PWM, the shoot through state (ST) is generated. These signals can be greater than or equal to the positive maximum of sinusoidal reference waves, and or can be equal to or less than the negative maximum of sinusoidal reference waves. The peak-phase output voltage of the three-phase inverter is expressed as follows:

\[ v_{an,max} = M \cdot \frac{V_{dc,max}}{2} \]  

(12)

Where \( M \) is the amplitude modulation index. By replacing relation (11) in (12), the peak-phase output voltage in terms of the boost factors \( (B) \) can be derived as:

\[ v_{dc,max} = M \cdot B \cdot \frac{V_i}{2} \]  

(13)

In the above relation, the product of \( M \cdot B \) is the voltage gain \( (G) \) of the inverter. Given that, the simple boost PWM control method, modulation index \( (M) \) relative to the shoot-through duty cycle \( (D) \) is \( 1 - D \); therefore, the voltage gain relative to \( M \) in the proposed structure can be obtained as follows:

In Fig. 6 and Table II, the voltage gain of the proposed structure is compared with other structures. As can be seen, the proposed structure has a higher voltage gain than the other structures at the same input voltage and shoot through duty cycle.
C. Comparison of Voltage Stress on Capacitors and Diodes

Reduction of power electronic converters [23-25]. The voltage stress relations of the proposed structure capacitors are obtained as follows.

With the substitution of relation (11) in (10), the relation of the voltage stress on the capacitor $C_1$ can be found as:

$$V_{C1} = \frac{1 - 2D}{1 - 4D + D^2} V_i$$

By the substitution of the relation (11) in (9), the relation of the capacitor voltage $V_{C2}$ is obtained:

$$V_{C2} = \frac{2D}{1 - 4D + D^2} V_i$$

Similarly, by substituting relation (11) in relations (7) and (6), voltage stresses are found on capacitors $C_3$ and $C_4$, respectively:

$$V_{C3} = \frac{D}{1 - 4D + D^2} V_i$$

$$V_{C4} = \frac{1 - D}{1 - 4D + D^2} V_i$$

And also, by substituting the (16) in (8), $V_{C5}$ is obtained:

$$V_{C5} = \frac{1 - 3D}{1 - 4D + D^2} V_i$$

A comparison of the voltage stress on the capacitors in the proposed structure and EB-qZSI structure has been carried out. As shown in Fig. 7, voltage stresses are almost equal in most capacitors, and only on the capacitor $C_4$ of the proposed structure has higher than the other capacitors in both structures. Table II shows the voltage stress relations on capacitors in different structures.

In Fig. 8, the diodes voltage stress of the proposed structure is compared with those of EB-qZSI and iESL-qZSI. By applying KVL in the circuits of Fig. 2 (a) and 2 (b), the stress of the diodes in terms of input voltage can be obtained as follows:

$$V_{D1} = -\frac{D}{1 - 4D + D^2} V_i$$

$$V_{D2} = V_{D3} = -\frac{1}{1 - 4D + D^2} V_i$$

$$V_{D4} = -\frac{1 - D}{1 - 4D + D^2} V_i$$

As can be seen in Fig. 8, the voltage stress of the $D_1$ diode of the proposed structure is equal to the diodes $D_{1,2}$ of the ESL-qZSI structure and the diodes $D_{3,4}$ of the EB-qZSI structure and lower than the other diodes. Also, the voltage stress of the diode $D_4$ of the proposed structure equal to the stress of the diodes $D_{3,4}$ of the ESL-qZSI structure and the $D_{1,2}$ diodes of the EB-qZSI structure. However, the voltage stress on diodes $D_{2,3}$ of the proposed structure is larger than the other diodes and less than the diodes $D_{1,2}$ of the iESL-qZSI structure.

D. Current Ripple of Inductors and Voltage Across Inductors

The voltage across the inductors is calculated using the relations of shoot-through (ST) and non-shoot-through (N-ST) states. Therefore, by replacing the voltage stresses of the capacitors in (13) and (14) for the ST and N-ST states, the voltage across the inductors is obtained for both states.

For ST state:

$$V_{L1} = V_{L2} = V_{L3} = \frac{1 - D}{1 - 4D + D^2} V_i$$

$$V_{L4} = \frac{(1-D)^2}{1 - 4D + D^2} V_i$$

And similarly for N-ST state:

$$V_{L1} = V_{L2} = V_{L3} = -\frac{D}{1 - 4D + D^2} V_i$$

$$V_{L4} = -\frac{D(1-D)}{1 - 4D + D^2} V_i$$

The relation between voltage and current of the inductor can be expressed as follows:

$$V_L = L \frac{di}{dt}$$

Accordingly, by replacing the relations (23) and (24) in (25), and also, considering that in the simple boost control method
in each switching cycle the ST state occurs twice, the current ripple of the inductors is obtained as follows.

\[ \Delta I_{L1} = \Delta I_{L2} = \Delta I_{L3} = \frac{D(1 - D)}{1 - 4D + D^2} \frac{V_i}{2L_fS} \]  

(28)

\[ \Delta I_{L4} = \frac{D(1 - D)^2}{1 - 4D + D^2} \frac{V_i}{2L_fS} \]  

(29)

And similarly for N-ST state:

\[ \Delta I_{L1} = \Delta I_{L2} = \Delta I_{L3} = \frac{D(1 - D)}{1 - 4D + D^2} \frac{V_i}{2L_fS} \]  

(30)

\[ \Delta I_{L4} = \frac{D(1 - D)^2}{1 - 4D + D^2} \frac{V_i}{2L_fS} \]  

(31)

Assuming the inverter is ideal, accordingly, the input and output power must be equal. As a result, in a pure resistance load, the input current relation will be equal to:

\[ I_{in} = \frac{3M^2}{(1 - 4D + D^2)^2} \frac{V_i}{2BR} \]  

(32)

Fig. 9 and Table II show the comparison of volt-sec (flux) curves [15] relative to the voltage gain for inductor of the proposed structure and other structures. According to this figure, volt-sec in the inductor \( L_4 \) is more than \( L_1 \) and \( L_2 \) inductors of the structures EB-qZSI, ESL-qZSI, iESL-qZSI and less than the inductors \( L_3 \) and \( L_4 \) of the same structures. And also, the volt-sec of the inductors \( L_1 \), \( L_2 \) and \( L_3 \) is less than the inductors of all structures.

III. SIMULATION RESULTS

Simulations with the MATLAB / SIMULINK software have been performed to confirm the above analysis. Figure 10 shows the simulation results at \( D = 0.2 \), \( M = 0.8 \) and \( V_i = 48 \) V, simulation results of the proposed inverter are presented using a simple boost control method. As shown in Fig. 10 (a), the maximum dc-link voltage, the voltage stress on \( C_s \), as well as the dc-link average current \( (I_{d}) \) are 200 V, 40 V, and 1.7 A, respectively. The simulation waveforms of the line-voltage \( (V_{ab}) \), the phase voltage before the \( LC \) filter \( (V_{pm}) \), also the voltage and phase current after the \( LC \) filter \( (V_{in} \) and \( I_{pm} \) are shown in Fig. 10 (b). All the simulation results confirm the relations obtained with the analysis of the

Table II

Comparison of boost factor, voltage gain, voltage stress on capacitors and diodes, inductors current ripple in proposed structure with other structures.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Parameter</th>
<th>DA-qZSI</th>
<th>CA-qZSI</th>
<th>SL-ZSI</th>
<th>cSL-qZSI</th>
<th>rSL-qZSI</th>
<th>Enhanced boost qZSI</th>
<th>ESL-qZSI</th>
<th>iESL-qZSI</th>
<th>Proposed Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitors</td>
<td>( C_1 )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
</tr>
<tr>
<td>Current</td>
<td>( L_1 )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
</tr>
<tr>
<td>Current</td>
<td>( L_2 )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
</tr>
<tr>
<td>Current</td>
<td>( L_3 )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
</tr>
<tr>
<td>Current</td>
<td>( L_4 )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
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<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
<td>( D(1 - D) ) ( \frac{V_i}{2L_fS} )</td>
</tr>
<tr>
<td>Current</td>
<td>( D_{L_1} )</td>
<td>( D_{L_2} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_3} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_4} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_5} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_6} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_7} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_8} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_9} ) ( \frac{V_i}{2L_fS} )</td>
<td>( D_{L_10} ) ( \frac{V_i}{2L_fS} )</td>
</tr>
<tr>
<td>Boost Factor</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
<td>( 1 )</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>( M )</td>
<td>( M )</td>
<td>( M )</td>
<td>( M )</td>
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<td>( M )</td>
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</tbody>
</table>

Fig. 9. Flux (volt-sec) comparison of the inductors.
proposed structure. For a more straightforward comparison, the relations derived from the proposed structure with other structures, are shown in Table II.

Fig. 10. (a). dc-link voltage, input current \( I_{\text{in}} \), shoot through current \( I_{\text{sh}} \), and capacitor voltage \( V_{\text{C3}} \).

Fig. 10. (b). line-voltage and phase-voltage before of the LC filter repeatedly, phase and phase current \( V_{\text{bn}} \) and \( I_{\text{bn}} \).

IV. Experimental results

A laboratory sample is made in accordance with Fig. 11. The obtained experimental results confirm the curves and relations established from simulation and analysis. Fig. 12 shows experimental results for the proposed topology with \( V_i = 48 \), \( D = 0.2 \) and \( M = 0.8 \). As can be seen, there is a good match between experimental values with simulation and theoretical ones. It indicates that the proposed structure has a high boost factor and the dc-link voltage has increased to 190V. The voltage stress on capacitors \( C_{1-5} \) are 118V, 76V, 37V, 156V and 78V, respectively. Table III illustrates experimental and simulation parameters.

Fig. 11. Photograph of the experimental setup of the proposed topology.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbols</th>
<th>Simulation</th>
<th>Experiment</th>
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<tr>
<td>fundamental frequency</td>
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<td>50 Hz</td>
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<tr>
<td>Switching frequency</td>
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<td>13500 Hz</td>
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<td>Z-Source network and switched inductor/capacitor</td>
<td>( L )</td>
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<td>1 mH</td>
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<tr>
<td></td>
<td>( C )</td>
<td>1000 ( \mu )F</td>
<td>1000 ( \mu )F</td>
</tr>
<tr>
<td>Three-Phase output filter</td>
<td>( L_f )</td>
<td>1 mH</td>
<td>1 mH</td>
</tr>
<tr>
<td></td>
<td>( C_f )</td>
<td>10 ( \mu )F</td>
<td>10 ( \mu )F</td>
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<tr>
<td>Input DC voltage</td>
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<td>48 V</td>
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<tr>
<td>Modulation Index</td>
<td>( M )</td>
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<tr>
<td>Boost Factor</td>
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<td>2.5</td>
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<tr>
<td>Three-Phase Resistive load</td>
<td>( R )</td>
<td>47( \Omega )/Phase</td>
<td>47( \Omega )/Phase</td>
</tr>
</tbody>
</table>

Fig. 12. (a) dc-link voltage, input current \( I_{\text{in}} \).
Experimental results of the proposed topology with $D = 0.2$, $M = 0.8$, $V_i = 48V$ and $R_{load} = 47\Omega$. From top to bottom: (a)dc-link voltage, input current ($i_{in}$), (b)inductor currents ($L_2, L_3$), (c)capacitor voltage ($C_3$), inductor current ($i_{L1}$), (d)capacitor voltages ($C_3, C_4$ respectively), (e)capacitor voltages ($C_2, C_1$ respectively), (f)diode voltages ($D_2, D_4$ respectively), (g)diode voltages ($D_3, D_4$ respectively), (h)inductor voltages ($L_1, L_2$ respectively), (i)inductor voltages ($L_3, L_4$ respectively), (j)shoot through current ($i_{sh}$), (k)line-voltage ($v_{bc}$), and phase voltage ($v_{bn}$).
currents \( (L_2, L_3) \), (c). capacitor voltage \( (C_3, C_4) \), inductor current \( (i_{L_3}) \), (d). capacitor voltages \( (C_3, C_4) \), (e). capacitor voltages \( (C_2, C_1) \), (f). diode voltages \( (D_2, D_3) \), (g). diode voltages \( (D_3, D_4) \), (h). inductor voltages \( (L_1, L_2) \), (i). inductor voltages \( (L_3, L_4) \), (j). shoot through current \( (i_{th}) \), (k). line-voltage \( (v_{dc}) \), and phase voltage \( (v_{ph}) \).

As well as the voltage stress on diodes \( D_{1-4} \), are 32V, 190V, 190V and 147V, respectively. The input average current or \( L_4 \) inductor is approximately 4A and the current of inductors \( L_1, L_2, \) and \( L_3 \) are 3.2A, 4A and 4A, respectively. The voltages across the inductors \( L_{1-3} \) are the same in both shoot through and non-shoot through states, 150V, and –40V, respectively. This value for \( L_4 \) are 115V, and –35V, respectively. Also, the dc-link average current is approximately 1.5A. In Fig. 13 (a), the waveforms of the voltage and output phase current of the resistive load \( (R_{load} = 47\Omega) \) are shown in \( V_i = 48V \) and \( D = 0.2 \). The waveforms of the voltage and output phase current of the inverter with inductive-resistive load \( (R = 47\Omega, L = 55mH) \) in Fig. 13 (b) are shown in the same conditions as the resistive load and they indicates that the load current lags approximately 20° behind than of the voltage.

To identify the advantages and disadvantages of the proposed topology, the prototype of the EB-qZSI is constructed and the experimental results of Fig. 14 are obtained. As it is seen, in similar conditions, the comparative structure produces a lower voltage in the dc-link relative to the proposed structure. Therefore, according to the input current, the proposed structure delivers more output power to the load, and as shown in Figure 15, the proposed structure has higher efficiency. Input current ripple is equal in both structures. Also, the voltage stress on the capacitors in both structures is almost equal and only the capacitor \( C_4 \) of the proposed structure has higher voltage stress than other capacitors.
In Fig. 15 (a), the proposed inverter efficiency is compared with EB-qZSI, which indicates the higher efficiency of the proposed inverter at the different output powers. This can be due to the fewer diodes in the proposed structure than EB-qZSI. The measured efficiency of the proposed structure is compared to different values of the duty cycle in Figure 15 (b), which indicates lower losses in the low duty cycle and high modulation index.

![Fig. 15. (a). comparison proposed topology and EB-qZSI at D = 0.2.](image)

![Fig. 15. (b). proposed topology at different operating points.](image)

![Fig. 15. Measured efficiency at V_l =48V: (a) comparison proposed topology and EB-qZSI at D = 0.2 (b) proposed topology at different operating points.](image)

V. CONCLUSIONS

In this paper, a new topology was proposed that had a higher boost factor and higher voltage gain compared to CA/DA-qZSI, SL-(q) ZSI, EB-qZSI, rSL/cSL-qZSI, and iESL/ESL-qZSI. Based on the experimental results, the proposed inverter had a higher efficiency due to the lower number of diodes compared to the EB-qZSI with the same output power. Another advantage of this structure is the continuous input current, common ground between the input source and the inverter bridge. Given the experimental and simulation results, as well as the theoretical results from the proposed topology and EB-qZSI, the voltage stress of the capacitors and the diode is low and approximately equal. In the same condition, both structures had a low shoot-through current, and the current ripple of inductors and the current through the inductors were also low. The experimental results and simulation results with MATLAB/SIMULINK software have authenticated the relations and performance of the proposed structure, and had a good match between the simulation results and the experimental results.

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Alireza Karbalaei received the B.S degree in electrical engineering from Shahid Rajaee Teacher Training University, Tehran, Iran, in 2003, and the M.S degree from Azad University of Saveh, Iran in 2008. He is PhD student in Department of Electrical Engineering, Shiraz university of Technology, Shiraz, Iran. His current research interests includes impedance source converter.

Mohammad Mardaneh received the B.S. degree in Electrical Engineering from Shiraz University, Iran, in 2002, and M.S. and Ph.D. degrees in the same subject from Amirkabir University of Technology, Tehran, Iran, in 2004 and 2008, respectively. He is currently Associate Professor at the Shiraz University of Technology. His research fields cover: modeling, design and control of electrical machines, and application of power electronics in renewable energy systems and distribution networks.

Mokhtar Shasadeghi received his B.Sc. degree in Electronics Engineering from Shiraz University in 1996 and the M.Sc. and Ph.D. degrees from Tarbiat Modares University, in 2001 and 2007, respectively, all in Iran. He is currently Associate Professor at the Shiraz University of Technology. His research interests include robust control, fuzzy control, time delay systems, linear matrix inequalities, sum-of-squares decomposition and optimization.
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