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Reconfigurable CT QDSM with mismatch shaping dedicated to multi-mode low-IF receivers

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ABSTRACT

A reconfigurable third-order multi-bit continuous-time quadrature delta-sigma modulator (CT-QDSM) with mismatch error correction is reported in this paper. This modulator is designed for a tri-mode WLAN/WCDMA/GSM Low-IF (Intermediate Frequency) receiver. A three-bit quantizer is utilized to achieve the bandwidth (BW) and signal to noise ratio (SNR) required in WLAN/WCDMA standards. In this modulator, the adders are eliminated to optimize the power consumption. The excess loop delay of modulator is compensated by half of the sampling period of quantizer. The reconfigurable dynamic element matching (DEM) is proposed to eliminate the mismatch error. Therefore, the I and Q mismatch error are alleviated by designing the data weighted average (DWA) and homogeneous block (HB) circuits for WCDMA/WLAN modes respectively. In addition, the complex_digital to analog converter (C_DAC) is designed to eliminate the mismatch between I and Q paths. Implemented in 180 nm CMOS, it achieves 53.6/74.2/81.63 dB SNR and figure-of-merits (FoM) of 0.863/0.495/1.63 pJ/ (conversion step) with a 20/2/0.2 MHz BW for WLAN/WCDMA/GSM operational mode.

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I. INTRODUCTION

The current evolution of telecommunication systems goes toward versatile, reconfigurable and multi-standard receivers [1, 2]. In receivers, the Low-IF architecture is widely employed, since it can avoid the direct current (dc) offset and 1/f noise issues and suppress the image signal [3]. One of the important challenges in multi-standard Low-IF receivers is the design of analog-to-digital converter. Because of reconfigurable structure, noise shaping capability and high accuracy, delta sigma modulators (DSMs) are suitable for these receivers [4-6]. Moreover, QDSMs have been prevalently employed in low-IF receivers due to inherent antialiasing filtering characteristic and the potential for wide BW with low power consumption [3, 7-9].

A second-order multi-bit band pass CT-QDSM employing a quadrature mismatch scrambler for a tri-mode GSM-EDGE/UMTS/DVB-T low-IF receiver is reported in [10, 11]. This modulator employs power-scaling technique op-amp to optimize power consumption among each operational mode. A fourth-order band pass CT-QDSM with 33 MHz BW for a dual-channel global navigation satellite system (GNSS) receiver in 65-nm CMOS has been presented in [12].

This modulator had high power consumption and tendency to instability. A dual-mode second-order reconfigurable Feed Back (FB) CT-QDSM for a low-IF GNSS receiver has been presented in [3, 8]. This modulator has been capable of supporting both 5 and 20-MHz bandwidth and employed power scaling amplifier technique to effectively adjust the power consumption for BWs. A flexible feed forward (FF) low-pass and complex band-pass CT-QDSM architecture with a programmable BWs of 5 and 10 MHz and scalable power consumption implemented in 65-nm CMOS has been presented in [13]. A real FF multi-standard low pass hybrid continuous/discrete modulator with adder removed and noise shaping enhancement technique for a tri-mode WLAN/WCDMA/GSM has been presented in [14]. The modulator has been simulated in system-level by MATLAB.
In this paper, a reconfigurable FF QDSM is designed to support the WLAN/WCDMA/GSM telecommunication

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standards. Because the adder before quantizer has high power consumption and reduces the gain and bandwidth of the loop filter [15], it is eliminated in our design based on the systematic method mentioned in [16]. Multi-bit quantizer is employed in WCDMA/WLAN modes to satisfy the SNR requirements. Therefore, to eliminate the multi-bit DAC mismatch errors, the DWA algorithm has been used in the WCDMA standard and is designed for the fast homogeneous method for the WLAN standard. The mismatch between I and Q paths would also lead to SNDR degradation [17] and emerge the image signal [10, 11]. Also, to eliminate the mismatch error between I and Q paths, the complex DACs are designed.

Proposed Multi-standard QDSM and its System architecture are described in sections 2 and 3. The structural of mismatch error rejection details is outlined in section 4. The Implementation of complex resonator is introduced in section 5. The modulator Circuit implementation is described in section 6. Section 7, presents the results and compares them with previously published works. Finally, section 8 concludes the work.

II. PROPOSED MULTI-STANDARD QDSM

The prime subject in design of QDSM is selecting the architecture and parameters in order to satisfy the requirement in BW applications. The modulator BW and central frequency are determined by the loop filter coefficients and the SNR is calculated by equation (1) [3].

$$SQNR = \frac{3(2L+1)}{2\pi^{2L}} OSR^{2L+1} (2^N - 1)^2 \qquad (1)$$

In eq. (1), N is the number of the quantizer bits, L is the modulator order, and OSR is the oversampling ratio. Increasing the L reduces the modulator's stability and the OSR incrementing increases the modulator frequency and the power consumption. Moreover, increasing N limits the linearity of multi-bit modulator by its multi-bit DACs and linearization techniques is required to correct the mismatch errors [18].

In this paper, a multi-standard QDSM based on the presented method in the reference [16] is designed to WLAN/WCDMA/GSM standards. In this method, the adder is removed to reduce the power consumption and avoid adverse effects on the modulator loop filter. Based on these standards' characteristics, the center frequencies 0/1/10 MHz are chosen respectively, with the aim of SNR optimization.

A mono bit quantizer is employed in GSM mode and three-bit quantizer is employed to WCDMA/WLAN modes to satisfy the SNR requirement. A programmable DEM block is designed and implemented to decrease the mismatch noise and remove DAC nonlinearity error.

III. SYSTEM ARCHITECTURE

The FF topology is considered for design of this modulator. The modulator filter's transfer function is shown in equation (2) [16].

$$H(s) = \frac{k_1 A_3}{(s-\omega_1 i)} + \frac{k_1 A_2 k_3}{s(s-\omega_1 i)} + \frac{A_1 k_1 k_2 k_3}{s(s-\omega_1 i)(s-\omega_2 i)} \qquad (2)$$

In this equation ω1≡kc1 and ω2≡kc2 are the filter transfer function's poles, or noise transfer function's zeroes of the modulator. Proper placement of these zeroes in BW will increase the modulator SNR. In the proposed modulator the real coefficients are fixed and complex coefficients are variable in three operation modes to provide the BW and central frequency in each standard. As shown in Fig. 1 the FF topology chooses for implementing of proposed modulator.

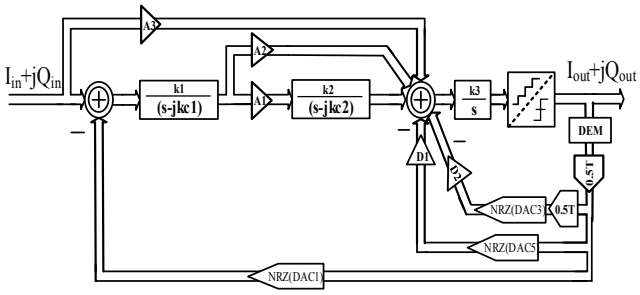


Fig. 1. Topology of the proposed multi-standard modulator

In this modulator, the adders are eliminated to reduce the power consumption and the feedforward paths applied to the last integrator [16]. The modulator's adders are removed and compensated the excess loop delay by half of the sampling period of quantizer [12]. In the modulator structure, in addition to main DAC1, two other DACs (DAC2, DAC3) are added to modulator due to compensate the delay loop and eliminated adders [16]. The modulator's real coefficients are shown in Table I. These coefficients are fixed in all modes. The complex coefficients are changed in different operating modes, as shown in the Table II.

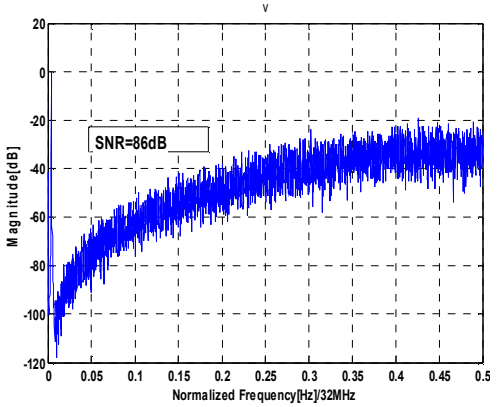
TABLE I
Real coefficient of modulator

A1	A3	D1	D2
0.4576	2.0537	0.3297	1.724

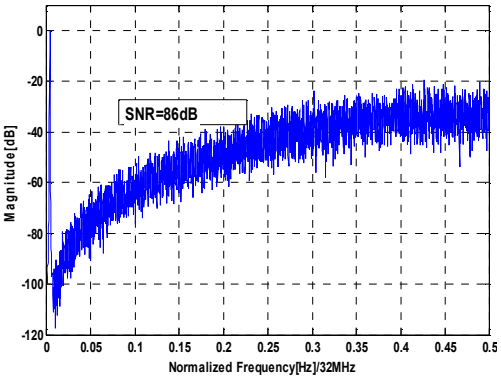
TABLE II
Complex coefficient of modulator

standard	A2	kc1	kc2
WLAN	1.3958+j0.9447	0.4060	0.181
WCDMA	1.3958+j0.1786	0.183	0.087
GSM	1.3958	0	0

As shown in Table II, in the GSM mode, the complex coefficients are zero and the modulator works in the real structure by one bit quantizer. The output spectrum of the modulator's system level at this mode is shown in Fig. 2. As shown in this figure, output power spectral density (PSD) and SNR are the same in both I and Q paths.



(a)



(b)

Fig. 2. System level Output PSD of modulator at I (a) and Q (b) paths in GSM mode

The modulator operates in quadrature in WCDMA and WLAN operational modes. System level output PSD of these simulation modes at the ideal status and 1 % mismatch error are shown in Figs. 3-4 respectively. As shown in figures, the mismatch reduces the SNR 15.36 and 2.06 dB in WCDMA and WLAN modes, respectively. The mismatch's effect is low in WLAN and it is corrected with a simple and fast DEM circuit.

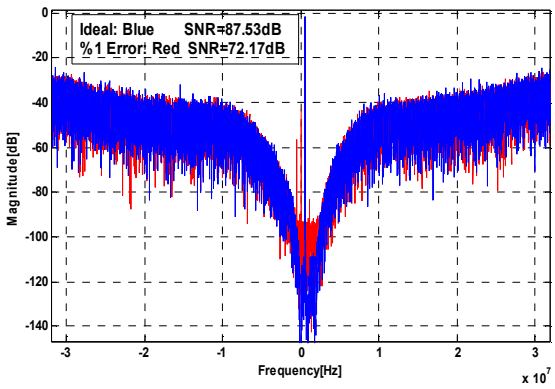


Fig. 3. System level PSD in the WCDMA mode at ideal and 1 % error

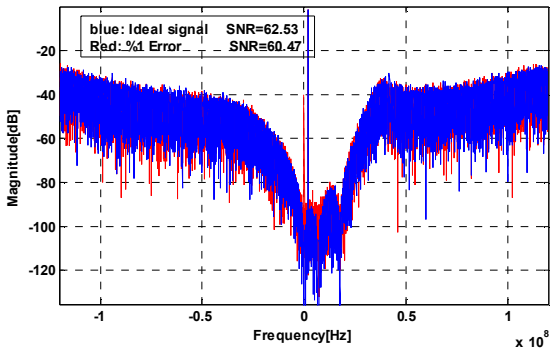


Fig. 4. System level PSD in the WLAN mode at ideal and 1 % error

IV. DEM DESIGN

In this paper, The DWA algorithm and complex DAC are employed to eliminate the mismatch errors in WCDMA mode. Moreover, the fast DEM method (HB) is proposed for WLAN mode, due to low effect of DAC mismatch errors and high speed of the modulator. In this mode, the DWA section is off and the HB and the complex DAC are on.

A. DWA structure

DWA algorithm has a pointer that indicates the start of DAC bits. An adder and a register are implemented to indicate the location of this pointer. In addition, XORs, binary to thermometer converters and MUXs are implemented to select the desired cells [19-21].

The block diagram of the data weighted average (DWA) is presented in Fig. 5. This algorithm utilized to eliminate the effect of their mismatch error, trying to make similar the probability of selecting each DAC cell at a given time interval.

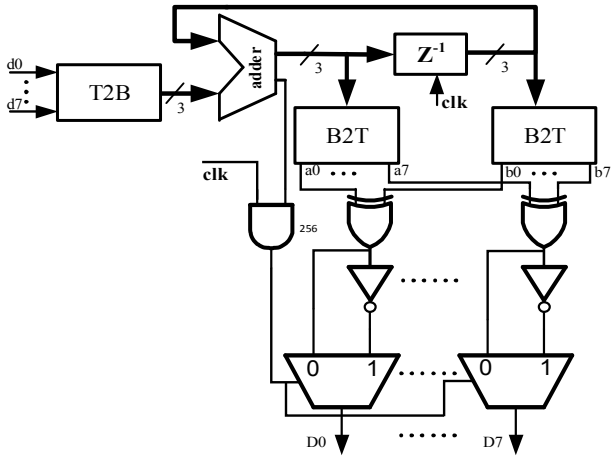


Fig. 5. Block structure of DWA_DEM algorithm

B. Proposed DEM method for WLAN mode

The distribution of ones and zeroes in the thermometric quantizer's outputs is shown in Fig. 6. This figure shows that the probability of lower bits to being one is more than the higher bits. Therefore, it's required to have a DEM block to homogenize the bit stream.

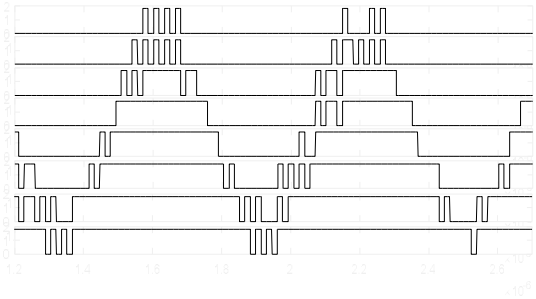


Fig. 6. One and zero distribution in at quantizer's outputs

The DWA algorithm is not suitable for WLAN mode, due to the speed limit. In this paper, a high speed and simple structure (HB) shown in Fig. 7 is proposed for this mode. In this method, each top and down pair bits of quantizer outputs apply to the one swapper[22] and replaced in decussate periods. As shown in Fig. 8, the output stream bits are become homogenized.

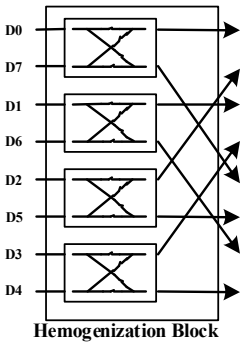


Fig. 7. Structure of homogeneous block (HB)

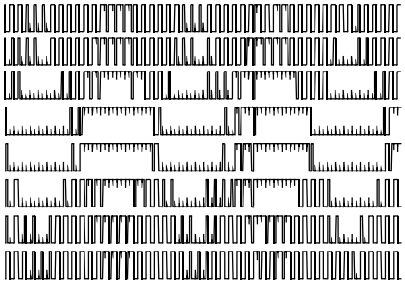


Fig. 8. One and zero distribution at homogenization block outputs

C. Implementation of C_DAC

Modulator's DACs are implemented by current string method to guarantee the high conversion speed [12, 15], and realized in complex mode to alleviate the I/Q mismatch error [3]. The block diagram of three-bit HB and C_DAC is depicted in Fig. 9.

The C_DAC consist of 16 cells that shared in two (I/Q) paths. Each cell consists of a swapper and a stream sequence, as shown in Fig. 10. In this structure the swapping sequence is done according to Table III, at the C_DAC cells.

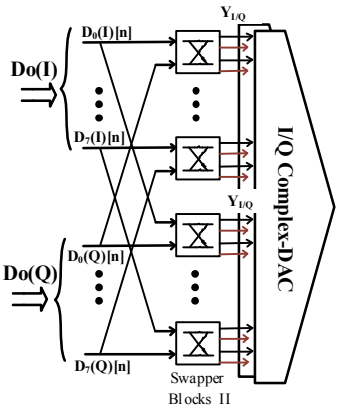


Fig. 9. HB section and C_DAC blocks

In this regard, depending on the values of the DI/DQ inputs, one of cell switches is illuminated and determined the path of the sequence. Therefore, all cells be shared in both I and Q paths then the mismatch error between two paths are alleviated. The governing equations for the selection of complex DAC cells are shown in equation (3). $D_{I,i}[n]$ and $D_{Q,i}[n]$ (i=0:7) are HB data outputs at n time that apply to C_DAC cells.

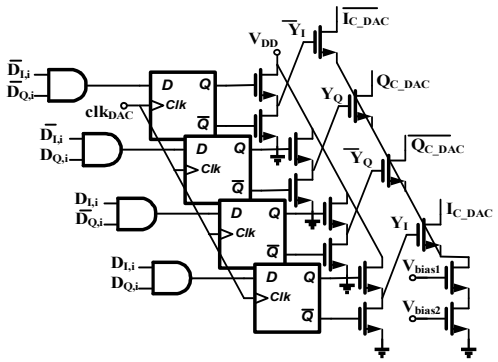


Fig. 10. The current-steering DAC unit with a swapper cell

The C_DACs bank take the signals from the I-DWA and Q-DWA circuits (in WCDMA) or I-HB and Q-HB (in WLAN) circuits and generate the current to apply to the filter path, as shown in Fig. 12.

$$Y_{I/Q,C\_DAC}\begin{cases} If\,(D_{I,i}[n]+jD_{Q,i}[n])=(0+j0)\Rightarrow Y_{I,C\_DAC}=D_Q \text{ and } Y_{Q,C\_DAC}=D_I \\ If\,(D_{I,i}[n]+jD_{Q,i}[n])=(1+j0)\Rightarrow Y_{I,C\_DAC}=D_I \text{ and } Y_{Q,C\_DAC}=D_Q \\ If\,(D_{I,i}[n]+jD_{Q,i}[n])=(0+j1)\Rightarrow Y_{I,C\_DAC}=D_I \text{ and } Y_{Q,C\_DAC}=D_Q \\ If\,(D_{I,i}[n]+jD_{Q,i}[n])=(1+j1)\Rightarrow Y_{I,C\_DAC}=D_Q \text{ and } Y_{Q,C\_DAC}=D_I \end{cases} \quad (3)$$

TABLE III
determines the direction of current tail

D_I	D_Q	Y_{I,C_DAC}	Y_{Q,C_DAC}
0	0	$\overline{Y_I}$	$\overline{Y_Q}$
0	1	$\overline{Y_I}$	Y_Q
1	1	Y_I	Y_Q
1	0	Y_I	$\overline{Y_Q}$

V. SIMULATION AND COMPARISON

A. Circuit implementation

The modulator integrators are implemented with active RC due to simplicity, linearity, parasitic insensitivity as well as the overall power consumption [23]. The modulator's resistors and capacitors are calculated by equation (4) for any standards.

$$f_s * A = \frac{1}{R * C} \quad (4)$$

It must replace the amount of resistors and capacitors by vary of the standards. This act is done by switches. In the modulator, the majority of the total power consumption is used in amplifiers. To save the power consumption, two amplifiers by different BW and power consumption are implemented in each integrator and replaced by switches, according to specification of standards. One of the modulator multi-standard complex resonators is shown in Fig.11.

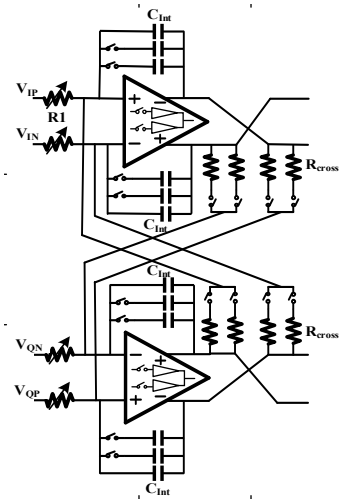


Fig. 11. Multi-standard complex resonator

The circuit implementation of proposed modulator is shown in Fig. 12. The first stage integrators are the most important modulator's integrators and consume a great part of the overall power. Therefore, telescopic op-amp due to low power consumption and large BW is suitable for first and third stages. Folded cascade op-amp is selected for second stage integrators because its input and output common modes can be adjusted independently [24, 25].

Flash analog to digital converter (ADC) is employed in quantizer block due to its speed. A three-bit flash quantizer is consists of eight comparators. Each comparator is consists of pre-amplifier, regenerative Latch, and SR Latch [15].

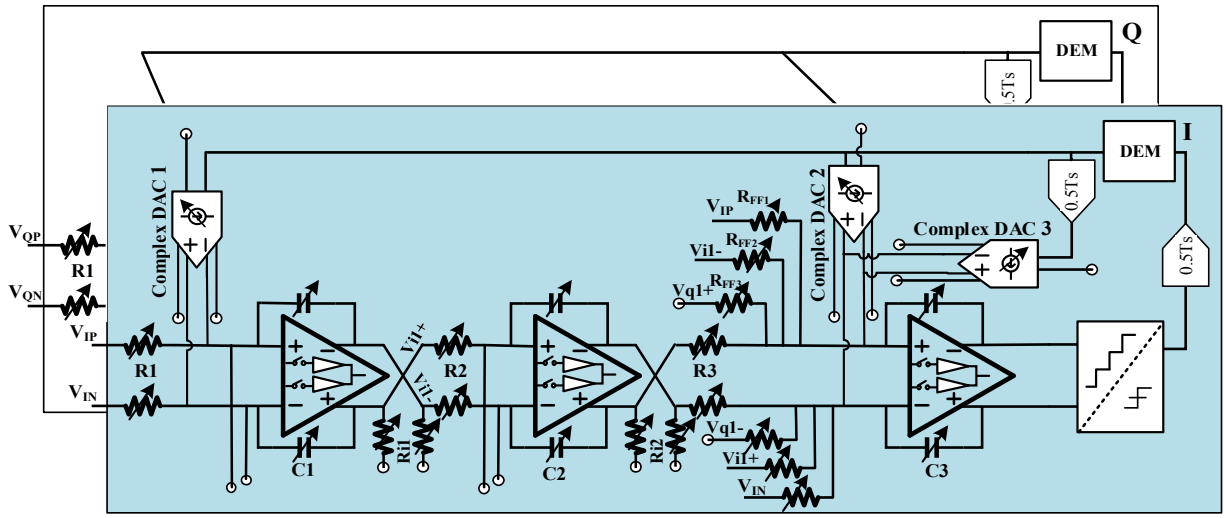


Fig. 12. Circuit of the proposed modulator

B. Simulation performance and comparison

The output spectrum of proposed modulator at transistor level in 180 nm technology in the Spectra-RF software and TSMC library are shown in Figs. 13-15, which have 53.6/74.2/81.63-dB SNR for WLAN/WCDMA/GSM operational modes, respectively.

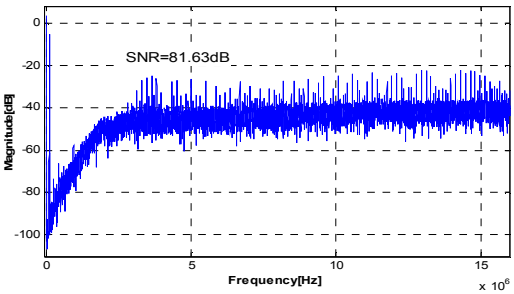


Fig. 13. Output PSD of the proposed modulator in GSM (BW 0.2 MHz) mode

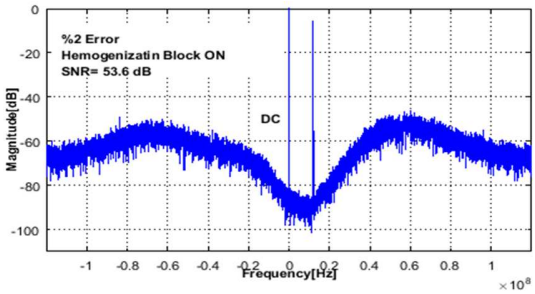


Fig. 14. Output PSD of the proposed modulator by 2 % error in DEM: on at WLAN (BW 20 MHz) mode.

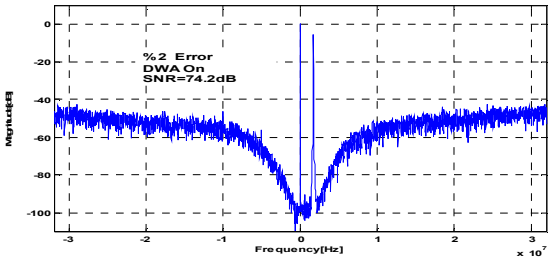


Fig. 15. Output PSD of the proposed modulator by 2 % error in DWA: on at WCDMA (BW 2 MHz) mode.

Table IV summarizes the simulation performance of the proposed QDSM and compares with some recent State of the art QDSMs. Here, criterion of comparison is FoM that it's defined by Power/(2×BW×2(SNDR−1.76)/6.02), and smaller FoM is better. Simulations represent the performance of the proposed modulator. As shown in Table IV, the proposed modulator has desirable performance in WLAN/WCDMA operational modes with FoM of 0.863/0.495, compared to similar cases presented in previous researches.

To saving the chip area, the op-amps employed in WCDMA mode are used in GSM mode. Due to the high speed of these op-amps, the OSR in the GSM operation mode is chosen to be high, in order to use mono bit quantizer. Thus, in this operational mode, the modulator does not need the DEM block. However, due to the high power consumption of these op-amps, FoM has increased in this mode with FoM of 1.63.

TABLE IV
Performance summary and Comparison

Ref.	Wireless standard	DSM structure	OSR	BW (MHz)	SNR (dB)	Technology (µm)	Supply voltage (v)	Power (mW)	FOM (pj/conv)
[12]	GNSS	QFB,FF4/CT	14	33	62.1	0.18	1.8	54.4	0.79
[11]	GSM-EDGE	QFB2/CT	190	0.27	81	0.18	1.8	4.9	0.99
	UMTS		24	5	61.2			8.9	0.95
	DVB-T		25	8	60.9			12.1	0.84
[26]	low-IF receivers	QFF3/CT	64	0.5	68.7	0.13	1.2	2.15	0.966
			32	1	60.6			2.13	1.21
			24	1.5	50.2			2	2.6
[27]	WLAN	QFB2/CT	16	16-20	54.5	0.25	2.5	32	2.07
[28]	GSM	RHybrid	160	0.2	91	System	--	--	--
	WCDMA	CT/DT	16	2	86	level			
	WLAN		10	20	73				
[29]	Zero/	LP/QBP CT	32	2.5	84.8	0.065	1.2	1.9	27
	low-IF receivers		32	5	85.8			2.6	16.3
			32	8	84.5			4.2	15.5
This work	GSM	QFF3/CT	162	0.2	81.63	0.18	1.8	6.4	1.63
	WCDMA		32	2	74.2			8.3	0.495
	WLAN		12	20	53.6			13.5	0.863

VI. Conclusion

A reconfigurable QDSM for multi-standard LOW-IF receiver is proposed in this paper. Multi-bit quantizer is employed to satisfy the SNR requirements and programmable DEM block (DWA/HB) is designed to mitigate the mismatch effects in WCDMA/WLAN mods. In addition, to remove the mismatch error between I and Q paths, C_DAC is designed. The output spectrum SNR of this modulator, by applying 2% error, Implemented in 180-nm CMOS, in WLAN/WCDMA modes with a 20/2 MHz BW are 53.6/74.2 dB and in GSM mode with mono bit quantizer and 0.2-MHz BW is 81.63 dB.

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